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Real-Time Implementation of a Packed U-Cell Seven-Level Inverter with Low Switching Frequency Voltage Regulator

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***Abstract*—In this paper a new cascaded nonlinear controller has been designed and implemented on the packed U-Cell (PUC) seven-level inverter. Proposed controller has been designed based on a simplified model of PUC inverter and consists of a voltage controller as outer loop and a current controller as inner loop. The outer loop regulates the PUC inverter capacitor voltage as the second DC bus. The inner loop is in charge of controlling the flowing current which is also used to charge and discharge that capacitor. The main goal of the whole system is to keep the DC capacitor voltage at a certain level results in generating a smooth and quasi-sine-wave 7-level voltage waveform at the output of the inverter with low switching frequency. The proposed controller performance is verified through experimental tests. Practical results prove the good dynamic performance of the controller in fixing the PUC capacitor voltage for various and variable load conditions and yet generating low harmonic 7-level voltage waveform to deliver power to the loads. Operation as an uninterruptible power supply (UPS) or AC loads interface for photovoltaic energy conversion applications is targeted.**

***Index Terms*— Packed U-Cell, Multilevel Inverter, Voltage Balancing, Nonlinear Controller, Renewable energy conversion.**

I. Introduction

Nowadays, power electronics converters are becoming exclusive in supplying high quality electric energy to various electric loads, and lately they are used to deliver renewable energies to the consumers [1-3]. Yet, power quality and harmonic issues pushed the power industries to design multifunctional, more energy efficient, and high density power electronics converters with less electromagnetic interferences [4-6]. Consequently, multilevel inverters have become inevitable topologies that could properly and efficiently answer the above mentioned issues. Conventional topologies known as 2-level inverters are being slowly replaced by such high efficiency devices that produce lower harmonic voltage/current due to multilevel quasi-sinusoidal waveform [7, 8].

Many topologies have been introduced for multilevel inverters that utilized combination of active switches and multiple isolated or dependent DC sources to generate different voltage levels at the output [9-17].

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The main challenging part of multilevel inverters is using less components count especially DC sources and power electronics devices to decrease manufacturing cost as well as reducing the package size [18-26]. Moreover, for the fast growing market of photovoltaic energy conversion applications, using less number of isolated DC sources means not requiring too many MPPT (maximum power point tracking) controllers to control output power and voltage of each separated solar arrays that results in simpler structure of the energy generation system [23, 27-29]. Among various reported topologies, PUC inverter has the less number of switches and DC sources by number of output voltage levels, while generating 7 voltage levels [30-33]. However, PUC topology requires complex controller to balance the dependent energy storage device voltage leads to reduce the number of isolated DC sources. As well, hysteresis current control has been applied on the PUC inverter to control the capacitor voltage at desired level that has its own related issues such as high and variable switching frequency which is undesirable for industries [34, 35].

In this paper a simple model of the PUC inverter is used which aims at defining a set of pulses for associated switches used in that topology. Based on formulated model, a cascaded nonlinear controller has been designed to fix the capacitor voltage (as dependent DC source) at one third of the reference voltage amplitude and consequently, to generate 7-level voltage waveform at the output with low harmonic contents and low switching frequency. This paper also deals with real-time implementation and experimental validation of the proposed controller in various conditions including change in load and also in DC source amplitude in stand-alone mode of operation. Generating 7-level voltage waveform using only six active switches, one isolated DC source and one capacitor combined with the proposed low switching frequency voltage controller makes this topology appealing for industries as a good candidate to replace conventional single-phase full-bridge inverter in various applications such as renewable energy conversion system, UPS, switch mode power supplies and etc.

Section II includes system configuration, modelling and proposed controller design procedure in details. Experimental tests of the designed controller implemented on the 7-level PUC inverter are performed using dSpace real-time controller. Tests results are illustrated and discussed in section III to verify the good dynamic performance of the proposed

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controller in tracking the reference signal to response quickly and precisely according to changes happening in the system like adding nonlinear load or DC source voltage variation.

II. PUC Inverter, Modelling and Controller Design

PUC inverter topology has been first introduced by Al-Haddad et al [30]. It consists of 6 active switches, one isolated DC supply and one DC capacitor as second DC source (or dependent DC source) which is shown in Fig. 1.

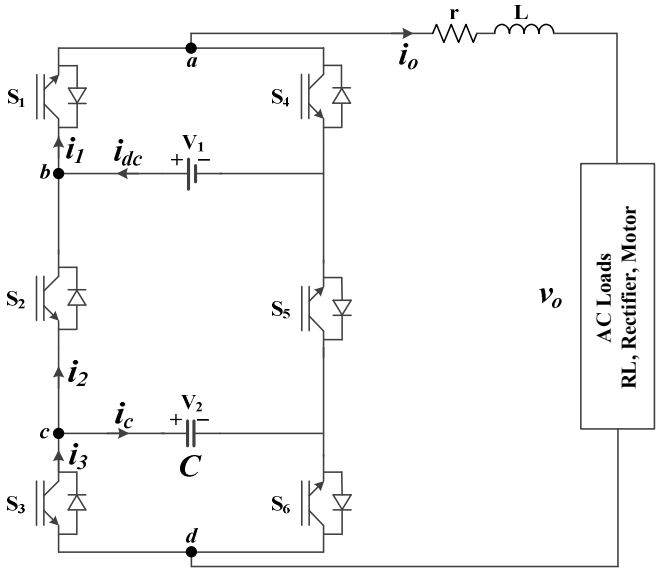

Fig. 1. Single-phase PUC inverter

The interesting advantage of PUC is the reduced number of components comparable to other topologies such as Cascaded H-Bridge (The less switches, the lower power losses, the less gate drives, the lower system cost. The output voltage levels of the single phase inverter topology of Fig. 1 are listed in table I. It should be mentioned that switches S_4, S_5 and S_6 are working in complementary of S_1, S_2 and S_3. So each pair of (S_1, S_4), (S_2, S_5) and (S_3, S_6) cannot conduct simultaneously.

To have all seven levels at the output voltage waveform, the capacitor voltage (V_2) should be 1/3 of the DC bus voltage V_1 (V_1=3V_2), so the output voltage levels would be 0, ±V_2, ±2V_2, ±3V_2. As it is clear, the PUC inverter cannot produce voltage level more than the DC bus voltage amplitude which is its prominent limitation. The maximum load voltage is equal to the DC bus voltage. In other words, it could be explained that the PUC advantage is to divide the DC bus voltage in multi levels to decrease the load voltage harmonics. This procedure reduces the required filters size at the output of the inverter.

The detailed dynamic model of the PUC inverter has been derived as follows [31, 35, 39]:

The switching functions of the PUC inverter shown in Fig. 1 are defined as:

$$S_i = \begin{cases} 0 & if\ S_i\ is\ Off \\ 1 & if\ S_i\ is\ On \end{cases} \quad i = 1,\ 2,\ 3 \tag{1}$$

The inverter output voltage can be formulated as:

$$v_{ad} = v_{ab} + v_{bc} + v_{cd} \tag{2}$$

TABLE I
SWITCHING STATES AND VOLTAGE LEVELS OF THE PUC INVERTER

Switching States	S1	S2	S3	V_{ad}
1	1	0	0	V_1
2	1	0	1	V_1-V_2
3	1	1	0	V_2
4	1	1	1	0
5	0	0	0	0
6	0	0	1	-V_2
7	0	1	0	V_2-V_1
8	0	1	1	-V_1

Where the points a, b, c and d are demonstrated in the above figure and each voltage can be computed based on the switching function:

$$\begin{cases} v_{ab} = (S_1 - 1)V_1 \\ v_{bc} = (1 - S_2)(V_1 - V_2) \\ v_{cd} = (1 - S_3)V_2 \end{cases} \tag{3}$$

By substituting (3) into (2),

$$\begin{aligned} v_{ad} &= (S_1 - 1)V_1 + (1 - S_2)(V_1 - V_2) + (1 - S_3)V_2 \\ &= (S_1 - S_2)V_1 + (S_2 - S_3)V_2 \end{aligned} \tag{4}$$

Similar to voltages relations, since one of switches in each pair of S_1&S_4, S_2&S_5 and S_3&S_6 are turned ON, the switches currents can be shown as a function of load current and switching function

$$\begin{cases} i_1 = S_1 i_o \\ i_2 = S_2 i_o \\ i_3 = S_3 i_o \end{cases} \tag{5}$$

Where,

$$i_3 = i_c + i_2 \tag{6}$$

$$i_c = (S_3 - S_2)i_o \tag{7}$$

$$\frac{dv_2}{dt} = \frac{(S_3 - S_2)i_o}{C} \tag{8}$$

As well, for the voltage and load current the KVL law is written as below:

$$v_o = v_{ad} - ri_o - L\frac{di_o}{dt} \tag{9}$$

Substituting Eq. (4) into (9), the following relation for the output current would be derived:

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$$\frac{di_o}{dt} = \frac{\left((S_1 - S_2)V_1 + (S_2 - S_3)V_2 \right) - ri_o}{L} = (S_1 - S_2)\frac{V_1}{L} + (S_2 - S_3)\frac{V_2}{L} - \frac{r}{L} i_o \quad (10)$$

In [31], three different duty cycles have been defined as (u_1, u_2, u_3) for each switches and a nonlinear controller has been designed accordingly; however, using 3 inputs for a single-phase inverter is not consistent with the concept of multilevel inverters in which a group of switches are closed to make a path for the current flowing through the load. Actually, those switches are not working separately to have individual duty cycles. In fact, they are turned on in a group of 3 at each level. Thus, the system input should be only one signal which is modulated by a multicarrier level-shifted PWM technique to produce required group of pulses that apply the associated voltage level at the output. For instance, one unclear issue raised from the previous work is the question that how does the controller or modulator selects the switching states (including a group of switches to generate a specific voltage level at the output) in a correct order to have respective voltage levels without any interference? To make it clearer, it can be said that when switches work independently, how the controller or modulator ensures that the voltage level (V_1-V_2) is generated exactly between levels V_1 and V_2 and there would not exist any problem like having level V_1 before V_2 that deforms the output multilevel waveform.

To present a solution for the above-mentioned issue, following two facts should be considered [40, 41]:

- A single-phase converter has only one output voltage or current waveform unlike the 3-phase one that has three output waveforms.
- Every controller designed for power converters can be categorized as voltage-control or current control depends on their output which is a voltage-type or current type signal.

Although single-phase multilevel inverter has more switches than a 2-level topology, it still generates one voltage and or one current waveform at its output. It uses higher number of switches in each conducting path, while they are not working independently. Actually, they work as a group and the group number is determined by the switching state as listed in Table I. The controlling signal is modulated and the modulator output data is the switching state number. Each state consists of a group of switches that should be turned on to produce corresponding voltage level at the output. Such structure ensures correct orders of voltage levels. To conclude, in a multilevel converter, switches act dependently as a group to generate desired voltage levels at the output in a correct order leads to have a smooth quasi-sine multilevel voltage waveform with low harmonic contents.

To comply with those facts, in this paper a new controller is designed based on a simplified model of the PUC inverter. It does have only one output signal which is modulated by a 6-carrier level-shifted PWM to generate associated switching pulses for all 6 switches dependently based on the switching states listed in Table I. Therefore, in this work, designed controller would send only one signal to the modulator (PWM) which is consistent with the concept of multilevel inverters switching as well as complies with the fact that single-phase converters controllers should produce one signal as their output which is sent to the modulator for pulse generation process. The 6-carrier level-shifted PWM scheme is shown in Fig. 2 where the reference wave is modulated by different carriers to produce the associated switching pulses for the 7-level PUC inverter.

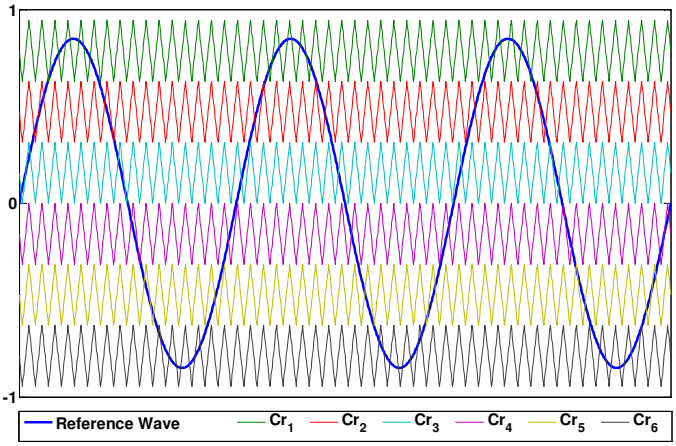

Fig. 2. Multicarrier PWM for 7-level PUC inverter

As mentioned earlier, to solve the problem regarding three individual inputs for a single-phase inverter, a simple model of the PUC inverter has been used to design a new controller in which only equations (8) and (9) are considered as voltage and current control sections respectively.

Based on Eq. (8) capacitor voltage is related to the load current therefore an equivalent signal u_v can be defined as:

$$u_v = C\frac{dv_2}{dt} = d_v i_o \quad (11)$$

Where, d_v depends on the switching functions of S_2 and S_3. To regulate the DC capacitor voltage (V_2), error signal of $\tilde{v}_2 = v_2^* - v_2$ should be minimized through the PI controller. Therefore:

$$u_v = k_{pv}\tilde{v}_2 + k_{iv}\int \tilde{v}_2 dt \quad (12)$$

Transfer function of the PI voltage controller is:

$$G_v(s) = \frac{U_v(s)}{\tilde{V}_2(s)} = k_{pv} + \frac{k_{iv}}{s} \quad (13)$$

Regarding Eq. (11), output of the voltage controller is u_v which is current-type signal. The capacitor voltage should be regulated by proper charging and discharging process which is done through the flowing current. As a cascaded controller concept, voltage controller can be used as outer loop and its output should go into the inner loop as a reference signal i_o^*. Controlled current goes through the capacitor and regulates its

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DC voltage at reference value. The inner loop is a current controller that is designed based on Eq. (9) and its dynamic should be fast enough to ensure good dynamic performance of the cascaded controller. Assuming that the outer loop regulates the capacitor voltage at the desired level and ensures $V_2 = 1/3\ V_1$, then:

$$\begin{aligned} v_{ad} &= (S_1 - S_2)V_1 + (S_2 - S_3)V_2 \\ &= (S_1 - S_2)V_1 + (S_2 - S_3)\ \frac{V_1}{3} \\ &= (S_1 - \frac{2}{3}\ S_2 - \frac{1}{3}\ S_3)V_1 \end{aligned} \tag{14}$$

Eq. (14) can be turned into Eq. (15) considering d_i as a signal depending on switching functions of S_1, S_2 and S_3.

$$v_{ad} = d_i v_1 \tag{15}$$

Substituting (15) into (9),

$$L\ \frac{di_o}{dt} + ri_o = d_i v_1 - v_o \tag{16}$$

Same as voltage controller design procedure shown above, an equivalent signal u_i can be defined as:

$$u_i = L\ \frac{di_o}{dt} + ri_o = d_i v_1 - v_o \tag{17}$$

The current can be regulated through a PI compensator in which the input is the error signal $\tilde{i}_o = i_o^* - i_o$ and the output is u_i:

$$u_i = k_{pc}\tilde{i}_o + k_{ic}\int \tilde{i}_o dt \tag{18}$$

Where the transfer function of the PI current controller is:

$$G_i(s) = \frac{U_i(s)}{\tilde{I}_o(s)} = k_{pi} + \frac{k_{ii}}{s} \tag{19}$$

Eventually, to derive the single input signal which should be modulated by level-shifted PWM, right side of the Eq. (17) is used as the following:

$$d_i = \frac{u_i + v_o}{v_1} \tag{20}$$

It should be noted for the inner loop (current control) that the PI controller would have performance where the input signal frequency is low (e.g. outer loop as DC voltage regulator); while it shows some steady-state error when the input is a time-varying signal, like a sinusoidal current, leads to tracking error in the line current. To ensure the possible minimum error on the output current, the integral gain of the $G_i(s)$ should be small enough which makes the inner loop faster than outer loop and results would be acceptable consequently. To ensure the good dynamic performance of the designed controller, inner loop dynamic should be at least five times faster than the outer loop controller. Therefore, the proportional gain of the inner loop PI should be higher than the outer loop one. Due to same reason, the inner loop PI integral gain should be smaller than the outer loop one. Gains are listed in Table II which comply with the above-mentioned points. The controller diagram is shown in Fig. 3 as well.

TABLE II
GAINS VALUES USED IN DESIGNED CONTROLLER

k_{pv}	3
k_{iv}	10
k_{pi}	30
k_{ii}	0.1

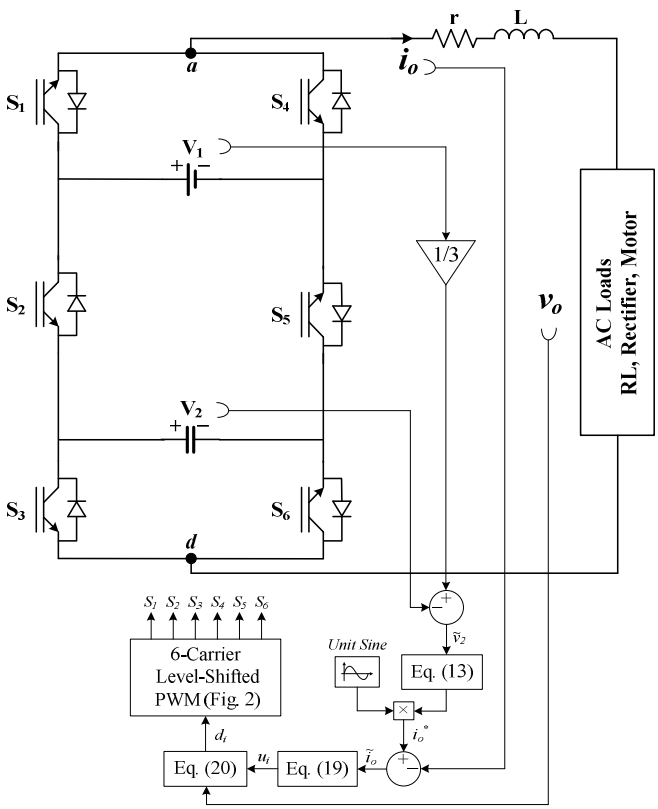

Fig. 3. Block diagram of proposed controller applied on 7-level PUC inverter

As depicted in Fig. 3, output of Eq. (13) which is the PI voltage controller is a DC signal so it should be multiplied by a unit sine-wave to generate a sinusoidal current waveform as a reference signal for inner loop. As explained earlier, the current is regulated through the PI with transfer function of (19). Afterwards, Eq. (2) is used to generate the final input signal to the system from the u_i. It is obvious that the output of the controller (that can be called system input) is a single signal d_i which is modulated by the 6-carrier levels shifter PWM to produce the required pulses.

The 7-level PWM shown in Fig. 2 includes six carriers to modulate the input signal. Six carriers are shifted vertically to cover d_i. Unlike the switching pattern described in the literature in which switching signals were produced for each switch separately; in this paper a group of switches would be

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fired by produced pulses from modulated signal. For instance, each carrier is responsible to generate pulses for group of three switches in three cells. For example if the reference wave is greater than Cr_1, then the higher voltage level which is V_1 would be generated at the output. Looking at Table I, it is clear that switches S_1, S_5 and S_6 should be turned ON. In the same manner, if reference wave is between Cr_1 and Cr_2 then the second voltage level (V_1-V_2) would be produced at the output terminal of the PUC inverter which requires switches S_1, S_5 and S_3 to be closed. All other switching states would be used to generate suitable switching pulses, similarly. Using multicarrier PWM technique ensures the low and fixed switching frequency of the inverter switches against the hysteresis switching technique used in the previous works. Moreover, it would prevent the undesirable jumping between switching sequences which was occurred in other reported techniques. This phenomenon results in injecting unwanted harmonics into the voltage and current waveform as well as producing more power losses due to higher dv/dt and higher switching frequency.

III. Experimental Results

A laboratory prototype for PUC inverter has been built using six 1.2KV 40A SiC MOSFETs type SCT2080KE active switches. dSpace 1103 is used for real time implementation of the designed controller which produces and sends associated pulses to the PUC inverter switches. Due to light calculations of the controller, low sampling time of 20us in implementation on the real-time controller is achieved which increases the controller accuracy significantly. System parameters used in practical tests are listed in Table III.

TABLE III
SYSTEM PARAMETERS USED IN PRACTICAL TESTS

Load Voltage Frequency	60 Hz
Inductive Filter (L_f)	2.5 mH
DC Source Voltage (V_1)	150 V
Regulated Capacitor Voltage (V_2)	50 V
Switching Frequency	2 kHz
RL Load	40 Ω, 20 mH
Rectifier as Nonlinear Load (DC Side R_{dc} and L_{dc})	40 Ω, 100 mH
DC Capacitor	2500 µF

In this part, the PUC inverter has been tested as stand-alone supplier which is connected to static RL load. This mode is suitable for PV system application in microgrids with small size filters, low THD voltage waveform and low power losses due to low and fixed switching frequency. Fig. 4 shows the test results in which capacitor voltage V_2 (50 V) is exactly regulated at one third of the V_1 (150 V) by the proposed controller. Moreover, the capacitor voltage ripple is measured around 1.9V which is acceptably less than 5% of its main voltage. 7-Level voltage waveform is formed at the output of the PUC inverter due to proper voltage regulation of the designed controller. It should be noted that voltage waveform before the L has been depicted in all figures which is demonstrated by V_{ad} in Fig. 1. THD of the 7-level V_{ad} is measured at 12% without using any voltage filter. With such THD% value, it could be ensured that although PUC topology has two more switches than conventional full-bridge inverter, it requires smaller filters that reduce manufacturing costs and increases the life time of the product significantly.

Moreover, the number of commutations is clearly low in this figure that validates the low switching frequency operation of the inverter running by the proposed controller. The lower switching frequency, the lower power losses and the higher efficiency.

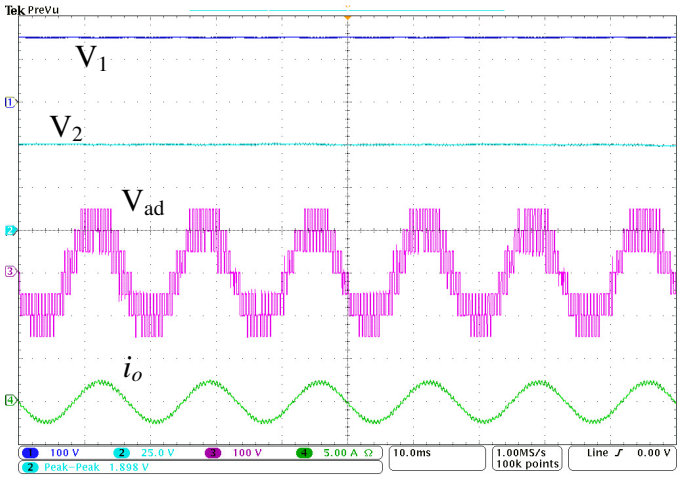

Fig. 4. PUC inverter voltage and current waveforms in steady state condition

In second test, the DC source voltage amplitude has been changed suddenly to validate fast response of the implemented controller in tracking the reference signal accurately. Fig. 5 shows the test result in which V_2 is tracking the reference value which is $V_1/3$ during change in V_1. V1 has been increased for 66% from 120V to 200V and V_2 smoothly follows the one third value from 40V to 66V highlighting good dynamic performance of the proposed controller. Seven-level voltage waveform of the inverter (V_{ad}) is increasing without losing symmetry on the voltage levels during the DC source voltage variation. Such situation can happen in startup of a motor with V/f control.

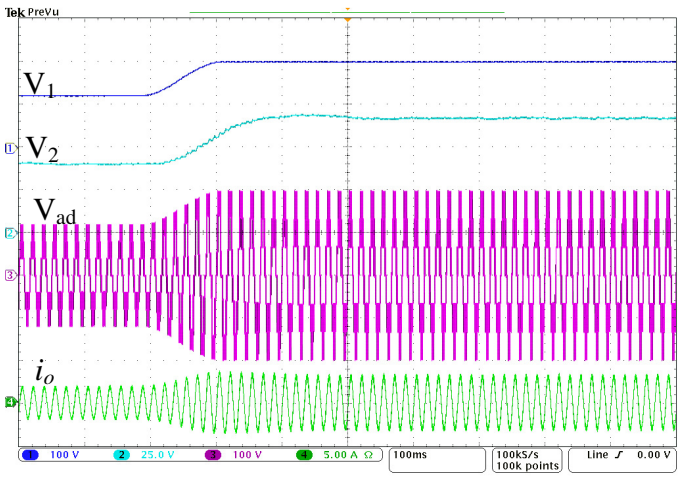

Fig. 5. Voltage regulation during a fast 66% increase in DC source amplitude

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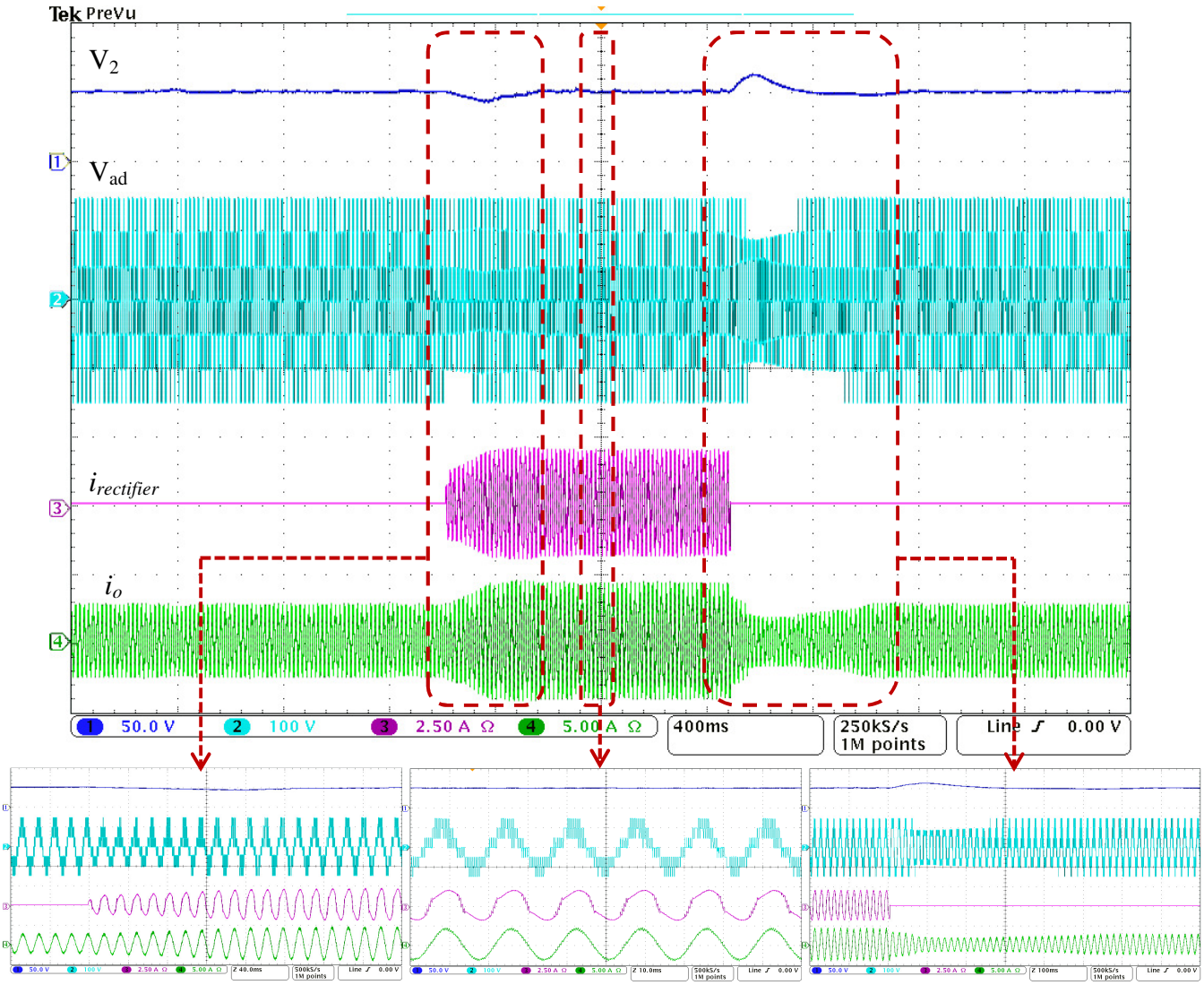

Fig. 6. Adding a nonlinear load (rectifier) to the PUC inverter while supplying an RL load

To show the good dynamic performance of the designed controller in load change conditions as well as appropriate action in harmonic environment, a nonlinear load consists of a single-phase rectifier with R_{dc} and L_{dc} on the DC side is connected to the PUC inverter while it was supplying an RL load. Results have been illustrated in Fig. 6 in which a current probe measures the rectifier AC side current demonstrating its harmonic contents clearly.

Considering zoomed figures, it is obvious that when a nonlinear load is added or removed from the output of the PUC inverter, applied controller adjusts the V_2 at the desired level and prevents any unbalancing in the capacitor and output voltages. Proposed controller fixes the capacitor voltage and produces seven-level voltage waveform at the output within an acceptable time limit.

Results validate acceptable performance of the proposed controller not only in fixing the PUC inverter capacitor voltage at desired level, but also in generating equal voltage levels in 7-level voltage waveform. Low switching frequency, fast response and good dynamic performance of the experimentally tested PUC inverter proves the excellence of proposed controller against other reported techniques. Moreover, it should be repeatedly mentioned that the system input is only one signal di which is regulated by the PWM technique and ensures the correct order of switching states to be produced and sent to associated switches. Using PWM technique in generating switching pulses leads to a fix switching frequency and also results proved that the PUC inverter can work in low switching frequency as mentioned in the system parameters.

IV. Conclusion

In this paper a new cascaded nonlinear controller has been designed for 7-level PUC inverter based on the simple model derived by multilevel inverter topology concept. Experimental results showed appropriate dynamic performance of the proposed controller in stand-alone mode as UPS, renewable energy conversion system or motor drive applications. Different changes in the load and DC bus voltage have been made intentionally during the tests to challenge the controller

reaction in tracking the voltage and current references. Proposed controller demonstrated satisfying performance in fixing the capacitor voltage of the PUC inverter, generating seven-level voltage with low harmonic content at the output of the PUC inverter and ensures low switching frequency operation of those switches. By applying the designed controller on the 7-level PUC inverter it can be promised to have a multilevel converter with maximum voltage levels while using less active switches and DC sources aims at manufacturing a low-cost converter with high efficiency, low switching frequency, low power losses and also low harmonic contents without using any additional bulky filters.

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