2015 IEEE International Symposium on Circuits and Systems (ISCAS)
DOI: 10.1109/ISCAS.2015.7168627

# A 1-V 690 µW 8-bit 200 MS/s Flash-SAR ADC with Pipelined Operation of Flash and SAR ADCs in 0.13µm CMOS

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***Abstract*—The successive-approximation-register (SAR) analog-to-digital converter (ADC) has recently attracted a lot of interest due to its power efficiency as well as its simple structure. The main challenge with this type of ADC is the limited sampling rate which is due to its sequential operation. In flash-SAR architectures, this problem is mitigated by cascading flash and SAR ADCs which operate in two consecutive phases. This paper presents a flash-SAR architecture which noticeably increases the ADC sampling rate using pipelined operation of the first-stage flash ADC and the second-stage SAR ADC. In the first stage, a low-power flash ADC is developed using charge distribution dynamic comparators which require no external reference generator. Using the proposed technique, an 8-bit ADC was designed in a 0.13 µm CMOS technology and its simulation results show an SNDR of 49.29 dB with 690 µW total power consumption at 200 MS/s and 1-V supply.**

Keywords— SAR ADC, flash ADC, low power, pipeline, time-interleaved, hybrid ADC**.**

## I. INTRODUCTION

Recently, extensive research efforts on energy-efficient analog-to-digital converters (ADCs) have been directed towards successive-approximation-register (SAR) ADCs. The low power consumption, simple structure and achievable improved performance due to technology downscaling are the main advantages of the SAR ADC, making it suitable for wide variety of applications. However, its sequential operation (i.e., one bit per step) limits its sampling rate which is generally undesirable. So far, several structures such as two-bit/step SAR ADCs [1] and time-interleaved ADCs (TI-ADCs) [2] have been proposed to eliminate this limitation. Two-bit/step architectures resolve two bits in each comparison step and thus only require N/2 clocks to determine N bits. Although this topology can boost the ADC speed, it is not efficient in terms of area and power consumption because it requires several comparators and reference generators. Alternatively, time-interleaved ADCs, which enhance the ADC sampling rate using several parallel channels, suffer from mismatch effects that hinder their performance.

Recently, new ADC architectures have been proposed which combine two or more different types of ADCs [3-5]. One of these hybrid structures is the flash-SAR architecture which takes the advantage of the high conversion rate of flash ADCs and low power consumption of SAR ADCs, creating an improved structure with a conversion rate that is higher than that of the SAR ADC, and with lower power consumption than that of the flash ADC. However, the operation of the flash and SAR ADCs remains sequential, limiting the conversion rate.

In this paper, a flash-SAR architecture with a pipelined operation of the flash and SAR ADCs is presented to improve the conversion rate without considerable added power consumption and complexity. To further increase the ADC conversion rate, a SAR ADC with two capacitive digital-to-analog converters (CDACs) is employed in the second stage to provide concurrent operation of the flash and SAR ADCs. Moreover, a low power flash ADC, which does not require a resistive ladder or any other reference generator, is used in the first stage, leading to increased power efficiency.

This paper is organized as follows. Section II describes the proposed flash–SAR ADC and its pipelined operation. Section III discusses the detailed circuits and design considerations. Section IV presents the simulation results, and finally, a brief conclusion is given in Section V.

## II. PROPOSED PIPELINED FLASH-SAR ARCHITECTURE

Flash-SAR architectures combine a low-resolution (and thus low-power) flash ADC with a SAR ADC to overcome the limited conversion rate of the SAR ADC [3].

In the typical flash-SAR architecture [3, 5], the flash and SAR converters sequentially work in two distinct consecutive phases. In other words, in the first phase, the flash ADC resolves the first coarse bits and then the MSB capacitors in the DAC array of the second stage are switched according to MSB values. In the second phase the SAR ADC starts the LSB conversions, and the fine bits are determined after several steps. With such a sequential procedure, the flash-SAR architecture does not significantly increase the sampling rate.

In the proposed architecture, the flash ADC performs all coarse conversions in one step, and then all the MSB capacitors are simultaneously switched by the coarse bits of the flash ADC to complete the conversion. Therefore, the total number of comparison cycles is reduced compared with a typical SAR ADC and, hence, the conversion rate is enhanced.

Accordingly, similarly to other flash-SAR architectures, the proposed ADC has two conversion phases: the coarse conversion phase which is accomplished by the first-stage flash ADC, and the fine conversion phase which is accomplished by the second-stage SAR ADC. The sampling rate of the flash-SAR ADC can be further increased by concurrent operation of the first and second stages which is almost similar to that of pipelined ADCs. The operating principle is that before completing the fine conversion phase by the SAR ADC, the flash ADC starts the coarse conversion

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of a new sample. In a typical flash-SAR ADC, sampling and coarse conversion phases take almost 35% of the total conversion time [3]. Therefore, the proposed pipelined operation increases the sampling rate by about 35% compared with a typical flash-SAR ADC. To realize this pipelined operation of flash and SAR ADCs, two CDACs are required.

Figure 1a shows the block diagram of the proposed flash-SAR ADC. A 3.5-bit flash ADC is used in the first stage and a 5-bit SAR ADC is employed in the second stage. In each cycle, coarse and fine conversions are performed concurrently based on the following steps:

*A. Coarse Conversion Phase*

1- The input signal is sampled and digitalized by the flash ADC, and the first 4 bits are determined.
2- This input is simultaneously sampled on CDAC1 to perform its fine conversions in the next phase.
3- After coarse conversion, the related MSB capacitors of CDAC1 are switched.
4- In the next conversion cycle, steps 1-3 are repeated using CDAC2 since CDAC1 will be under its fine conversion phase.

*B. Fine Conversion Phase*

1- After the coarse conversion phase, the CDAC1 LSB capacitors are switched in a similar fashion to that in SAR ADCs (using a comparator and the SAR logic), and the LSB bits are determined.
2- In the next conversion cycle, step1 is repeated using CDAC2, because CDAC1 is used for sampling.

In comparison with other flash-SAR architectures, only an additional CDAC and a few digital circuits are added to the ADC structure. Therefore, the pipelined operation can be implemented without a considerable power and area penalty.

The use of a low-power flash architecture is another key advantage of the proposed ADC. In the first stage, a 3.5-bit flash ADC is implemented using dynamic comparators (with no pre-amplifier). This flash ADC does not require a resistive ladder or pre-amplifier to generate the decision levels. Therefore, these two typical sources of power dissipation are removed in the first stage. However, the DC offset of these dynamic comparators can significantly degrade the accuracy of the flash ADC. In practice, for high-resolution ADCs, it is difficult to design a dynamic comparator that meets high accuracy requirements. Here, the design employs a commonly-used digital error correction method used in pipelined ADCs to relax the requirement of the flash comparators. Based on this method, an overlapping bit between the first stage (i.e., flash ADC) and the second stage (i.e., SAR ADC) is used.

Figure 1b shows the timing diagram of the proposed ADC. In the first cycle, the input signal is sampled by the flash converter and CDAC through CLKS and $CLKS_1$, respectively. Then, in the coarse conversion phase (latch=1), the flash ADC determines the first 4 bits. Afterwards, the MSB capacitors of CDAC1 are switched depending on the value of coarse bits. Then, the SAR comparator is connected to CDAC1 on the rising edge of $\Phi_{DAC1}$ (fine conversion phase) and the SAR starts the LSB conversions. Before the completion of this

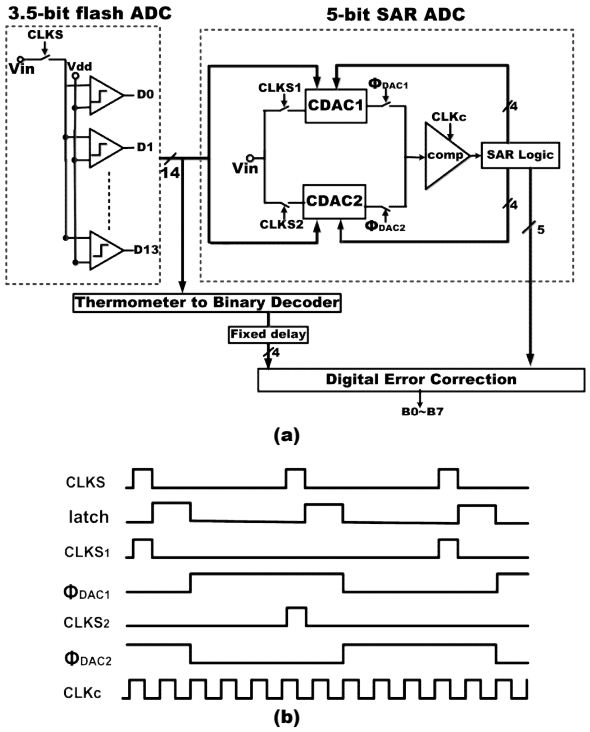


Fig. 1. Proposed 8-bit flash-SAR ADC: (a) block diagram, (b) timing diagram.

phase, $CLKS_2$ and CLKS are enabled and the input signal is sampled by CDAC2 and the flash ADC. Then, while CDAC1 is converting the last LSBs of the first sample, the flash ADC concurrently determines the coarse bits of the new sample. Note that, at the end of $\Phi_{DAC1}$ phase**,** five LSBs of the first sample are determined along with four MSBs of the second sample. At the rising edge of $\Phi_{DAC2}$**,** LSB conversions of the second sample start. Finally, the flash ADC's 4 bits and the SAR ADC's 5 bits are delivered to digital error correction (DEC) block. The DEC corrects the digital code by overlapping 1 bit between two stages yielding a total of 8 converted bits.

## III. Circuit-Level Implementation

*A. Flash ADC (Coarse ADC)*

In most flash converters, a power hungry resistive ladder is used to generate the decision levels. To reduce the power consumption of the flash coarse ADC, this work takes advantage of replacing the comparator and resistive ladder with charge-distribution dynamic comparators [6] that do not require an external reference voltage generator (Fig. 2). In these comparators, which are widely used in pipeline ADCs, the decision levels are generated by means of dividing capacitors ($C_{IN}$ and $C_{REF}$). The comparator shown in Fig. 2 performs the comparison in two phases. In the sampling phase (CLKS=1), the dividing capacitors are pre-charged to $V_{IN}$ and $V_{REF}$, then in the comparison phase (latch=1), the capacitor bottom plates are grounded and the capacitor charge redistribution constitutes a threshold voltage which can be expressed as [6]:

$$V_{IN}^{+} - V_{IN}^{-} = \frac{C_{REF}}{C_{IN}} \times (V_{REF}^{+} - V_{REF}^{-}) \quad (1)$$

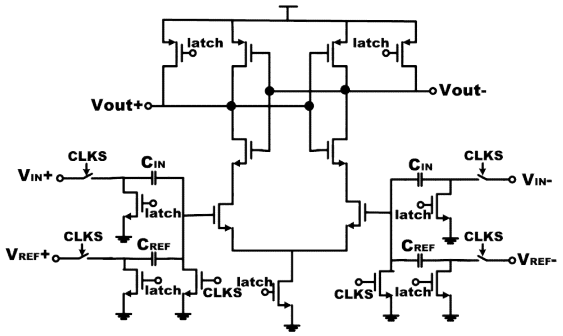


Fig. 2. Charge distribution comparator [6].

In the comparison phase, the input signal is compared with the threshold of $\frac{C_{REF}}{C_{IN}} \times (V_{REF}^{+} - V_{REF}^{-})$. As it could be concluded from (1), the threshold voltage of the comparator varies linearly with the capacitance ratio ($C_{REF}/C_{IN}$). Therefore, the reference voltages required for the decision of the comparators can be obtained by varying the $C_{REF}/C_{IN}$ value. This structure eliminates the resistive ladder requirement and, hence, enhances the flash converter power efficiency.

In this topology, transistor mismatches can seriously affect the comparator offset. The mismatch of the input transistors arises mostly from the threshold voltage mismatch. The standard deviation of the offset voltage induced by threshold voltage mismatch can be expressed as:

$$\sigma_{VTH} = \frac{A_{VTH}}{\sqrt{WL}} \tag{2}$$

where W and L are transistor dimensions and $A_{VTH}$ is a process-dependent parameter which is a value around 5 mV·µm in the 0.13 µm CMOS process used. For L = 0.13 µm and W = 0.5 µm (as used in this work), the standard deviation of the offset voltage calculated from (2) is 19.6 mV. As mentioned before, in this design, the offset requirement of the flash comparators is effectively relaxed by employing a 3.5-bit flash structure and one bit overlapping between coarse and fine stages. This technique eliminates the need for a pre-amplifier in the flash comparators. For a 2 $V_{p\text{-}p}$ input swing, this structure can tolerate up to 62.5mV offset in the flash comparators which is sufficient to accommodate the expected $\sigma_{VTH}$.

### B. SAR ADC (Fine ADC)

To determine the fine bits, a 5-bit SAR ADC with two CDACs is employed in the second stage. Each of the CDACs is designed as a segmented DAC similar to that in [3]. As shown in Fig. 3, the segmented CDACs are composed of 28 unary-weighted capacitors and 10 binary-weighted capacitors. The unary-weighted capacitors are directly switched by the flash comparators' thermometer output, and those that are binary-weighted are controlled by digital control logic, depending on the SAR comparator decision.

The SAR ADC in the second stage utilizes the monotonic switching procedure for the LSB capacitors (binary-weighted capacitors). An important advantage of this method over the conventional one is that the average switching energy is reduced by ~81%, and the total capacitance in the CDAC array is decreased by 50% [7]. This reduction in CDAC area becomes important in this design, since two CDACs are required to implement the proposed technique.

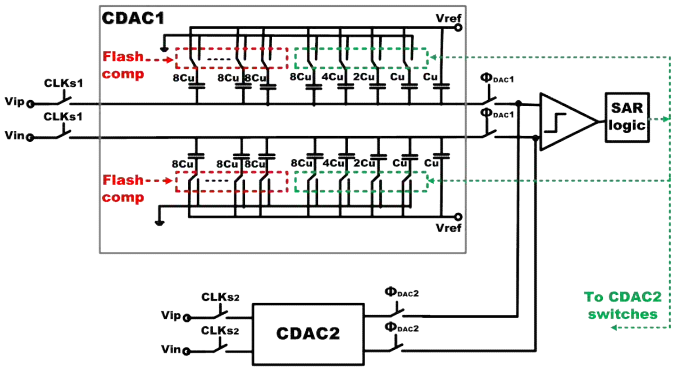


Fig. 3. Second-stage SAR ADC with two segmented DACs. Either CDAC1 or CDAC2 is connected to the comparator and the SAR logic.

An important issue in the multi-channel ADCs (especially with a large number of channels) is the matching amongst channels. Although the proposed design does not use separate channels, mismatches between the two CDACs may reduce the performance of the ADC. Specifically, the impact of the gain, offset, and timing mismatches on the proposed ADC can be studied as follows:

#### 1) Gain Mismatch

In the proposed ADC, the capacitor mismatch of the second-stage CDACs would result in a gain mismatch. Similar to time interleaved ADCs the gain matching requirement for CDAC1 and CDAC2 in the second stage is given by [8]:

$$SNDR_{gain,mis} = 20\log\left(\frac{1}{\sigma_{g,mis}}\right) - 10\log\left(1 - \frac{1}{M}\right) \tag{3}$$

where M is the number of channels and represents the number of CDACs in our case. To obtain a 50 dB SNDR (8 bits), the $\sigma_{g,mis}$ should be less than 0.44%. This value can be directly achieved using proper layout design techniques such as common-centroid patterns with matched interconnects.

The unit capacitor is usually determined by the thermal noise and capacitor mismatch. However, the capacitors mismatch which affect non-linearity parameters of the ADC such as integral non-linearity (INL) and differential non-linearity DNL) is dominant over thermal noise for medium resolutions. For an N-bit flash-SAR ADC, variance of the maximum DNL error can be expressed as [3]:

$$\sigma_{maxDNL}\left(\frac{FS}{2}\right) = \sqrt{\frac{3}{2^{Tc}}} \times \frac{\sigma_0\sqrt{2^{N-1}}}{C_0}\, LSB \tag{4}$$

where $C_0$ is unit capacitance, $\sigma_0$ is the standard deviation of a unit capacitor random offset, $T_C = \lceil T \rceil$ is the ceiling function value of T, and T is the resolution of the flash coarse ADC [3]. To have high yield, it is necessary to achieve $3\sigma_{maxDN} < \frac{1}{2}LSB$. The minimum value of unit capacitor to satisfy this requirement can be obtained using (4); assuming that capacitor mismatch is dominated by oxide variation, we have:

$$\frac{\sigma 0}{C0} = \frac{\alpha 0}{\sqrt{C0}} \tag{5}$$

where $\alpha_0$ is a technology-dependent coefficient. Manipulating (4) and (5) the minimum value of unit capacitor can be calculated as:

$$C_0 > \alpha_0^2 \times 54 \times 2^{N-Tc} \tag{6}$$

For N= 8 and $T_C$=4 (as used in this work), considering $\alpha_0$ lies in the range of 1% and the worst-case value of 3% (for the

0.13 µm CMOS process used), the minimum unit capacitor should be larger than 0.086 fF and 0.77 fF to fulfill the CDAC matching requirement. The value of the unit capacitor in this design is 3 fF which satisfies the above condition.

*2) Time-skew Mismatch*

Another important issue in the multi-channel or multi-stage ADCs is timing mismatch or timing skew. The timing skew greatly depends on the routing of signal and layout design. Therefore, the layout should be designed such that all signals have the same delay. The timing skew requirement for an M-channel ADC can be expressed as [8]:

$$SNDR_{time,mis} = 20\log\left(\frac{1}{\sigma_t\, 2\pi f_{in}}\right) - 10\log\left(1-\frac{1}{M}\right) \quad (7)$$

For M = 2 (number of CDACs) and SNDR = 50 dB at the input Nyquist frequency ($f_{in}$ = 100 MHz), $\sigma_t$ should be less than 7.11 ps. Owing to the simple structure and the low number of channels (two CDACs), the proposed ADC does not require complex routing for signals; thus, it is directly possible to achieve the timing matching conditions better than 7.11 ps.

*3) Offset Mismatch*

Offset mismatch is another error which degrades the performance of multi-channel and multi-stage ADCs. This problem is usually dominated by comparator offset. The proposed ADC shares one comparator between two CDACs in the second stage; thus, there is no considerable offset mismatch error in this stage. Moreover, in the first stage, the flash ADC uses 14 coarse comparators for MSB decisions. In these comparators, the offset error may cause an inter-stage offset error. As previously explained, this problem is mitigated through the use of a 3.5-bit flash ADC architecture and a one bit overlapping between the coarse and fine stages.

## IV. Simulation Results

The proposed flash-SAR ADC is simulated in a 0.13 µm CMOS technology. The simulation has been done with a mismatch of 5% applied to the input transistors of the flash comparators. Due to 1-bit overlap between the first and second stages, this mismatch is tolerable and does not degrade the ADCs performance. At the sampling frequency of 200 MS/s, the ADC consumes 600 µW from the 1 V supply. Figure 4 shows a 512-point FFT spectrum for a 70-MHz input signal, where the signal-to-noise and distortion ratio (SNDR) is 49.29 dB and spurious-free dynamic range (SFDR) is 62.93 dB. These results translate to an effective number of bits (ENOB) of 7.89 bits. The achieved figure-of-merit (FOM) is of 14.5 fJ/conversion-step.

The ADC has been simulated at five process corners and simulation results are summarized in Table I. The results imply that the ADC has an acceptable performance at different process corners.

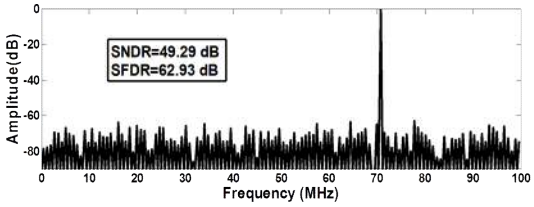

Fig. 4. FFT spectrum at 200 MS/s and with a 70 MHz input.

Table II compares the proposed ADC with other similar works such as flash-SAR and hybrid time-interleaved ADCs. As can be seen in Table II, the proposed ADC compares favorably to other works.

TABLE I. Simulation results in corners process.

| Process corner | Power (mW) | SNDR (dB) | SFDR (dB) | ENOB (bit) | FOM (fJ/conv.-step) |
|---|---|---|---|---|---|
| **TT** | 0.69 | 49.29 | 62.93 | 7.89 | 14.54 |
| **SS** | 0.59 | 49.78 | 63.15 | 7.97 | 11.76 |
| **FF** | 0.84 | 47.8 | 65.94 | 7.64 | 21.05 |
| **SF** | 0.6 | 49.29 | 65.08 | 7.89 | 12.64 |
| **FS** | 0.61 | 48.9 | 63.35 | 7.83 | 13.4 |

TABLE II. Comparison to the state-of-the-art.

| **Specification** | [2][a] | [3][a] | [4][a] | [5][a] | This Work[b] |
|---|---|---|---|---|---|
| **Resolution(bit)** | 10 | 9 | 9 | 9 | 8 |
| **Supply Voltage (V)** | 1 | 1.2 | 0.9 | 1 | 1 |
| **Speed (MS/s)** | 170 | 150 | 90 | 100 | 200 |
| **Power (mW)** | 2.3 | 1.53 | 13.5 | 6.1 | 0.69 |
| **SNDR (dB)** | 53.2 | 54.07 | 51.8 | 51.94 | 49.3 |
| **ENOB (bit)** | 8.54 | 8.69 | 8.31 | 8.33 | 7.89 |
| **FOM (fJ/conv.-step)** | 36.4 | 24.7 | 472 | 190 | 14.5 |
| **Technology** | 65nm | 90 nm | 90nm | 45nm | 130nm |

[a] measured results
[b] simulation results

## V. Conclusion

In this work, a flash-SAR architecture has been presented that utilizes a pipelined operation between the flash and SAR ADCs to further increase the ADC's conversion rate. To realize this pipelined operation, two CDACs in the second stage are required. A one bit overlap between the flash and SAR stages is also implemented to relax the requirements of the flash ADC comparators. Thus, these comparators are realized with a low-power dynamic latch structure requiring no pre-amplifier or resistive ladder. The proposed 8-bit ADC is simulated in a 0.13 µm CMOS technology at all corners and a FOM of 14.5 fJ/conversion-step at 200 MS/s is achieved.

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