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An Efficient Reference-Based Adaptive Antenna Impedance Matching CMOS Circuit

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***Abstract*—This paper presents a simple integrated reference based adaptive matching network capable of undertaking real time antenna tuning for applications such as wearable wireless sensors. The signal sent to the antenna is compared to a reference signal using a single flip-flop acting as a phase detector. In case of an impedance mismatch, a counter controlling a capacitor bank is activated reducing the sensed mismatch. The system is capable of three modes: calibration, matching and operation. The calibration mode ensures that the reference signal is in phase with the signal sent to the antenna when the impedance of the antenna is 50 Ω. In matching mode, the capacitor bank is adjusted to maintain antenna matching. In operation mode, the circuit is shut off allowing for low power consumption (85 nW while matching every 1 ms). The circuit is able to provide a VSWR < 2 over a wide range of antenna impedance levels. It is designed in CMOS 0.13 µm technology.**

I. INTRODUCTION

Adaptive matching networks are used in a wide range of systems in which there is a dynamic variation of the load impedance in order to ensure optimal power transfer to the load at all times. Such dynamically varying impedances are widely seen in wireless communication systems. Specifically, in mobile phones and emerging wearable wireless sensors, an integrated, low power, effective and robust adaptive matching network is of great importance. In such applications, the performance of the antenna is sensitive to its proximity to the human body causing significant time-varying shifts in impedance levels during device use. This shifts lead to a reduction of the power efficiency and therefore of battery lifetime of a given device [1-3].

Fixed matching networks designed for static impedances can be used, but become less efficient as the impedance varies [4]. Alternatively, adaptive matching networks are dynamically adjustable systems composed of variable capacitors or inductors minimizing antenna mismatch comprised in a certain impedance range. They are composed of three main parts: mismatch detector, control circuit and variable elements.

For the control circuit, there are mainly two approaches. The first one uses processors and algorithms [5-7]. While very accurate, these circuits require more space, power and are difficult to integrate. The second approach which is the scope of this paper uses a feedback circuit [8-10] and does not present the disadvantages of the first approach.

The main approaches to realize the mismatch detector, are: detection of the reflected power using a coupler [11], detection of the phase shift using voltage and current probes [8-9], and comparison with a reference signal. The latter is the technique presented in this paper.

The variable matching elements can be inductors, capacitor arrays, varactors or a combination of them. These elements need to have low parasitics, high tuning ratio and be highly linear to ensure little impact on the antenna. Generally, integrated components have low quality factors, and have small values which make it difficult for achieving high tuning ratio. Therefore, to the knowledge of the authors, a completely integrated adaptive matching network has not be realized yet. In [8] a sophisticated technique for controlling the imaginary and real part of the antenna impedance is presented. A quadrature detector extracts the impedance values. Then, the real and imaginary parts are independently adjusted using two control loops with inductances and capacitors in parallel and in series. This circuit however was not fabricated due to the unavailability of highly linear, high-Q variable elements as mentioned by the authors. In [9] a simplified version of the circuit presented in [8] is presented and has been implemented where RF-MEMS switches are used to control a capacitor array in series with the antenna. Because the adaptive matching network should not add parasitics to the antenna, low-resistance RF-MEMS switches are well suited for this application. However, they require a high actuation voltage and cannot typically be monolithically integrated into standard CMOS process nodes.

Accordingly, this paper presents a completely integrated antenna tuning circuit that is effective over a wide range of impedances while being simple, easy to implement and uses

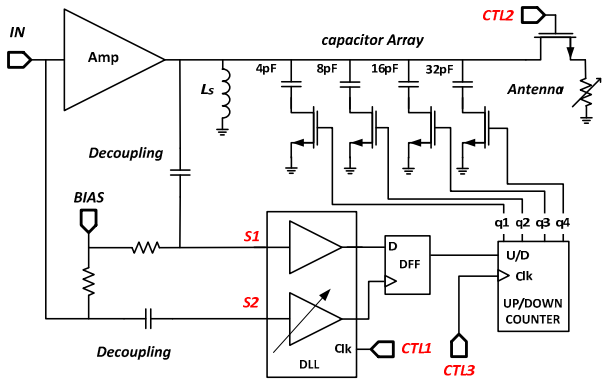

Figure 1: Circuit schematic of the reference based adaptive matcing circuit.

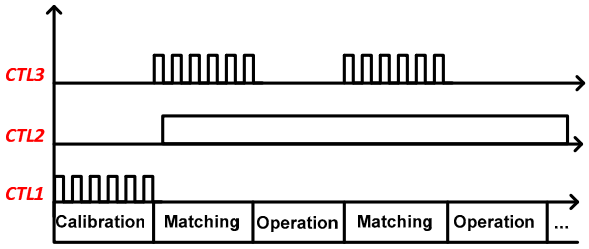

Figure 2: Temporal diagram of the different operation modes.

an agile power cycling technique allowing for very low power consumption. The target application is a communication system with a frequency of 900MHz and a 50 Ω antenna. A system description is given in section II, the simulation results are presented in section III and the layout is presented in section IV.

II. System Description and Design

The circuit shown in Fig. 1 is composed of a capacitor bank, an up and down counter, a flip-flop based phase detector, a delay lock loop, an amplifier and a switch to connect or disconnect the antenna. The IC is designed in IBM CMOS 0.13 µm technology.

A. Operation Modes

In Fig. 2 a temporal diagram of the three operation modes is shown. The first mode is the calibration during which any phase shift between signal S1 and S2 caused by the delay of the amplifier is minimized. To do so, the delay-locked loop (DLL) is activated by feeding a clock signal to input CTL1, shown in Fig. 1. Concurrently, control signal CTL2 is kept low in order to disconnect the antenna and avoid an additional source of phase shift between S1 and S2. During the calibration time, communication is not possible.

The second mode is the matching mode. The CTL1 input is kept low to ensure that the DLL keeps the fixed delay between S1 and S2 that results from the calibration phase. The antenna is then reconnected by toggling the control signal CTL2. The up and down counter controlling the capacitor bank is then activated by feeding a clock signal into

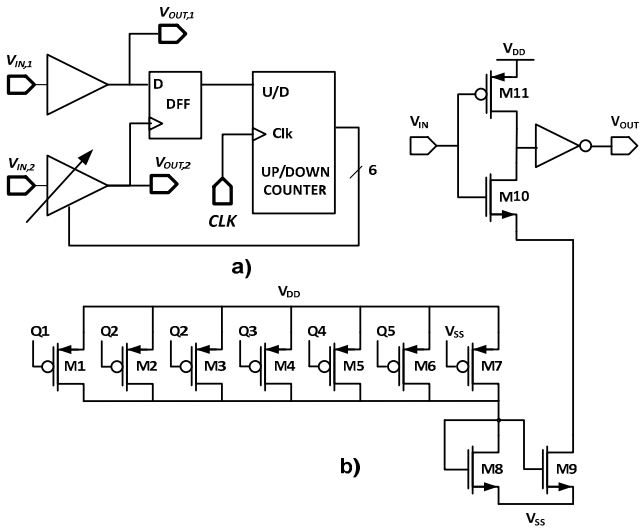

Figure 3: Diagram of the a) delay lock loop, and b) the programmable delay element.

CTL3. In matching mode, the antenna mismatch is gradually minimized by the counter action on the capacitor array.

The third mode is the operation mode. During this phase, the DLL and the up and down counter controlling the capacitor bank are deactivated and the antenna stays connected. This mode is meaningful because it can allow for a power saving, as depending on the application, the adaptive matching does not have to be undertaken continuously.

B. Delay-locked Loop

The DLL is used for calibration, i.e., to cancel out the delay induced by the amplifier. It is composed of a D flip-flop for phase detection and a digital delay element controlled by an up and down counter. Fig. 3a shows the schematic of the DLL.

The programmable delay element is presented in Fig. 3b. The amount of current flowing through inverter M10 and M11 is steered by M9 to change its delay. Transistors M1 to M7 compose a programmable voltage divider with transistor M8 while transistors M1 to M6 are connected to the counter outputs. When the counter counts up, transistors M1 to M6 are successively closed resulting in a decrease of the voltage at the gate of M9. This lets less current to flow through M9, decreasing the speed of the inverter and increasing the overall delay of the programmable delay element.

C. Matching Network

The matching network is composed of 4 binary weighted switched capacitors and an inductor L_s in parallel. The inductor centers the impedance variation range symmetrically around 50 Ω. In this fashion the circuit can efficiently correct both inductive and capacitive mismatches.

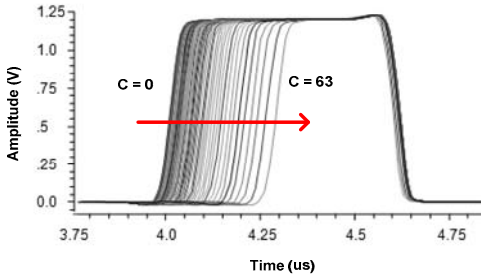

Figure 4: Time response of the programmable delay element for each counter state.

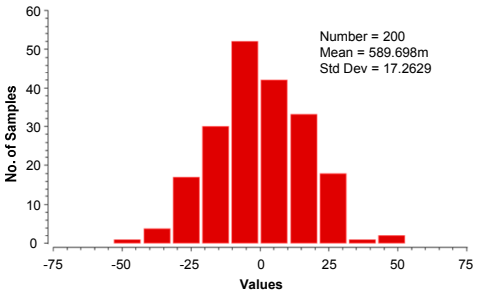

Figure 5 : Monte carlo analysis of amplifier delay

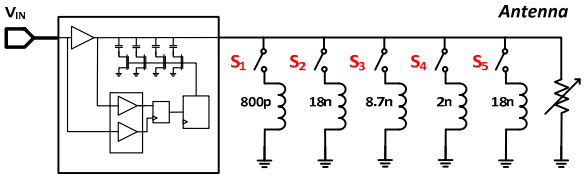

Figure 6: Test bench of the adpative tunning circuit.

III. Simulation Results

To measure the delay range reachable by the DLL temporal simulations of its output signal for each counter position were made and juxtaposed as shown in Fig. 4. When the counter increases, the delay decreases. The time difference between count 0 and count 63 is approximately 0.3 ns corresponding to a phase shift of about 97 degrees for a signal of 900 MHz frequency.

To ensure that this delay is sufficient to calibrate effectively the circuit, Monte Carlo analysis of the amplifier delay has been undertaken. Fig. 5 shows the number of samples versus the delay phase. The standard deviation is 17.3º. This value is well below the maximum achievable phase shift of the DLL. Hence, the calibration circuit is sufficiently broad in range to overcome amplifier process variations.

To test the agile matching circuit, the test bench in Fig. 6 was used. Each 20 ns, switches S1 to S5 are successively switched ON one at the time. This way, inductive loads of 800 pH, 18 nH, 8.7 nH, 2 nH and 18 nH are placed in parallel with the 50 Ω antenna model resulting in a mismatch that has to be readjusted by the adaptive matching circuit.

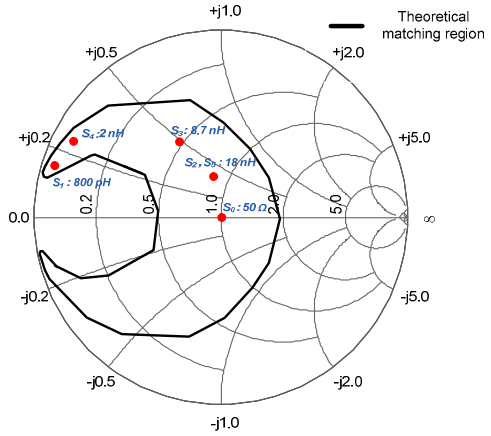

Figure 7: Theoretical matching region for which VSWR < 2.

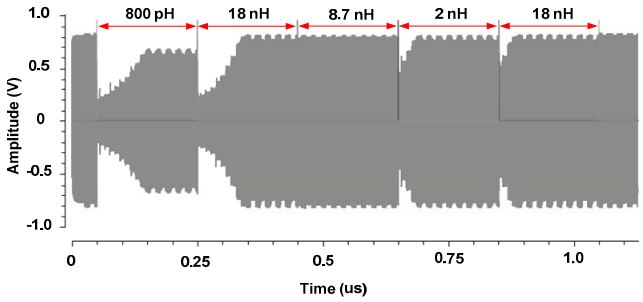

Figure 8: Temporal simulation of the circuit output signal for 5 different mismatches induced by inductances placed in parallel with the antenna.

Considering the range of the capacitor bank and the inductor used to center the matching region around 50 Ω, one can calculate a theoretical mismatch region for which the circuit can readjust the impedance and ensure a VSWR < 2. This region is presented in Fig. 7. The mismatches produced by activating switches S1 to S5 are also shown on Fig. 7.

The temporal simulation of the test bench of Fig. 6 is shown in Fig. 8. During the first 50 ns, the output impedance is equal to 50 Ω. This corresponds to the case of ideal matching. After the first 50 ns, the inductive loads are successively connected. One can see that for each inductive load, the circuit can successfully adjust the output impedance to ensure that the amplitude of the output signal is restored to almost that observed for an ideal matching. Further, in the case of a strong mismatch, especially for the first inductive load, the circuit is slightly less effective in readjusting the amplitude and requires more time. This is because, in this case, a great number of capacitors are activated to compensate the mismatch resulting in an increase of parasitics, and reduced Q-factor.

The average power consumption of the DLL using a clock with a frequency of 100 MHz is 560 µW. However, because the DLL is solely used during the calibration period occurring only when the system is turned on, its power consumption can be significantly reduced to a point where it can be ignored. The circuit having a significant impact on the overall power consumption is the control circuit which

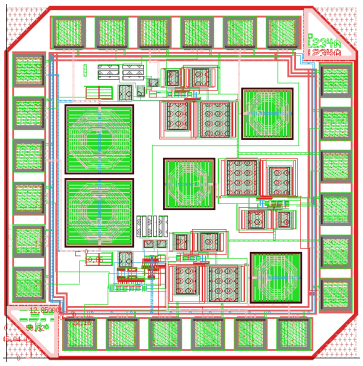

Figure 9: Layout of the integrated circuit.

includes the 4 bit counter, the phase detector and the capacitor bank. Its power consumption under power cycling condition can be calculated assuming no leakage as follows:

$$P_{eff} = P_{cc} \cdot \frac{t_a}{t_a + t_o} \quad (1)$$

where P_{eff} is the maximum effective power consumption of the control circuit, P_{cc} the average power consumption of the control circuit, t_a the maximum time needed for matching and t_o, the time of operation during which the control circuit is shut off. Considering a clock of 100 MHz, P_{cc} has a value of 532 µW. The maximum matching time can be calculated as follows:

$$t_a = 2^{nbit} \cdot \frac{1}{f_{clk}} \quad (2)$$

where, f_{clk} is the clock frequency and *nbit* is the number of bits of the counter. For a 4 bit counter and a frequency of 100 MHz t_a has a value of 160 ns. We can consider that a reasonable value of t_o can be 0.84 ms. This would mean that the matching would be undertaken every 1 ms. In this case, P_{eff}, considering this power cycling, is calculated to be 85 nW which is very low in comparison with the power that can be saved with the circuit when considering the reflected power lost. For instance, considering the 800 nH load mismatch in Fig. 8, the signal amplitude was increased during tuning from 0.2 V to 0.7 V. For a 50 Ω antenna, this corresponds to an increase in output power of 9 mW using the proposed tuning circuit.

IV. LAYOUT

The layout of the circuit shown in Fig. 9 has been sent for fabrication using CMOS 0.13 um technology. To improve the testability of the circuit, three version of different complexity levels were designed: 1) an open loop version containing solely the phase detector, the capacitor bank and its counter, which will allow to increment manually the counter controlling the capacitor bank and to measure the impedance variation achieved by the circuit, 2) a closed-loop version without the DLL, allowing to test the complete circuit while being able manually calibrate it, and 3) the complete circuit to test the overall behavior of the circuit. The size of the die comprising all three circuits is of 1 mm^2.

CONCLUSION

This paper has presented a completely integrated reference-based antenna tuning circuit. It has been shown that the circuit is effective over a wide range of impedances to adjust antenna mismatch in real-time for communication applications without the need of any external components.

The use of a reference with the circuit allows to reduce the design complexity and the power consumption. However, doing so, the circuit has to be calibrated. It has been shown that this calibration can be achieved using a DLL. Finally, the DLL is activated only for the calibration and the matching is carried out only for short repetitive periods of time. This allows a significantly reduction in the power consumption. Indeed, if the matching is undertaken every 1 ms, the average power consumption is of 85 nW.

Because the circuit is simple, low power and does not require external components while being effective and robust, it can have significant applications in the field of integrated adaptive matching networks for mobile communication applications, amongst which emerging wireless wearable sensors.

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