

A Hybrid Modulation Scheme for Dual-Output Five-Leg Indirect Matrix Converter

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Abstract—this paper proposes a hybrid modulation method for a dual-output five-leg indirect matrix converter topology. The proposed control technique combines a space vector modulation scheme (SVPWM) applied to the rectifier stage so as to control the input currents and a new digital scalar modulation scheme (DSPWM) designed to control the two loads output voltages. A generalized expression of the output voltage references is also developed showing the capability of the proposed method to control more than two independent loads without requiring additional mathematical development. Furthermore, a new modified expression of the output voltages references is proposed to enable the correct operation of the converter under unbalanced grid voltages. Also, the paper proposes a detailed mathematical analysis that allows evaluating the effect of output loads unbalances on the input current harmonic content. Simulation and experimental results are provided to show the effectiveness of the proposed theoretical investigations and confirm the capability of the proposed method to control multiple drive systems as well as ac input currents.

Index Terms— ac/ac conversion, carrier-based pulse width modulation (SPWM), dual-output converter, fault-tolerant operation, grid-connected converters, load unbalance, matrix converters, multi-drive systems, scalar modulation, space vector modulation (SVPWM), unbalanced grid voltages.

I. INTRODUCTION

MATRIX converters are ac/ac power conversion type of topologies that can provide sinusoidal input/output waveforms, unity input power factor operation, and bidirectional power flow [1] [2]. Their more important benefit over traditional ac/dc/ac power conversion topologies is the absence of electrolytic dc-bus bulky capacitors [3] [4]. The

latter is suitable to design high compact and reliable power supplies operating in hostile environment such as high temperatures and high pressures. The conventional indirect matrix converter (IMC) shown in Fig. 1 consists of a four-quadrant 12-switch rectifier stage cascaded with a two-level six-switch inverter stage [5]. This topology has some favorable characteristics compared to the direct matrix converter such as a simpler commutation scheme and a more compact clamping circuit. It also offers the possibility of reducing the power switches number in case of unidirectional power flow application [6].

In recent years, many research papers have demonstrated that this conventional IMC topology can be extended to perform independent control of more than a three-phase ac load. Such application is nowadays required in many manufacturing process such as steel, textile, and paper industries. Therefore, several new IMC topologies were proposed with the aim to reduce the cost and volume of such multi-machine drive. Note that the reduction of power semiconductors count allows saving on the number of gate drivers and other electronic circuits such as microcontroller's pwm outputs. The first alternative to the reduction of power semiconductors number is the use of more than one rear end inverter sharing the common virtual dc-link voltage produced by the front end rectifier of the IMC [7]. In this framework, a three-phase dual-output IMC that uses only one rectifier stage cascaded with a pair of three-leg inverter stages was investigated in [8] [9]. A second alternative to further reduction of switches count is to use more compact topologies. In this framework, a dual-output IMC topology with a nine-switch inverter stage has been proposed in [10]. The reduction of power semiconductors count in the nine-switch inverter stage is obtained at the cost of the switch rating which needs to be doubled. Indeed, each power semiconductor of the nine-switch inverter stage must ensure a common current path of both loads 1 and 2. The third alternative, proposes a dual-output IMC with five-leg inverter [11]. Its conceptual topology as shown in Fig. 2 consists of a rectifier stage cascaded with a five-leg inverter. Four legs of the inverter stage feed two phases of each load while the remaining two phases C_1 and C_2 are connected to a common leg of the inverter stage. As compared to the conventional dual-output IMC, the number of active switches in the inverter stage is reduced from 12 to 10. On the other hand, the switch capacity is divided by two as compared to the IMC's nine-switch inverter except the common leg, where the switches must ensure a common current path for both loads 1 and 2.

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Furthermore, it has been shown in [12] that the five-leg inverter losses are less than those of nine-switch inverter. Note that the five-leg inverter topology is well suited to two-motor constant power applications especially center-driven winders [13] [14]. On the other hand, this topology is very suitable to enable the fault-tolerant operation of a conventional two-motor drive that consists of two independent three-leg inverters stages. Indeed, one can simply eliminate the faulted leg and reconfigure the healthy legs into a five-leg inverter [15] [16].

Up to now, two modulation methods have been developed to control the dual-output five-leg indirect matrix converter [11]. The first one is based on the SVPWM technique and has not been implemented owing to its complexity. The second method is based on the carrier PWM technique where two modulation signals and one logical equation are needed to generate the switching sequences of each two transistors forming one leg of the five-leg inverter stage. Moreover, the mathematical development made to obtain the modulation signals is based on the expressions of application times that are determined by the SVPWM method. Unfortunately, the overall complexity of the SVPWM theory increases when the number of space vectors describing each set of three-phase output voltage system is more than one.

Note also that many algorithms were proposed in the recent literature to control the conventional five-leg inverter topology fed by a constant dc source such as the carrier-based PWM [13] [17], the space vector PWM [13], the scalar PWM [18], the finite state machine PWM [19], the predictive control [14] [20], etc. Obviously, these control schemes cannot be applied to modulate the input currents and output voltages of the matrix converter topology since the latter is supplied by a three-phase voltage system and not a dc source.

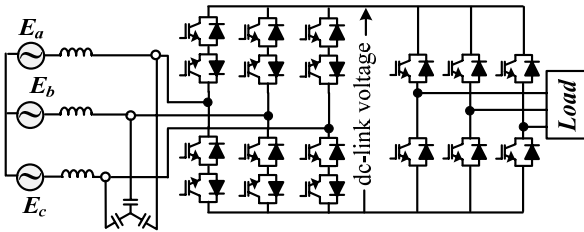


Fig. 1. Topology of a standard indirect matrix converter (IMC)

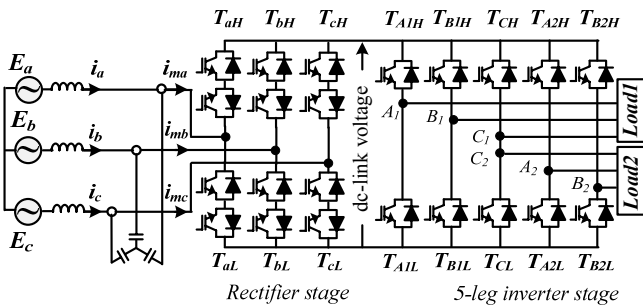


Fig. 2. Topology of a dual-output five-leg IMC

This paper proposes a new hybrid modulation method which uses the SVPWM technique to control the rectifier stage and a modified digital scalar modulation method (DSPWM) to control the five-leg inverter stage. For instance, for each leg of the converter five legs, the new algorithm computes only one modulating signal that allows the determination of the opportune duty cycles. The obtained five duty cycles are thereafter used by the DSP to generate the switching sequences of the 5-leg inverter stage; without the need of any additional logical operation. A generalized expression of the output voltage references is also given to show the capability of the proposed method to control more than two independent loads. Furthermore, a modified new expression of the output voltages references is developed to enable the correct operation of the converter under unbalanced grid voltages. Also, the paper provides a detailed mathematical development to evaluate the effect of unbalanced loads connected to the converter's output on the input current harmonic content.

This manuscript is organized as follows. Section II, describes the operation principle and pwm control method of the rectifier stage. Section III explains the proposed DSPWM method applied to the five-leg inverter stage. Section IV, provides a detailed mathematical analysis of the output loads unbalances on the input currents harmonic content. In section V, simulation and experimental results are given to show the effectiveness of the theoretical development made in this paper. Finally, some conclusions are given in section VI.

II. OPERATION PRINCIPLE AND SVPWM CONTROL TECHNIQUE OF THE RECTIFIER STAGE

The rectifier stage shown in Fig. 2, which operates in a similar manner as a four-quadrant current source rectifier, must provide sinusoidal input currents (i_{ma} , i_{mb} , and i_{mc}) with unity input displacement factor as well as a positive voltage (V_{dc}) across the virtual dc-link [1] [5]. The operation principle and modulation method explained hereafter are based on the SVPWM theory applied to conventional single-output IMC topology. The four-quadrant switching devices (T_{aH} , T_{aL} , T_{bH} , T_{bL} , T_{cH} , T_{cL}) can assume 9 switching states that can be classified into 2 groups:

- 6 active states: giving rise to 6 active currents vectors and 6 different values of the dc-link voltage (V_{dc}) as illustrated in Fig. 3. The number 1 means the top four-quadrant switch T_{xH} , of the leg x ($x = a, b, c$) is ON and the bottom T_{xL} is OFF. The opposite case is represented by the number -1. Finally, the number 0 means both switches T_{xH} , and T_{xL} , are OFF.
- 3 zero states: Both the current in the rectifier stage poles and voltage across the virtual dc-link are equal to zero. These states are not represented in Fig. 3 for clarity purpose.

Assume now that the converter is fed by a symmetrical and balanced three-phase voltage system:

$$\begin{cases} E_a = \hat{E} \cos(\omega_i t) \\ E_b = \hat{E} \cos\left(\omega_i t - \frac{2\pi}{3}\right) \\ E_c = \hat{E} \cos\left(\omega_i t - \frac{4\pi}{3}\right) \end{cases} \quad (1)$$

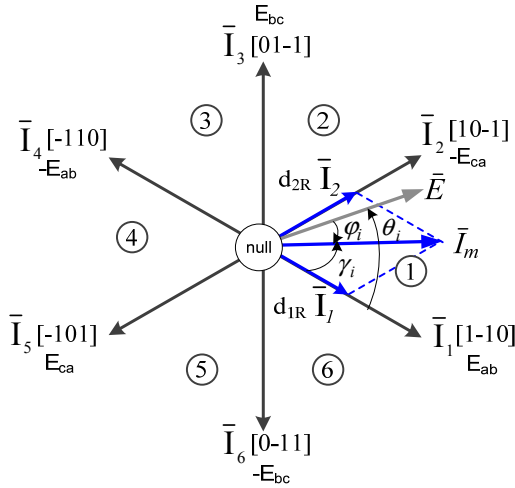


Fig. 3. SVPWM of the input current reference vector \bar{I}_m

The three-phase system of (1) can be represented by the space vector \bar{E} obtained according to the following complex transformation where \bar{X} can represent a voltage or current vector.

$$\bar{X} = \frac{2}{3} \left(X_a + X_b e^{j\frac{2\pi}{3}} + X_c e^{j\frac{4\pi}{3}} \right) \quad (2)$$

In a similar manner, the three input currents i_{ma} , i_{mb} , and i_{mc} that must be provided by the rectifier stage can be represented in the complex plane by the space vector \bar{I}_m obtained according to (2). At any sampling time, the direction of \bar{I}_m can be deduced from the position of \bar{E} in the complex plane as well as the target input displacement angle φ_i as illustrated in Fig. 3. In the example of Fig. 3, \bar{I}_m is located in sector 1 and $\gamma_i = \theta_i + \varphi_i$ is its phase angle within this sector. Therefore \bar{I}_m can be modulated by impressing the two adjacent active vectors \bar{I}_1 and \bar{I}_2 by the two duty cycles d_{1R} and d_{2R} . According to the geometrical construction of Fig. 3, one can obtain the following relationships:

$$d_{1R}|\bar{I}_1| = \sin\left(\frac{\pi}{3} - \gamma_i\right)|\bar{I}_m| \quad (3.a)$$

$$d_{2R}|\bar{I}_2| = \sin(\gamma_i)|\bar{I}_m| \quad (3.b)$$

Moreover, in order to provide the highest value of the dc-link voltage, one should use only the active vectors implying that:

$$d_{1R} + d_{2R} = 1 \quad (3.c)$$

By taking into account that the active vectors have the same amplitude ($|\bar{I}_1| = |\bar{I}_2|$), the expressions of d_{1R} and d_{2R} are derived from (3.a-b-c) as follows:

$$d_{1R} = \frac{\sin\left(\frac{\pi}{3} - \gamma_i\right)}{\cos\left(\frac{\pi}{6} - \gamma_i\right)}, \quad d_{2R} = \frac{\sin(\gamma_i)}{\cos\left(\frac{\pi}{6} - \gamma_i\right)} \quad (4.a)$$

Equation (4.a) can be generalized for the six possible positions of \bar{I}_m by substituting the term γ_i by $\bar{\gamma}_i = \gamma_i -$

$(k_i - 1)\frac{\pi}{3}$ where k_i is the operating sector of \bar{I}_m . Therefore, equation (4.a) is rewritten as:

$$d_{1R} = \frac{\sin\left(\frac{\pi}{3} - \bar{\gamma}_i\right)}{\cos\left(\frac{\pi}{6} - \bar{\gamma}_i\right)}, \quad d_{2R} = \frac{\sin(\bar{\gamma}_i)}{\cos\left(\frac{\pi}{6} - \bar{\gamma}_i\right)} \quad (4.b)$$

Note that, the unity power factor operation is achieved by modulating the input current space vector \bar{I}_m along the same direction of the grid voltage space vector \bar{E} . According to Fig.3, the input displacement angle φ_i between \bar{I}_m and \bar{E} must be set to zero which means $\gamma_i = \theta_i$ at any sampling time.

On the other hand, the example of Fig. 3 shows that two values of the virtual dc-link voltage are provided over a switching period. Indeed, the voltage V_{dc} is equal to E_{ab} during the application of the first switching state [1-10]. It becomes equal to $-E_{ca}$ during the application of the second switching state [10-1]. Therefore, the local average value of V_{dc} within a switching period is deduced as follows:

$$\langle V_{dc} \rangle = d_{1R}E_{ab} - d_{2R}E_{ca} \quad (5.a)$$

Replacing (1) and (4.b) into (5.a) yields:

$$\langle V_{dc} \rangle = \frac{3}{2} \hat{E} \frac{\cos(\varphi_i)}{\cos\left(\frac{\pi}{6} - \bar{\gamma}_i\right)} \quad (5.b)$$

It is clear that the dc-link voltage includes a low-frequency ripple term due to the variation of $\bar{\gamma}_i$ within the range $\left[-\frac{\pi}{6}, \frac{\pi}{6}\right]$. This ripple will be compensated by the proposed modulation scheme of the five-leg inverter stage as discussed in section III hereafter.

III. THE PROPOSED DSPWM TECHNIQUE APPLIED TO THE FIVE-LEG INVERTER STAGE

A. Theoretical principle of the DSPWM scheme

Define (V_{A1}, V_{B1}, V_{C1}) and (V_{A2}, V_{B2}, V_{C2}) as two normalized three-phase output voltage systems referred to the neutral points of load1 and load2 and given by:

$$\begin{cases} V_{A1} = M_1 \cos(\omega_1 t + \varphi_1) \\ V_{B1} = M_1 \cos\left(\omega_1 t - \frac{2\pi}{3} + \varphi_1\right) \\ V_{C1} = M_1 \cos\left(\omega_1 t - \frac{4\pi}{3} + \varphi_1\right) \end{cases} \quad (6.a)$$

$$\begin{cases} V_{A2} = M_2 \cos(\omega_2 t + \varphi_2) \\ V_{B2} = M_2 \cos\left(\omega_2 t - \frac{2\pi}{3} + \varphi_2\right) \\ V_{C2} = M_2 \cos\left(\omega_2 t - \frac{4\pi}{3} + \varphi_2\right) \end{cases} \quad (6.b)$$

$\omega_{i(i=1,2)}$ and $\varphi_{i(i=1,2)}$ are the angular velocities and initial phase angles of each three-phase output voltage system. $M_{i(i=1,2)}$ are the two modulation index given by (6.c) where $\hat{V}_{i(i=1,2)}$ are the maximum amplitudes of the output voltages fundamental components.

$$M_i = \frac{\hat{V}_i}{V_{dc}/2} \quad (6.c)$$

To synthesize these two three-phase voltage systems, one should obviously determine the opportune modulating signals which are referred to a virtual midpoint O in the virtual dc-link. For this purpose, define first the two normalized output voltage systems $(V_{A1o}, V_{B1o}, V_{C1o})$ and $(V_{A2o}, V_{B2o}, V_{C2o})$ referred to the virtual midpoint O. According to Fresnel construction shown in Fig. 4a, the relationship between the two aforementioned output voltage systems is derived as follows:

$$\begin{cases} V_{A1o} = V_{A1} + V_{1o} \\ V_{B1o} = V_{B1} + V_{1o} \\ V_{C1o} = V_{C1} + V_{1o} \end{cases} \quad (7.a)$$

$$\begin{cases} V_{A2o} = V_{A2} + V_{2o} \\ V_{B2o} = V_{B2} + V_{2o} \\ V_{C2o} = V_{C2} + V_{2o} \end{cases} \quad (7.b)$$

One can observe the existence of two different common mode voltages V_{1o} and V_{2o} that must be specified to determine the output voltages referred to the virtual midpoint O. For this purpose we will first determine a relationship between V_{1o} and V_{2o} . Since the output phases C_1 and C_2 share the same leg, therefore the output voltages V_{C1o} and V_{C2o} are inherently equal i.e.

$$V_{C1o} = V_{C1} + V_{1o} = V_{C2o} = V_{C2} + V_{2o} = V_{Co} \quad (8.a)$$

It is now possible to deduce from (8.a) a relationship between the two common mode voltages V_{2o} and V_{1o} such that:

$$V_{2o} = (V_{C1} - V_{C2}) + V_{1o} \quad (8.b)$$

Accordingly, all normalized output voltages given by (7.a) and (7.b) can be expressed in terms of only one common mode voltage also referred to as zero-sequence signal such that:

$$\begin{cases} V_{A1o} = V_{A1} + V_{1o} \\ V_{B1o} = V_{B1} + V_{1o} \\ V_{Co} = V_{C1} + V_{1o} \end{cases} \quad (9.a)$$

$$\begin{cases} V_{A2o} = V_{A2} + (V_{C1} - V_{C2}) + V_{1o} \\ V_{B2o} = V_{B2} + (V_{C1} - V_{C2}) + V_{1o} \end{cases} \quad (9.b)$$

Fig. 4b shows the Fresnel construction justifying the relationship given by equation (9.b).

Since the virtual dc-link voltage provided by the rectifier stage is not constant within a switching period as already reported in (5.b), therefore the normalized reference voltages given by (9.a) and (9.b) are unable to provide the two balanced output voltage systems described by (6.a) and (6.b). This constraint can be solved simply by compensating the ripple term that exists in the denominator of (5.b). Doing so, one can obtain the five modulation signals as given hereafter:

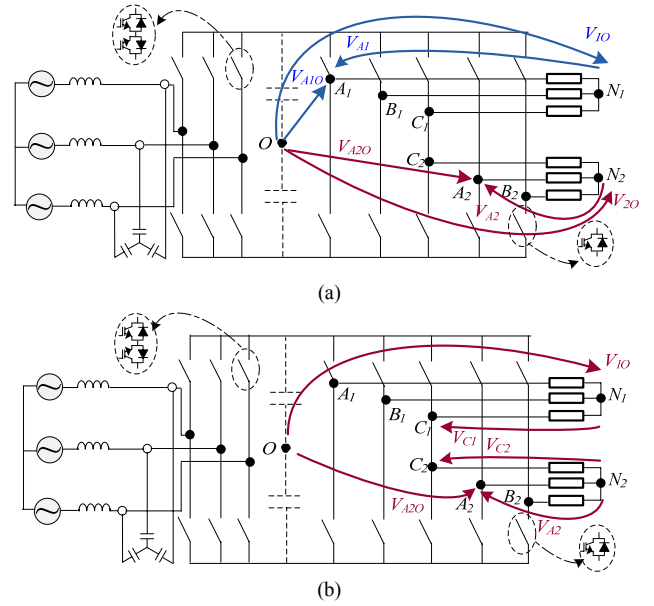


Fig. 4. (a) Fresnel construction explaining equations (7a) and (7b) – (b) Fresnel construction justifying equation (9.b)

$$\begin{cases} V_{A1o}^* = [V_{A1} + V_{1o}] \cos\left(\frac{\pi}{6} - \bar{\gamma}_i\right) \\ V_{B1o}^* = [V_{B1} + V_{1o}] \cos\left(\frac{\pi}{6} - \bar{\gamma}_i\right) \\ V_{Co}^* = [V_{C1} + V_{1o}] \cos\left(\frac{\pi}{6} - \bar{\gamma}_i\right) \end{cases} \quad (10.a)$$

$$\begin{cases} V_{A2o}^* = [V_{A2} + (V_{C1} - V_{C2}) + V_{1o}] \cos\left(\frac{\pi}{6} - \bar{\gamma}_i\right) \\ V_{B2o}^* = [V_{B2} + (V_{C1} - V_{C2}) + V_{1o}] \cos\left(\frac{\pi}{6} - \bar{\gamma}_i\right) \end{cases} \quad (10.b)$$

Therefore, one can deduce the opportune duty ratios of all upper switches forming the five-leg inverter stage (T_{A1H} , T_{B1H} , T_{CH} , T_{A2H} , and T_{B2H}) as follows:

$$d_{x(x=A1,B1,C,A2,B2)} = \frac{V_{xo}^* + 1}{2} \quad (11)$$

To avoid operation in the overmodulation region and make full use of the virtual dc-link voltage, all duty cycles d_x computed in (11) should be limited within the range $[0,1]$, leading therefore to the following constraint on the modulation signals V_{xo}^* ($x=A1,B1,C,A2,B2$)

$$-1 \leq V_{xo}^* (x=A1,B1,C,A2,B2) \leq 1 \quad (12.a)$$

Define,

$\vartheta_{max} = \max(V_{A1}, V_{B1}, V_{C1}, (V_{A2} + V_{C1} - V_{C2}), (V_{B2} + V_{C1} - V_{C2}))$ and $\vartheta_{min} = \min(V_{A1}, V_{B1}, V_{C1}, (V_{A2} + V_{C1} - V_{C2}), (V_{B2} + V_{C1} - V_{C2}))$. The relationship in (12.a) remains true if the following two conditions are fulfilled:

$$\begin{cases} \vartheta_{max} \cos\left(\frac{\pi}{6} - \bar{\gamma}_i\right) + V_{1o} \cos\left(\frac{\pi}{6} - \bar{\gamma}_i\right) < 1 \\ \vartheta_{min} \cos\left(\frac{\pi}{6} - \bar{\gamma}_i\right) + V_{1o} \cos\left(\frac{\pi}{6} - \bar{\gamma}_i\right) > -1 \end{cases} \quad (12.b)$$

The above constraints can be expressed in a generalized form using the apportioning factor μ ($0 \leq \mu \leq 1$) such that:

$$V_{1o} = \frac{(2\mu - 1)}{\cos\left(\frac{\pi}{6} - \bar{\gamma}_i\right)} - \mu \vartheta_{max} + (\mu - 1) \vartheta_{min} \quad (12.c)$$

Compared to the space vector modulation technique, μ is equivalent to the ratio $\frac{t_{v7}}{t_0}$; t_0 is the free-wheeling time interval of the five-leg inverter stage, and t_{v7} is the application time of the zero-vector V_7 where all upper switches are simultaneously ON. The particular value $\mu = \frac{1}{2}$ leads to the following well know expression of V_{1o} :

$$V_{1o} = -\frac{(\vartheta_{max} + \vartheta_{min})}{2} \quad (12.d)$$

Note that the optimized value of μ is the one that leads to an optimal performance in terms of total harmonic distortion THD of load1, load2, and grid currents. Therefore advanced optimization methods need to be utilized to solve the problem related to the above three constraints. This very interesting problematic is beyond the objective of this paper.

B. Distribution of pwm switching sequences

In section II, it is shown that for each switching period, there exist two switching states of the rectifier stage giving rise to two different voltages across the virtual dc-link of the converter. The corresponding duty ratios associated to each switching state are namely d_{1R} and d_{2R} . Therefore, the pwm switching sequences of the five-leg inverter stage must be distributed with a perfect coordination with those of the rectifier stage so as to generate balanced output voltages and input currents. This coordination can be achieved by dividing each inverter stage duty ratio d_x ($x = A_1, B_1, C, A_2, B_2$) proportionally between the two rectifier's duty ratios d_{1R} and d_{2R} as illustrated in the example given by Fig. 5 [5]. In this example, the input current reference vector is assumed to be within sector 1 of the complex plane. When the rectifier stage switches are gated so as to obtain the active vector \bar{I}_1 , the duty ratios assigned to the five-leg inverter upper switches are $d_{1R}d_x$ ($x = A_1, B_1, C, A_2, B_2$). Consequently, the duty ratios corresponding to the application of the second active vector \bar{I}_2 become $d_{2R}d_x$ ($x = A_1, B_1, C, A_2, B_2$).

Note that the commutation process of the five-leg inverter occurs in a similar manner as a conventional voltage source inverter. One can also observe that the switching sequences can be distributed freely within a sampling period to all five legs which makes this algorithm very suitable for common mode voltage CMV reduction; therefore contributing significantly to solving EMC issues. An extended study can therefore be carried out to determine the best switching pattern that optimizes the converter's CMV as well as the conducted and radiated disturbances.

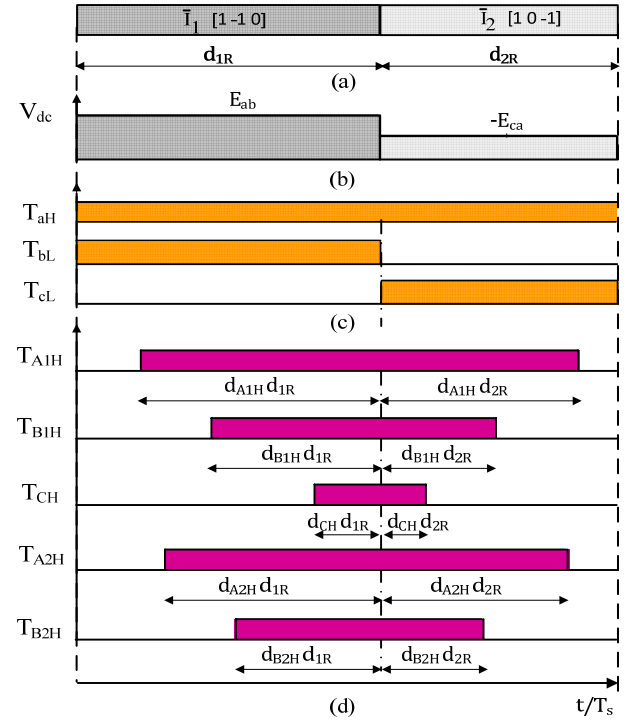


Fig. 5. PWM switching sequences (a) switching states of rectifier stage (b) dc-link voltage– (c) gating pulses of rectifier stage– (d) gating pulses of the five-leg inverter stage

C. Maximum voltage transfer ratio

In order to enable the five-leg inverter stage to operate in the linear region, the maximum amplitude of the line-to-line output voltages (\hat{V}_{line}) should never exceed the dc-link voltage [17] i.e.

$$\hat{V}_{line} \leq \langle V_{dc} \rangle \quad (13)$$

Consider as an example:

$$V_{line} = V_{B1A2} = V_{B1o} - V_{A2o} \quad (14)$$

Substituting (9.a) and (9.b) into (13) yields:

$$V_{line} = (V_{B1} - V_{C1}) + (V_{C2} - V_{A2}) \quad (15)$$

The maximum value of V_{line} (\hat{V}_{line}) is achieved when $(V_{B1} - V_{C1})$ and $(V_{C2} - V_{A2})$ are both equal to their peak values i.e.

$$\begin{cases} (V_{B1} - V_{C1}) = (V_{B1} - V_{C1})_{max} = \sqrt{3}\hat{V}_1 \\ (V_{C2} - V_{A2}) = (V_{C2} - V_{A2})_{max} = \sqrt{3}\hat{V}_2 \end{cases} \quad (16)$$

Where \hat{V}_i ($i=1,2$) are defined in (6.c). Substituting now (15) (16), and (5.b) into (13) yields:

$$\hat{V}_{line} = \sqrt{3}\hat{V}_1 + \sqrt{3}\hat{V}_2 \leq \frac{3}{2}\hat{E} \frac{\cos(\varphi_i)}{\cos\left(\frac{\pi}{6} - \bar{\gamma}_i\right)} \quad (17.a)$$

Define the two output to input voltage transfer ratios $q_1 = \frac{\hat{V}_1}{\hat{E}}$ and $q_2 = \frac{\hat{V}_2}{\hat{E}}$. Therefore, equation (17.a) can be

rewritten as follows:

$$q_1 + q_2 \leq \frac{\sqrt{3}}{2} \frac{\cos(\varphi_i)}{\cos\left(\frac{\pi}{6} - \bar{\gamma}_i\right)} \quad (17.b)$$

It is clear that the maximum values of q_1 and q_2 are obtained when the right side hand term of (17.b) is equal to its minimum value i.e. $\cos\left(\frac{\pi}{6} - \bar{\gamma}_i\right) = 1$, which yields:

$$q_{1max} + q_{2max} \leq \frac{\sqrt{3}}{2} \cos(\varphi_i) \quad (18)$$

Assume now the two output voltage systems are perfectly synchronized i.e. $\omega_1 = \omega_2$ and $\varphi_1 = \varphi_2$. Consider the same previous example. The line voltage V_{B1A2} is expressed as follows:

$$V_{line} = V_{B1A2} = \hat{V}_1 \cos\left(\omega_1 t - \frac{2\pi}{3} + \varphi_1\right) - \hat{V}_2 \cos(\omega_2 t + \varphi_2) \quad (19.a)$$

Taking into consideration, $\omega_1 = \omega_2$ and $\varphi_1 = \varphi_2$, leads to:

$$V_{line} = V_{B1A2} = \hat{V}_{line} \cos(\omega_1 t + \varphi_1 - \delta) \quad (19.b)$$

Where $\hat{V}_{line} = \sqrt{\hat{V}_1^2 + \hat{V}_2^2 + \hat{V}_1 \hat{V}_2}$ and $\delta = \tan^{-1}\left(\frac{\frac{\sqrt{3}}{2}\hat{V}_1}{-\frac{1}{2}\hat{V}_1 + \hat{V}_2}\right)$

Using the same constraint defined in (13), leads to:

$$\sqrt{\hat{V}_1^2 + \hat{V}_2^2 + \hat{V}_1 \hat{V}_2} \leq \frac{3}{2} \hat{E} \frac{\cos(\varphi_i)}{\cos\left(\frac{\pi}{6} - \bar{\gamma}_i\right)} \quad (20.a)$$

Consider the situation where $\hat{V}_2 \leq \hat{V}_1$ i.e:

$$q_2 = \frac{\hat{V}_2}{\hat{E}} \leq q_1 = \frac{\hat{V}_1}{\hat{E}} \quad (20.b)$$

Therefore, the following inequality remains true:

$$\hat{V}_{line} \leq \sqrt{\hat{V}_1^2 + \hat{V}_1^2 + \hat{V}_1 \hat{V}_1} = \sqrt{3} \hat{V}_1 \quad (20.c)$$

The inequality in (20.c) remains always true if $\sqrt{3} \hat{V}_1 \leq \frac{3}{2} \hat{E} \frac{\cos(\varphi_i)}{\cos\left(\frac{\pi}{6} - \bar{\gamma}_i\right)}$, leading to the following constraint on q_1 :

$$q_1 = \frac{\hat{V}_1}{\hat{E}} \leq \frac{\sqrt{3}}{2} \frac{\cos(\varphi_i)}{\cos\left(\frac{\pi}{6} - \bar{\gamma}_i\right)} \quad (21.a)$$

The minimum value of the right side hand term of (21.a) is achieved when $\cos\left(\frac{\pi}{6} - \bar{\gamma}_i\right) = 1$. Therefore, the condition for q_{1max} is derived from (21.a) such that:

$$q_{1max} \leq \frac{\sqrt{3}}{2} \cos(\varphi_i) \quad (21.b)$$

Considering (20.b), one can also deduce:

$$q_{2max} \leq \frac{\sqrt{3}}{2} \cos(\varphi_i) \quad (21.c)$$

Equations (21.b-c) clearly show that if the two output voltage systems are perfectly synchronized, both voltage

transfer ratios can be increased up to $\frac{\sqrt{3}}{2} \cos(\varphi_i)$. In case of unity power factor operation, we have, $q_{1max} = q_{2max} \leq \frac{\sqrt{3}}{2}$, which constitutes an advantage to this system.

D. Algorithm extension to control multiple output loads

This technique can be easily extended to control multiple output loads without requiring additional mathematical development. In fact, the modulation signals for the k^{th} load are directly derived from equation (10.b) where the subscript 2 is simply replaced by k as shown in equation (22).

$$\begin{cases} V_{Ako}^* = [V_{Ak} + (V_{C1} - V_{Ck}) + V_{1o}] \cos\left(\frac{\pi}{6} - \bar{\gamma}_i\right) \\ V_{Bko}^* = [V_{Bk} + (V_{C1} - V_{Ck}) + V_{1o}] \cos\left(\frac{\pi}{6} - \bar{\gamma}_i\right) \end{cases} \quad (22)$$

E. Algorithm extension to operate under unbalanced grid voltages

When the converter is fed by an unbalanced three-phase grid voltage system, the modulation algorithm must minimize input currents distortions and provide balanced output voltages with reduced low-order harmonics. The input current distortions can be minimized by adopting the method recommended upon the comprehensive analysis made in [21]. It consists simply in modulating the input current space vector \bar{I}_m shown in Fig. 3 along the direction of the positive sequence of the grid voltage space vector. Note also that closed-loop control methods of the input current provided by the conventional indirect matrix converter [6] remain valid with this topology. As for the control of the five-leg inverter stage, one can estimate the expression of the local average value of the dc-link voltage in a similar manner as done in [6] which yields to:

$$\langle V_{dc} \rangle = \frac{3}{2} \hat{E}^+ \frac{\left[\cos(\varphi_i) + \frac{\hat{E}^-}{\hat{E}^+} \cos(2\omega_i t + \theta^- + \varphi_i) \right]}{\cos\left(\frac{\pi}{6} - \bar{\gamma}_i\right)} \quad (23)$$

\hat{E}^+ and \hat{E}^- are the peak amplitudes of grid voltages positive and negative sequences. θ^- is the initial phase-angle of grid voltage negative sequence [6]. One can observe that an additional ripple term with frequency equal to twice of the grid appears in the expression of $\langle V_{dc} \rangle$. Accordingly, the opportune modulating signals are deduced by multiplying the normalized output voltages (9.a) and (9.b) by the inverse of the ripple term as shown in (24.a) and (24.b).

$$\begin{cases} V_{A1o}^* = \frac{[V_{A1} + V_{1o}] \cos\left(\frac{\pi}{6} - \bar{\gamma}_i\right)}{\left[\cos(\varphi_i) + \frac{\hat{E}^-}{\hat{E}^+} \cos(2\omega_i t + \theta^- + \varphi_i) \right]} \\ V_{B1o}^* = \frac{[V_{B1} + V_{1o}] \cos\left(\frac{\pi}{6} - \bar{\gamma}_i\right)}{\left[\cos(\varphi_i) + \frac{\hat{E}^-}{\hat{E}^+} \cos(2\omega_i t + \theta^- + \varphi_i) \right]} \\ V_{Co}^* = \frac{[V_{C1} + V_{1o}] \cos\left(\frac{\pi}{6} - \bar{\gamma}_i\right)}{\left[\cos(\varphi_i) + \frac{\hat{E}^-}{\hat{E}^+} \cos(2\omega_i t + \theta^- + \varphi_i) \right]} \end{cases} \quad (24.a)$$

$$\begin{cases} V_{A2o}^* = \frac{[V_{A2} + (V_{C1} - V_{C2}) + V_{1o}] \cos(\frac{\pi}{6} - \bar{\gamma}_i)}{\left[\cos(\varphi_i) + \frac{\hat{E}^-}{\hat{E}^+} \cos(2\omega_i t + \theta^- + \varphi_i) \right]} \\ V_{B2o}^* = \frac{[V_{B2} + (V_{C1} - V_{C2}) + V_{1o}] \cos(\frac{\pi}{6} - \bar{\gamma}_i)}{\left[\cos(\varphi_i) + \frac{\hat{E}^-}{\hat{E}^+} \cos(2\omega_i t + \theta^- + \varphi_i) \right]} \end{cases} \quad (24.b)$$

IV. INPUT CURRENT HARMONIC CONTENT UNDER OUTPUT LOADS UNBALANCES

To investigate the effect of unbalanced loads that could be connected to the converter's outputs on the input current signature, let us first determine a generalized expression of the instantaneous input current space vector \bar{I}_m . For this purpose, assume \bar{I}_m is modulated along the direction of an arbitrary space vector $\bar{\Psi}$ [22]. By doing some mathematical developments, quite similar to those made in [22], the expression of \bar{I}_m can therefore be deduced in terms of grid voltage space vector \bar{E} , the instantaneous output power P_o , and $\bar{\Psi}$ such that:

$$\bar{I}_m = \frac{4}{3} \frac{P_o \bar{\Psi}}{\bar{E} \bar{\Psi}^* + \bar{E}^* \bar{\Psi}} \quad (25)$$

Where, $\bar{E} = \hat{E} e^{j\omega_i t}$ is the grid voltages space vector, and the * stand for the complex conjugate operator. According to the modulation algorithm of the rectifier stage discussed in section II and the geometrical construction of Fig. 3, the space vector $\bar{\Psi}$ can be chosen as follows:

$$\bar{\Psi} = \bar{E} e^{-j\varphi_i} \quad (26)$$

Reporting (26) into (25) leads to:

$$\bar{I}_m = \frac{2}{3} \frac{P_o e^{j(\omega_i t - \varphi_i)}}{\bar{E} \cos \varphi_i} \quad (27)$$

On the other hand, the analytical expression of the instantaneous output power P_o can be computed in terms of output voltages and currents space vectors as follows:

$$P_o = \frac{3}{4} \sum_{h=1}^2 \bar{V}_h \bar{I}_{Lh}^* + \bar{V}_h^* \bar{I}_{Lh} \quad (28)$$

By neglecting the high switching frequency harmonic components of both three-phase output voltages, the latter are therefore considered perfectly sinusoidal and balanced. Their corresponding space vectors expressions are:

$$\bar{V}_1 = \hat{V}_1 e^{j(\omega_1 t + \varphi_1)} \quad (29.a)$$

$$\bar{V}_2 = \hat{V}_2 e^{j(\omega_2 t + \varphi_2)} \quad (29.b)$$

\hat{V}_h, ω_h , and φ_h ($h = 1, 2$) are the two output voltages systems peak amplitudes, angular velocities and initial phase angles respectively. The space vectors \bar{I}_{L1} and \bar{I}_{L2} of output currents demanded by unbalanced loads include therefore a positive and a negative sequence components such that:

$$\bar{I}_{L1} = \hat{I}_{L1}^+ e^{j(\omega_1 t + \varphi_{L1}^+)} + \hat{I}_{L1}^- e^{j(-\omega_1 t - \varphi_{L1}^-)} \quad (30.a)$$

$$\bar{I}_{L2} = \hat{I}_{L2}^+ e^{j(\omega_2 t + \varphi_{L2}^+)} + \hat{I}_{L2}^- e^{j(-\omega_2 t - \varphi_{L2}^-)} \quad (30.b)$$

Introducing (29a-b) and (30a-b) in (28) leads to:

$$\begin{aligned} P_o = \frac{3}{4} \sum_{h=1}^2 \hat{V}_h \hat{I}_{Lh}^+ \left[e^{j(\varphi_h - \varphi_{Lh}^+)} + e^{-j(\varphi_h - \varphi_{Lh}^+)} \right] \\ + \hat{V}_h \hat{I}_{Lh}^- \left[e^{j(2\omega_h + \varphi_h + \varphi_{Lh}^-)} + e^{-j(2\omega_h + \varphi_h + \varphi_{Lh}^-)} \right] \end{aligned} \quad (31)$$

Therefore, the instantaneous expression of the input current space vector can be deduced by replacing (31) in (27) leading to (32). Equation (32) shows that the harmonic spectrum of the input current space vector \bar{I}_m may include the following low-frequency components:

- A Fundamental component with frequency equal to ω_i , and peak amplitude equal to $\frac{\hat{V}_1 \hat{I}_{L1}^+ \cos(\varphi_1 - \varphi_{L1}^+) + \hat{V}_2 \hat{I}_{L2}^+ \cos(\varphi_2 - \varphi_{L2}^+)}{\bar{E} \cos \varphi_i}$
- 4 harmonic components with frequencies equal to $\omega_i + 2\omega_1$, $\omega_i - 2\omega_1$, $\omega_i + 2\omega_2$, and $\omega_i - 2\omega_2$. Note that for the common frequency mode of operation i.e. $\omega_1 = \omega_2$, the lower frequency harmonics caused by unbalanced loads are reduced to only two components.

It is also worth noting that the operation at unity input power factor minimizes the amplitude of the fundamental and harmonic components of the line currents resulting in reduced losses in the grid.

V. SIMULATION AND EXPERIMENTAL RESULTS

In this section, experimental results are provided showing the operation of the proposed topology and the performance of the control algorithm under balanced grid voltages. Moreover, the assessment of the line current quality in case of unbalanced output loads is performed based on simulations results. All the tests are carried out with $\mu = 0.5$

$$\bar{I}_m = \frac{1}{\bar{E} \cos \varphi_i} \left\{ \sum_{h=1}^2 \left[\hat{V}_h \hat{I}_{Lh}^+ \cos(\varphi_h - \varphi_{Lh}^+) e^{j(\omega_i t - \varphi_i)} \right] + \sum_{h=1}^2 \left[\frac{\hat{V}_h \hat{I}_{Lh}^-}{2} \left(e^{j((\omega_i + 2\omega_h)t + \varphi_h + \varphi_{Lh}^- - \varphi_i)} + e^{j((\omega_i - 2\omega_h)t - \varphi_h - \varphi_{Lh}^- - \varphi_i)} \right) \right] \right\} \quad (32)$$

A. Experimental setup

A scaled-down laboratory prototype of a dual-output five-leg indirect matrix converter was built to test the validity and performance of the proposed modulation scheme. A photo of the experimental prototype is shown in Fig. 6. Two three-phase R-L type of loads are connected to the poles of the five-leg inverter stage, while the rectifier stage is tied to the grid through a LC filter. The control algorithm including the synchronization with the grid voltages, computation of duty cycles for the rectifier stage, computation of the modulating signals and duty cycles for the five-leg inverter stage, and the distribution of the switching sequences is implemented on the DSP TMS320F28335 of Texas Instruments. The switching pulses for the 5-leg stage switching devices are provided using only the epwm modules of the DSP device without the need of additional CPLD chip to implement the additional logical operations. On the other hand, a low cost CPLD (CoolRunner-II of Xilinx) is utilized to generate the gating pulses for the rectifier stage power switches. The system parameters used for the experimental tests are listed in table I.

B. Common frequency mode

For this operating mode, both load frequencies are equal. Fig. 7 and Fig. 8a illustrate both load currents waveforms and line currents flowing through the input filter inductor. These results are obtained with $q_1 = q_2 = 0.86$, $f_1 = f_2 = 70$ Hz and $\varphi_1 = \varphi_2$. The line-to-line grid voltage peak amplitude is equal 120V. Note that the value 0.86 of q_1 and q_2 can be achieved only if the output voltages are perfectly synchronized i.e. $\varphi_2 - \varphi_1 = 0$. As can be seen the currents are balanced and also sinusoidal. Apart from the high switching frequency distortions, no low frequency harmonics can be observed in the waveforms of the load currents implying that the voltage transfer ratio can effectively reach the maximum values expected by (21b-c). Fig. 8b displays the phase-to-neutral grid voltage and the line current in the same phase. One can observe that both waveforms are in phase which emphasizes that near unity input power factor is achieved.

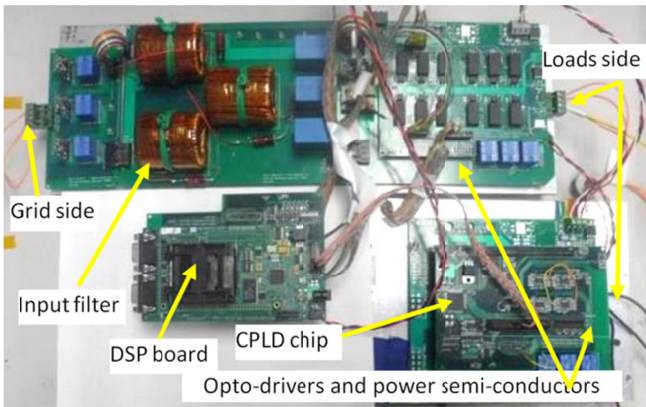


Fig. 6. Photo of the experimental prototype showing five-leg IMC

TABLE I
SYSTEM PARAMETERS FOR THE EXPERIMENTAL TEST

Parameter	Assigned value
Input filter Inductor	$L = 2$ mH
Input filter capacitor	$C = 12$ μ F
Load 1	$R_1 = 12.5 \Omega$; $L_1 = 9$ mH
Load 2	$R_2 = 25 \Omega$; $L_2 = 9$ mH
Sampling frequency	9 kHz
Switching frequency	9 kHz
Grid frequency	$f_i = 60$ Hz
Target input displacement factor	$\cos(\varphi_i) = 1$
Turn-on delay time (rectifier stage switches)	0.5 μ s
Turn-on delay time (5-leg inverter switches)	1 μ s

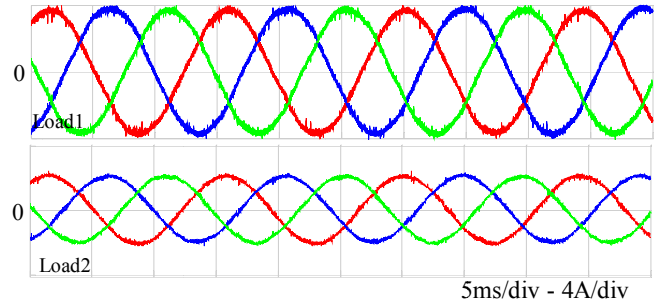


Fig. 7. Load currents obtained with $q_1 = q_2 = 0.86$, $f_1 = f_2 = 70$ Hz, and $\varphi_1 = \varphi_2$

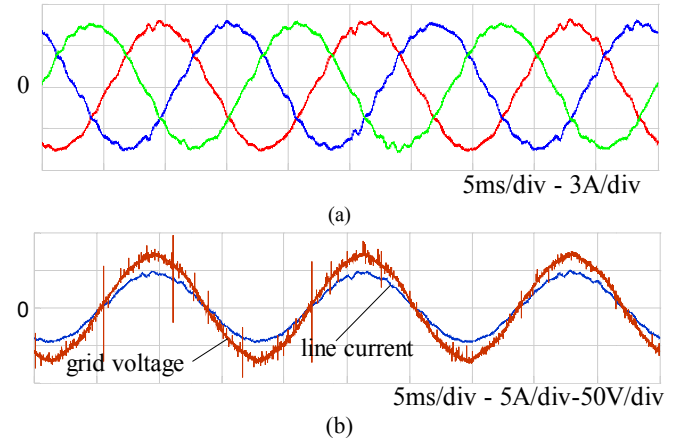


Fig. 8. (a) grid currents (b) phase-to-neutral grid voltage and line current; obtained with $q_1 = q_2 = 0.86$, $f_1 = f_2 = 70$ Hz, and $\varphi_1 = \varphi_2$

In order to assess the quality of the line currents as a function of the voltage transfer ratio, an experimental test is carried out using the open-loop V/F control. Table II depicts the obtained THDs of the line currents for several values of the voltage transfer ratios ($q_1 = q_2$) and output frequencies ($f_1 = f_2$). The results of the last two lines in table II are obtained when q_1 and q_2 are different. It is clear that the best quality of the line currents is achieved when the voltage transfer ratios are equal to their maximum values. Indeed, the obtained results show that the THD of the line current for the operating points near the nominal ratings is smaller than 5% which meets the international standards such as IEEE Std 929-2000. However, this THD increases as the voltage transfer ratio decreases implying that the quality of the line currents worsens when decreasing the active power transferred to this type of loads.

TABLE II
THD OF THE LINE CURRENTS AS A FUNCTION OF VOLTAGE TRANSFER RATIOS (q_1, q_2) AND OUTPUT FREQUENCIES (f_1, f_2)

$f_1 = f_2$ (Hz)	q_1	q_2	THD (%)
100	0.86	0.86	4.70
80	0.86	0.86	4.29
70	0.86	0.86	3.92
60	0.76	0.76	4.15
50	0.66	0.66	4.56
40	0.56	0.56	5.21
30	0.46	0.46	6.5
25	0.41	0.41	7.65
20	0.36	0.36	9.26
15	0.31	0.31	10.55
10	0.26	0.26	12.2
30	0.76	0.56	5.01
30	0.66	0.46	5.87

Fig. 9 shows the RMS values of the common leg current i_c and the line current i_a as a function of the phase shift ($\varphi_2 - \varphi_1$). Note that, the immediate consequence of common frequency mode of operation with non-synchronized load voltages ($\varphi_2 - \varphi_1 \neq 0$) is the reduction of the maximum transfer ratio such that ($q_{1max} + q_{2max}$) must be inferior to $\frac{\sqrt{3}}{2} \cos(\varphi_i)$ as concluded in (18). These results are obtained with $q_1 = q_2 = 0.43$ and $f_1 = f_2 = 50$ Hz. For this test, the line-to-line grid voltage peak amplitude is set to 145V. It is clear that RMS current in the common leg greatly depends on ($\varphi_2 - \varphi_1$). This results has already been deduced with conventional five-leg VSI fed by a dc voltage source; the maximum and minimum values of the RMS current are reached when the phase shift between the two load currents are equal to 0 and π respectively. The novelty in Fig. 9 concerns the RMS value of the line current which is almost insensitive to the phase shift ($\varphi_2 - \varphi_1$). Therefore, it can be concluded that the maximum losses in the common leg occur when ($\varphi_2 - \varphi_1$) is equal to 0; however, this phase shift has no effect on the line losses.

C. Differential frequency mode

For this operating mode, the frequencies of the two output voltages systems are different from each other. Therefore, ($q_{1max} + q_{2max}$) can never be superior to $\frac{\sqrt{3}}{2} \cos(\varphi_i)$. To check the correct operation of the proposed modulation scheme, an experimental test is carried out with $q_1 = 0.5$, $f_1 = 70$ Hz, $q_2 = 0.35$ and $f_2 = 40$ Hz. Figs.10a-b-c display the dc-link voltage, output voltages U_{A1B1} , U_{A2B2} as well as the currents flowing through both loads. One can clearly observe that apart the high switching frequency harmonics; both load currents (load1 and load2) are sinusoidal and also balanced. The harmonic spectra of i_{A1} and i_{A2} illustrated by Fig. 11 show clearly that the frequencies of their fundamental components are equal to 70 Hz and 40 Hz as target. In particular, there is no ripple at 40 Hz in the frequency spectrum of load1 current and vice versa. One can also observe the existence of very small low-order harmonics. These may be due to the ripple of the dc-link voltage caused by the pwm operation of the rectifier stage, non-ideal waveform of grid voltages, and also the non-ideal structure of power semiconductors.

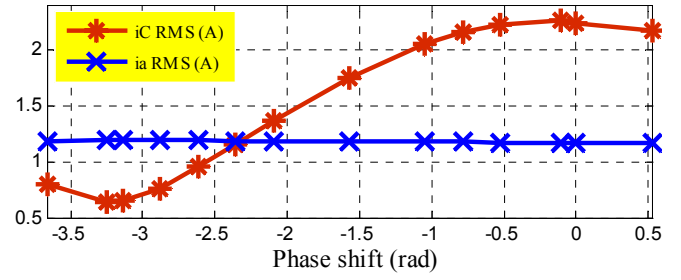


Fig. 9. RMS values of common leg current and line current versus the phase shift $\varphi_2 - \varphi_1$

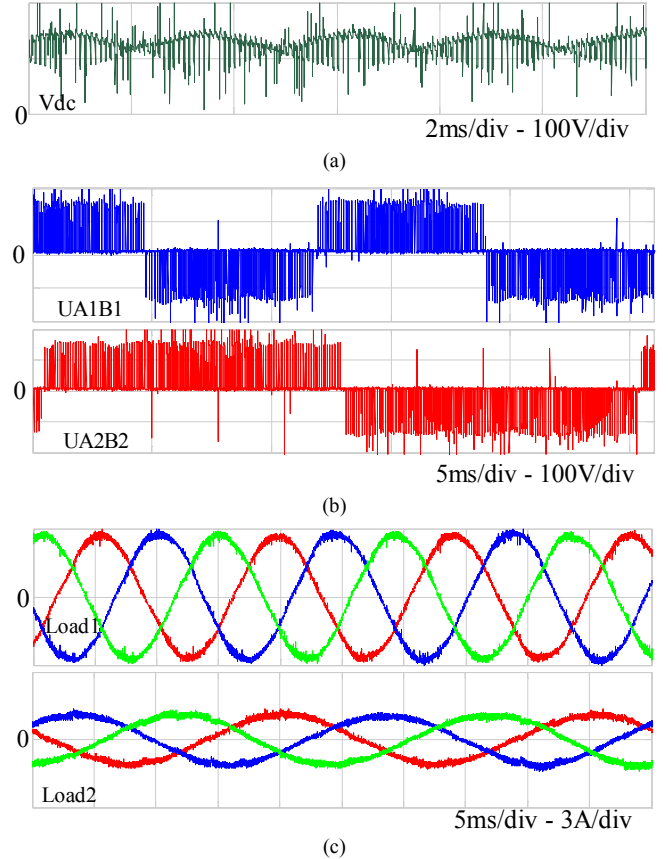


Fig.10. (a) dc-link voltage (b) output voltages U_{A1B1} , U_{A2B2} (c) Load currents. (b) and (c) are obtained with $q_1 = 0.5$, $f_1 = 70$ Hz, $q_2 = 0.35$, and $f_2 = 40$ Hz

On the other hand, Fig. 12a shows that the line currents are sinusoidal and balanced. However, one can observe more distortions as compared to the waveforms of Fig. 8a. This is due to the decrease of the fundamental component amplitude (active power) caused by the decrease of the voltage transfer ratio as already discussed in the previous section. Fig. 12b displays the phase-to-neutral grid voltage and the line current of the same phase. One can observe a little displacement angle between the line current and grid voltage for this operating point. This phenomenon is caused by the input filter that increases the input displacement angle when the active power transferred to the load is decreased. Note that the input filter elements are usually designed to achieve a near unity displacement factor at nominal power rating [23].

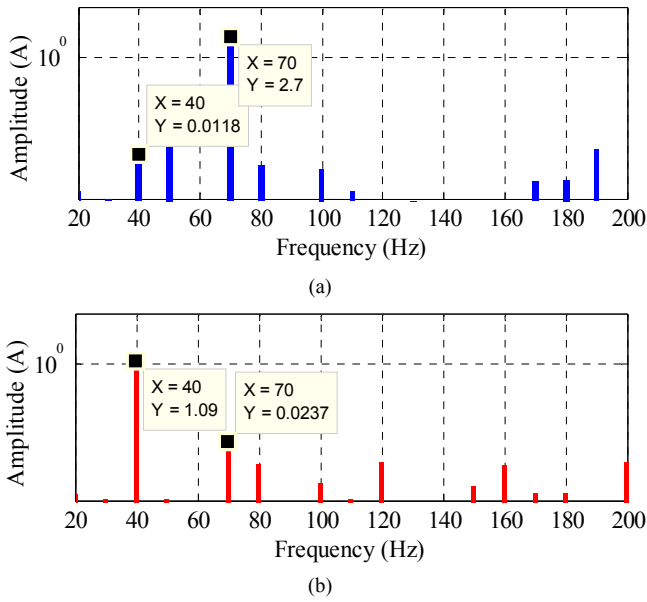


Fig. 11. Frequency spectra of loads phase a currents (a) i_{A1} - (b) i_{A2}

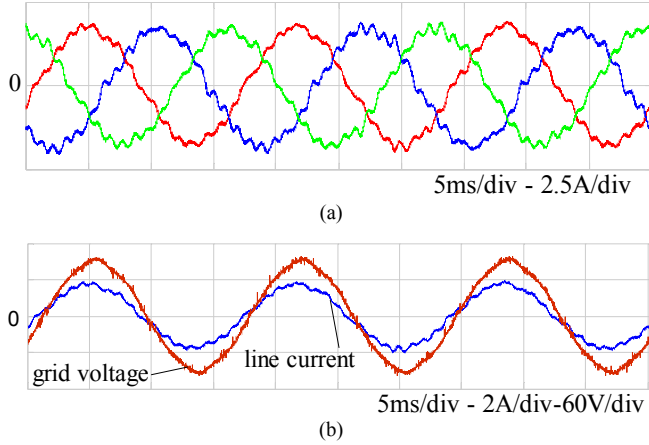


Fig. 12. (a) grid currents (b) phase-to-neutral grid voltage and line current; obtained with $q_1 = 0.5$, $f_1 = 70\text{Hz}$, $q_2 = 0.35$, and $f_2 = 40\text{Hz}$

Fig. 13 displays the line and load currents waveforms obtained for abrupt changes of q_1 , f_1 , q_2 , and f_2 , all occurred at the same time. q_1 decreases from 0.55 to 0.3 while f_1 changes from 80 to 40 Hz. q_2 increases from 0.3 to 0.55 while f_2 changes from 40 to 80 Hz. One can observe that the two load currents amplitudes and frequencies increase/decrease accordingly without fundamental component of the waveforms being deteriorated after the transient regime. As for the line current it remains sinusoidal without any effect on the frequency of the fundamental component. One can observe only a decrease of the peak amplitude due to the variation of the active power transferred to the two loads.

D. Input current harmonic content under output loads unbalances

Numerical simulations were carried out with the loads and grid parameters shown in table III. The loads impedances of phases A_1 and A_2 are both decreased by 50 %. A first test is made with a common frequency mode of operation.

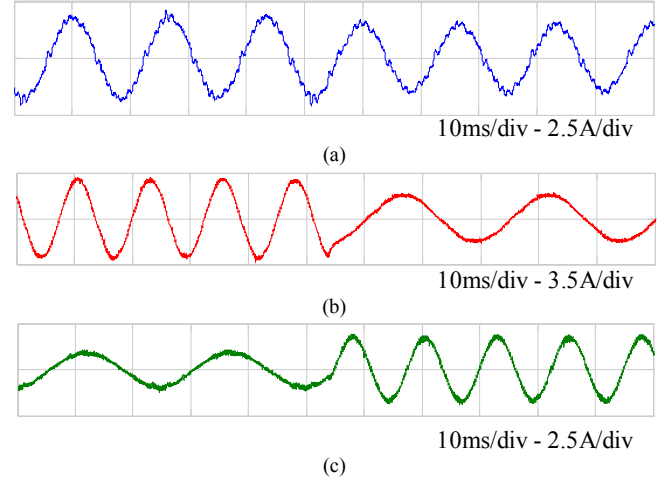


Fig. 13. Transient response to q and f changes: (a) line current (b) load1 current, and (c) load2 current

The voltage transfer ratios and output frequencies are set to $q_1 = q_2 = 0.86$, and $f_1 = f_2 = 50\text{ Hz}$. Fig. 14a displays the harmonic spectrum of the line currents. Since the waveforms of these currents are inherently periodical, therefore the fundamental and harmonic components of the space vector \bar{I}_m will appear in both, the positive and negative sides of the frequency axis. For display purpose, only the positive frequencies parts of the spectra are shown in the figures. As is possible to see in Fig. 14a, in addition to the fundamental spectral ray located at 60 Hz, there exist two dominant low-order components located at 160 Hz and 40 Hz respectively. The first frequency is equal to $\omega_i + 2\omega_1$. The second one is the positive image of $\omega_i - 2\omega_1$.

A second test is carried out with differential frequency mode of operation. The voltage transfer ratios and output frequencies are set to $q_1 = 0.43$, $q_2 = 0.43$, $f_1 = 40\text{ Hz}$, and $f_2 = 50\text{ Hz}$. The corresponding frequency spectrum of Fig. 14b shows that in addition to the fundamental component, the 4 dominant spectral rays are located at 20 Hz, 40 Hz, 140 Hz and 160 Hz. The first two frequencies (20 Hz and 40 Hz) are the positive images of $\omega_i - 2\omega_1$ and $\omega_i - 2\omega_2$. The remaining two frequencies (140 Hz and 160 Hz) are equal to $\omega_i + 2\omega_1$ and $\omega_i + 2\omega_2$ respectively. These results emphasize the existence of low-order harmonic components caused by unbalanced loads in the input current harmonic spectrum. These results are also in perfect agreement with those expected by equation (32). Unfortunately, these harmonics cannot be mitigated by the input filter, because of their low-order frequencies very close to the fundamental one, which results in additional losses and disturbances to the grid.

TABLE III
PARAMETERS USED FOR SIMULATIONS UNDER UNBALANCED LOADS

Parameter	Assigned value
Load 1	$R_1 = 12.5\Omega$; $L_1 = 9\text{ mH}$
Load 2	$R_2 = 15\Omega$; $L_2 = 9\text{ mH}$
line-to-line grid voltage amplitude	120 V
Grid frequency	$f_i = 60\text{ Hz}$
Sampling/switching frequency	10 kHz

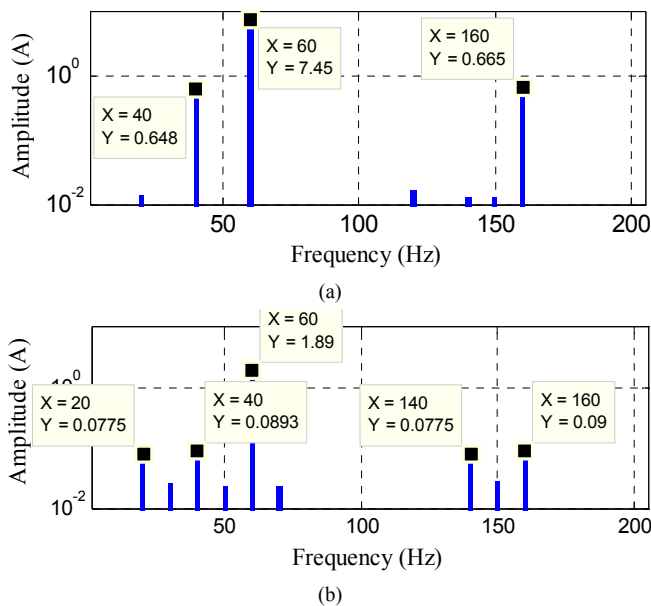


Fig. 14. Frequency spectra of load currents obtained with 50% decrease of phase A_1 load 1 and phase A_2 load 2 impedances. (a) common frequency mode of operation with $q_1 = q_2 = 0.86$ and $f_1 = f_2 = 50$ Hz; (b) differential frequency mode of operation with $q_1 = 0.43$, $q_2 = 0.43$, $f_1 = 50$ Hz and $f_2 = 40$ Hz.

VI. CONCLUSION

In this paper the authors proposed a hybrid modulation scheme implemented on a five-leg indirect matrix converter. The SVPWM technique is applied to control the rectifier stage while a DSPWM scheme was designed for the 5-leg inverter stage. A modified expression of the output voltage references was also determined to enable the correct operation of the converter under unbalanced grid voltages. It was also shown that if both output voltage systems are synchronized, both voltage transfer ratios can reach the maximum value 0.866 simultaneously.

The following advantages of this algorithm are also recorded:

- Only 5 modulation signals are needed to perform the novel proposed control of the 5-leg inverter stage.
- The algorithm can easily be extended to control more than two three-phase output loads without requiring any additional mathematical development.
- The switching sequences can be distributed freely within a sampling period, which makes this algorithm very suitable for common mode voltage CMV reduction and for solving EMC issues.

The paper investigated also some additional features of this dual-output topology. The following concluding remarks are recorded:

- The output loads unbalances give rise to 4 low-order harmonic components with frequencies equal to $\omega_i + 2\omega_1$, $\omega_i - 2\omega_1$, $\omega_i + 2\omega_2$, and $\omega_i - 2\omega_2$. These harmonics are reduced to only two components in case of common frequency mode.
- In common frequency mode of operation, the maximum losses in the common leg occur when the phase shift ($\varphi_2 -$

φ_1) is equal to 0; however, this phase shift has no effect on the line losses.

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