

Five-Level Reduced-Switch-Count Boost PFC Rectifier with Multicarrier PWM

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Abstract—A multilevel boost PFC (Power Factor Correction) rectifier is presented in this paper controlled by cascaded controller and multicarrier pulse width modulation technique. The presented topology has less active semiconductor switches compared to similar ones reducing the number of required gate drives that would shrink the manufactured box significantly. A simple controller has been implemented on the studied converter to generate a constant voltage at the output while generating a five-level voltage waveform at the input without connecting the load to the neutral point of the DC bus capacitors. Multicarrier PWM technique has been used to produce switching pulses from control signal at a fixed switching frequency. Multi-level voltage waveform harmonics has been analyzed comprehensively which affects the harmonic contents of input current and the size of required filters directly. Full experimental results confirm the good dynamic performance of the proposed five-level PFC boost rectifier in delivering power from AC grid to the DC loads while correcting the power factor at the AC side as well as reducing the current harmonics remarkably.

Index Terms—Multilevel Converter, Active Rectifier, Multicarrier PWM, Cascaded Control, Power Quality.

I. INTRODUCTION

High power factor or PFC boost converters are one of the mostly used equipment in the industries. The main concerns of such converters are the unity power factor operation and low harmonic distortion of the input AC waveforms that can be ensured by generating a DC voltage higher than the grid peak voltage amplitude, which makes use of switching devices inevitable [1-3]. Conventional two-level rectifiers known as full bridge converters have been working for many decades satisfactorily, however they are being replaced by emerging multilevel converter technologies [4].

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Multilevel converters produce more voltage levels decreasing the voltage and current harmonics significantly while operating at lower switching frequency. They are comprehensively investigated as DC-AC energy conversion mode and now they have found many applications in AC-DC power conversion systems called rectifier [5-10].

Most of the works have been performed on two-stage rectifiers in which the input AC voltage were rectified by a diode bridge and then a DC-DC chopper were used to change the DC voltage level at the second stage output. The main drawback of such system is the high switching frequency of active devices leads to high switching losses, audio noise and requiring bulky filters [11, 12]. On the other hand, active bridge rectifier could provide high power factor but the switching loss, filter size and current/voltage harmonic contents are still matters of concerns [13-16]. Considering proved advantages of multilevel converters such as low switching frequency, low harmonic distortion and high power conversion, they have been widely used in various industries [17-19]. Many multilevel rectifiers called bridgeless topologies are studied in the literature mainly including three-level ones [20-24]. Some five-level topologies have been also introduced that are using hysteresis current control or another complicated controllers that makes switching frequency higher than standard levels results in higher power losses and lower efficiency. Moreover, for medium voltage applications, high switching frequency is an important limit over choosing proper devices [25-30].

In this paper, a five-level boost PFC rectifier has been proposed using reduced number of active switches that affects the size of the manufactured box significantly [31]. On the other hand, gaining from multilevel converter advantages makes the presented rectifier appealing to use in medium-voltage high-power applications in which the switches suffer low voltage stresses and are operated at low switching frequency. Moreover, low harmonic content of the AC voltage and current would be a promising result of employing this 5-level PFC rectifier. To overcome the high switching frequency, a 4-carrier PWM technique has been adopted to modulate the reference signal and send associated switching pulses since this technique is still the most interesting method in industries. It should be noted that the reference signal is calculated by a simple cascaded controller in which two voltage and current loops are designed to regulate the output DC voltage, to make the input voltage and current in-phase and to generate 5-level voltage waveform at the rectifier input.

It should be noted that DC capacitors middle point is not connected to the load which is impossible in industrial practical applications. Full test results including change in the load, AC voltage fluctuation and generating different DC voltage values validate effective functionality of the proposed 5-level boost PFC rectifier, designed multicarrier PWM technique and simple controller in producing low ripple DC voltage at the output while drawing unity power factor and low harmonic current from the input along with operating at low and fixed switching frequency.

II. PROPOSED FIVE-LEVEL REDUCED-SWITCH RECTIFIER

Fig. 1 shows the proposed five-level boost PFC rectifier in which three active switches and six diodes have been used as a slight modification to a similar topology that includes four switches [32].

As is clear in Fig. 1, a bidirectional switch has been connected between leg b and midpoint of DC capacitors to provide different paths for current in order to produce five voltage levels at the output including $\pm V_{dc}$, $\pm V_{dc}/2$ and 0 where V_{dc} is the output DC voltage generated by the rectifier. The bidirectional switch is made by four diodes and one active switch to replace active parts with diodes. The full switching states are listed in table I along with the associate generated voltage level.

Noticing table I, it can be said that based on current direction, different voltage levels would be produced by firing necessary switches. If the current is positive, turning ON the switch S_1 leads to conducting the diode D_2 so $+V_{dc}$ will be appeared at V_{ab} and both capacitors (C_1 & C_2) are charged up. In next switching state, by firing switches S_1 and S_3 simultaneously, a low impedance current path would be provided through C_1 and bidirectional switch S_3 so the upper capacitor would be charged and V_{ab} will have the voltage level of $+V_{dc}/2$. The zero level would be generated by a short circuit between points a and b using switches S_1 and S_2 . For negative current direction, D_1 is mostly responsible to prepare required current path. Hence, by turning ON the S_3 , the current will pass through only the lower capacitor C_2 and charges it up while D_1 is conducting and the negative voltage level $-V_{dc}/2$ would be generated at the rectifier input. Finally, during negative current direction, if switch S_2 is fired, then diode D_1 conducts and V_{ab} would be equal to $-V_{dc}$. Having no redundancy switching states is the most important problem of this topology which makes the dc capacitors voltages balancing very difficult.

To prove the advantage of multilevel converters in generating lower harmonic components, some typical multilevel waveforms have been generated and analyzed by FFT. Fig. 2 demonstrates different waveforms with increasing levels and it is evident that the THD will decrease around 50% by adding one level due to making the waveform more similar to sine wave.

In a grid-connected application, the converter voltage imposes its harmonics into the current waveform. Therefore,

regarding table I, the proposed rectifier would have 5-level voltage waveform at the input so it will generate low harmonics affecting the grid current directly results in using smaller size filters compared to the conventional two-level or two-stage rectifiers. Reduced size of passive components results in light weight and cheaper manufacturing cost of the converter remarkably.

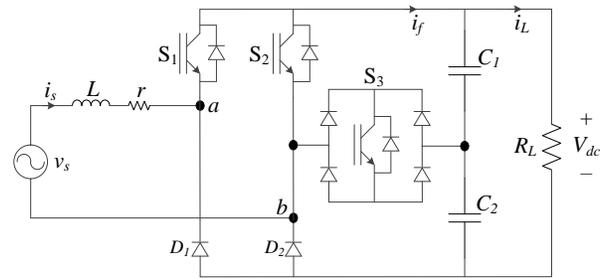


Fig. 1. Proposed five-level boost PFC rectifier with reduced number of switches

TABLE I
SWITCHING STATES AND PRODUCED VOLTAGE LEVELS OF
PROPOSED FIVE-LEVEL RECTIFIER

| Switching States | i_s | S_1 | S_2 | S_3 | V_{ab} |
|------------------|------------------------|-------|-------|-------|-------------|
| 1 | > 0 | 1 | 0 | 0 | $+V_{dc}$ |
| 2 | > 0 | 1 | 0 | 1 | $+V_{dc}/2$ |
| 3 | $\geq 0 \ \& \ \leq 0$ | 1 | 1 | 0 | 0 |
| 4 | < 0 | 0 | 0 | 1 | $-V_{dc}/2$ |
| 5 | < 0 | 0 | 1 | 0 | $-V_{dc}$ |

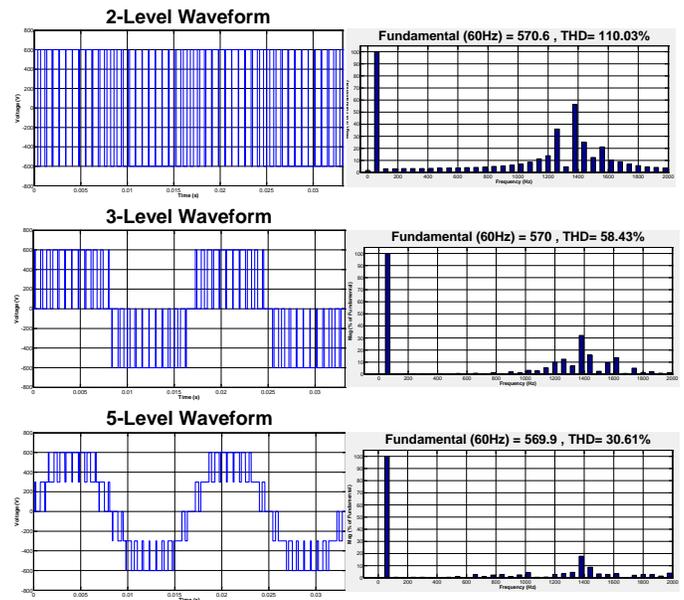


Fig. 2. Multilevel waveforms and corresponding harmonic spectrum

III. CONTROLLER AND MODULATION TECHNIQUE

A. Cascaded Control Design

Using hysteresis current control can help shaping the grid current into a sine wave but imposes switching problems such as high and variable switching frequency which makes

annoying noises and increasing power losses in the hardware implementation [32, 33]. In order to make this rectifier topology appealing and useable by industries, a simple controller including two cascaded loops have been designed in which the outer loop is voltage regulator and the inner one is the current controller. Initially, the AC line average current is modeled as shown by equation (1) [29, 31, 34, 35].

$$L \frac{di_s}{dt} = v_s - r \times i_s - V_{ab} \quad (1)$$

$$= v_s - r \times i_s - \alpha V_{dc}$$

Where, all variables can be seen in Fig. 1. L is the line inductor and r is that inductor parasitic resistance. α is the duty cycle of the rectifier. By assuming a constant value for grid voltage (v_s), and averaged value of current and duty cycle, small signal model of Eq. (1) can be converted into Laplace form as:

$$Ls i_s = -r i_s - \alpha V_{dc} \quad (2)$$

Since the inner loop should be at least 5 times faster than the outer loop, therefore the outer loop value which is the DC voltage could be considered constant. Using a reference value for DC voltage as V_{dc}^* , the following transfer function is obtained for the grid-connected rectifier inner loop giving the information that the output DC voltage, inductive filter value and line impedance affects the system AC current.

$$H_{rec.in}(s) = \frac{i_s}{\alpha} = \frac{-V_{dc}^*}{Ls + r} \quad (3)$$

Thus, the current control can be a simple gain as a proportional controller. Fig. 3 shows the inner loop of the controller.

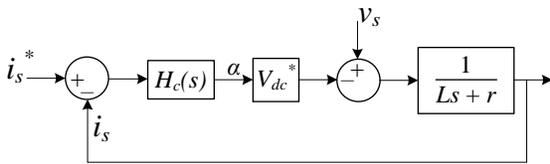


Fig. 3. Inner loop of the designed controller

The current controller $H_c(s)$ can be either a simple gain as proportional controller or a PI controller but it should be mentioned that the inner loop should have faster dynamic than the outer loop. Therefore, in case of using a PI controller for sinusoidal input current signal, the integral gain (k_{ic}) of that PI should be small enough not affecting the speed of that inner loop. However, using a PI compensator on a sinusoidal signal causes some steady-state errors which can be observed in the current harmonic spectrum as a DC component however it can do the job eventually. One alternative for such case is a proportional resonant (PR) controller that has an infinite gain at fundamental frequency (e.g. 60Hz in this work) and shows zero steady-state error [36].

In continue, to control the output DC voltage, another loop should be added to the controller which was mentioned as outer loop earlier. To obtain the system model for outer loop, equations from DC side of the rectifier should be investigated.

$$i_f = i_c + i_L$$

$$\rightarrow C \frac{dV_{dc}}{dt} = k i_s - \frac{V_{dc}}{R_L} \quad (4)$$

k is a constant average value for duty cycle and it is close to 1. i_c is the DC capacitor current (consider one capacitor C equals to $2C_1$ connected in parallel to C_1 & C_2). By small signal modelling of Eq. (4) and converting into s-plane, the following transfer function for the outer loop system would be achieved. This transfer function shows the relation between output DC voltage and the value of the load and DC capacitor.

$$H_{rec.out}(s) = \frac{V_{dc}}{i_s} = \frac{kR_L}{R_L Cs + 1} \quad (5)$$

Due to the relation between i_s and V_{dc} as Eq. (5), the voltage controller can be considered as outer loop. Such loops give the idea of cascaded controller in which the output of outer loop is an input for the inner loop.

Since the DC signal does not contain any frequency, a PI compensator with transfer function of $H_v(s)$ is used to regulate the voltage at the desired level. As shown in Fig. 4, the voltage controller loop is in charge of regulating the output DC voltage at V_{dc}^* and provides the peak value of the reference current as an input to the inner loop.

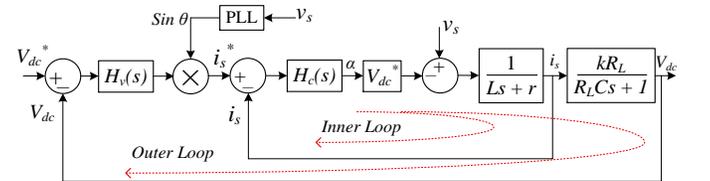


Fig. 4. Designed cascaded control block diagram applied on 5-level rectifier

Regarding Fig. 4, more details are given to derive the whole system open-loop transfer function ($H_{op}(s)$). It should be mentioned that at first the inner loop transfer function has to be calculated by multiplying the plant model and the compensator $H_c(s)$. PI controller has been chosen for the inner loop to show the detailed calculations but k_{ic} is selected small enough to have higher speed at inner loop in further analysis.

$$H_c(s) = k_{pc} + \frac{k_{ic}}{s} = \frac{k_{pc}s + k_{ic}}{s} \quad (6)$$

$$H_{in.ol}(s) = H_c(s) \times \frac{V_{dc}^*}{Ls + r} \quad (7)$$

$$= \frac{k_{pc} V_{dc}^* s + k_{ic} V_{dc}^*}{Ls^2 + rs}$$

$H_{in.ol}(s)$ demonstrates the open-loop transfer function of the inner loop controlled by the current controller of $H_c(s)$. To derive the whole system model, the closed-loop transfer function of $H_{in.ol}(s)$ should be calculated as:

$$\begin{aligned}
 H_{in.cl}(s) &= \frac{H_{in.ol}(s)}{1 + H_{in.ol}(s)} \\
 &= \frac{k_{pc}V_{dc}^*s + k_{ic}V_{dc}^*}{Ls^2 + k_{pc}V_{dc}^*s + rs + k_{ic}V_{dc}^*} \quad (8) \\
 &= \frac{k_{pc}s + k_{ic}}{\left(\frac{L}{V_{dc}^*}\right)s^2 + \left(k_{pc} + \frac{r}{V_{dc}^*}\right)s + k_{ic}}
 \end{aligned}$$

$$H_v(s) = k_{pv} + \frac{k_{iv}}{s} = \frac{k_{pv}s + k_{iv}}{s} \quad (9)$$

Equation (8) gives a transfer function of the inner system which should be compensated by a voltage controller of Eq. (9) and multiplied by the outer loop model. Thus:

$$H_{op}(s) = H_v(s) \times H_{in.cl}(s) \times H_{rec.out}(s) \quad (10)$$

Open-loop transfer function of the whole system with cascaded PI controller has been derived as Eq. (10). Using some specific gains results in simplifying the transfer function in which it can operate as a first order system with a reliable performance. Thus, the controller designer should consider all conditions and compute the gains accordingly. The controller shown in Fig. 4 can be implemented on real-time controllers due to low complexity and sufficient accuracy.

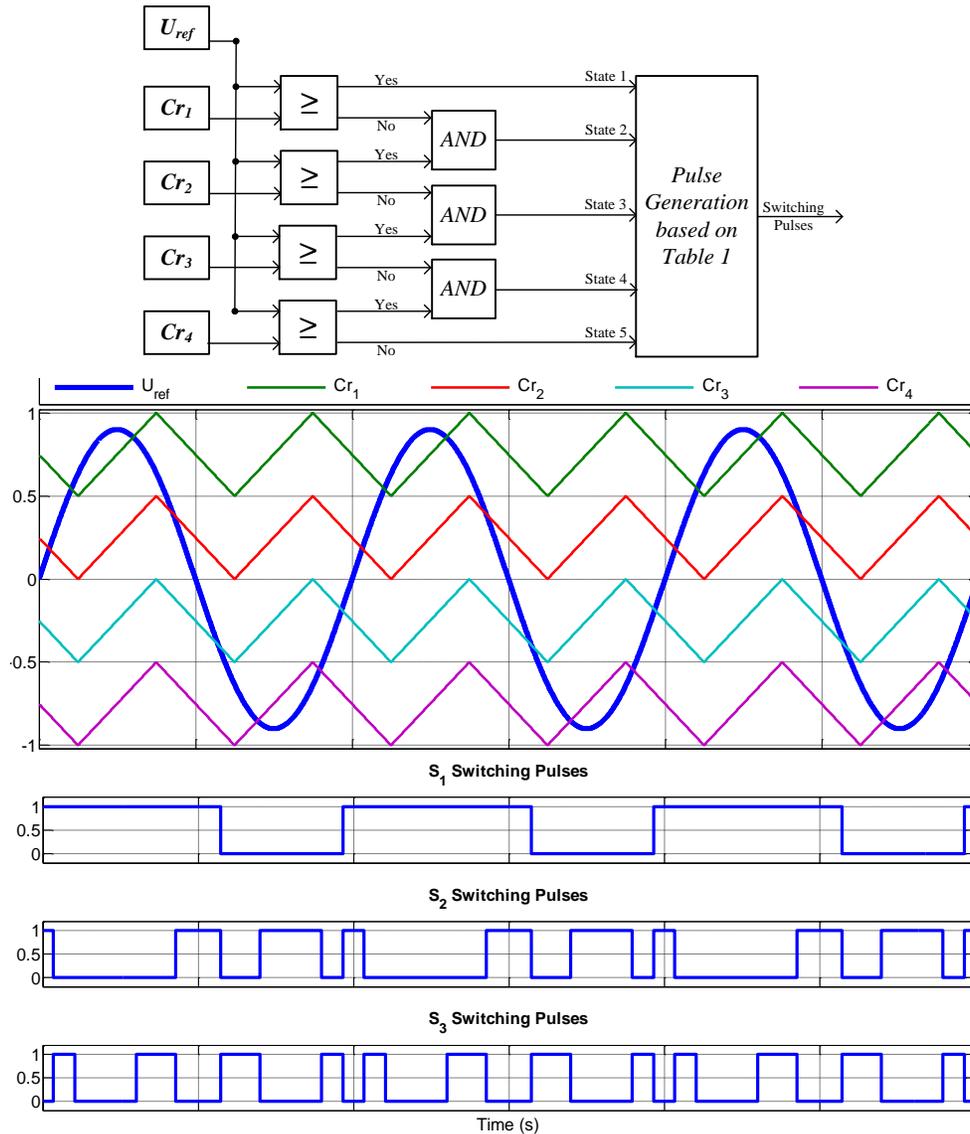


Fig. 5. proposed multicarrier PWM technique for low and fixed switching frequency purposes

B. Multicarrier PWM Technique

In order to have low and fixed switching frequency to be suitable for high power and industrial applications, the PWM method should be used to generate required switching pulses [37, 38]. It should be noted that other switching techniques like hysteresis has variable switching frequency which makes annoying audible noises. As illustrated in Fig. 5, four carriers (Cr_1 , Cr_2 , Cr_3 and Cr_4) are shifted vertically to modulate the calculated reference signal (U_{ref}). Each carrier is responsible of producing pulses for associate voltage level and switching states as shown by logic blocks. Moreover, corresponding switching pulses for three cycles of the modulated waveform (U_{ref}) have been depicted in Fig. 5 to demonstrate the fixed switching frequency in each cycle. The proposed method ensures low and fixed switching frequency functionality of the 5-level converter aims at low switching losses and high efficiency compared to other topologies.

IV. EXPERIMENTAL RESULTS

To show the good dynamic performance of the proposed rectifier as well as the implemented controller and modulation technique, it has been tested in the Lab under various conditions. The controller and switching technique have been implemented on dSpace 1103 and a sampling of $20\mu s$ has been achieved due to the simple controller algorithm.

At first the steady-state operation of the rectifier with implemented controller and switching technique has been shown in Fig. 6. The rectifier is fed from a 120V RMS grid while i_s is synchronized with v_s ensuring unity power factor mode of operation. 5-level voltage waveform at the input of the rectifier is illustrated in that figure containing low harmonic pollution which affects the grid current THD positively. 40Ω load is connected at the DC side and V_{dc} is fixed at 200V with acceptable voltage ripple around 6.9V. V_{C1} and V_{C2} have been balanced identically that made a symmetrical 5-level voltage waveform of V_{ab} with levels of 0V, $\pm 100V$ and $\pm 200V$. Grid side information including AC voltage/current waveforms, their RMS and THD% values, input active/reactive power and the power factor have been captured using AMEC power analyzer and displayed in Fig. 7. The AC current THD is almost 1.3% which is acceptably less than standard level (5%) [39]. It is also evident from Fig. 7 that the rectifier has been tested almost at 1kW power rating with the unity power factor.

In order to simulate the transient modes, different tests have been performed to verify the good dynamic performance of proposed converter with implemented controller. As shown in Fig. 8 a 50% change in the load has been made suddenly which is the most happening case in rectifier systems. Although i_s is increased due to reducing the load from 78Ω to 38Ω , the load voltage has been stabilized quickly at 200V as well as the rectifier is still working in unity power factor mode.

TABLE II
SYSTEM PARAMETERS

| | |
|--------------------------------|---------------------------|
| AC Grid Voltage | 120 V RMS |
| AC Grid Frequency | 60 Hz |
| Interface Inductor | 2.5 mH |
| DC voltages (V_{dc}) | 200 V |
| DC Capacitor (C_1 & C_2) | 1000 μF |
| DC Load (R_L) | 78Ω and 38Ω |
| Switching Frequency | 5 kHz |

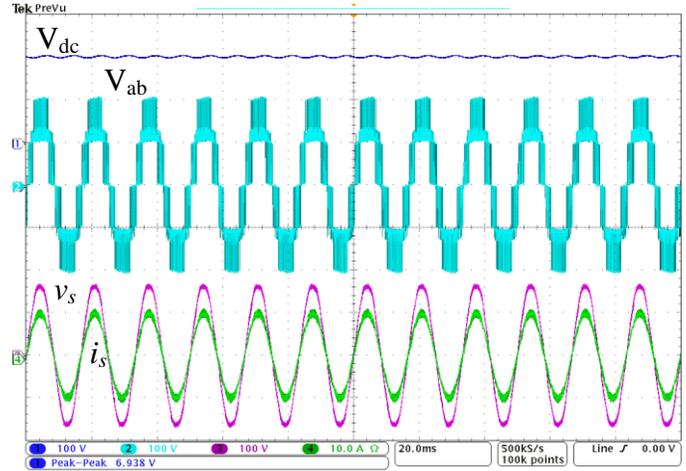


Fig. 6. Experimental results from steady-state operation of the rectifier

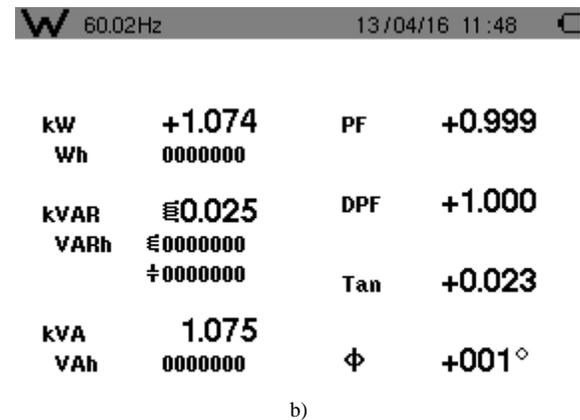
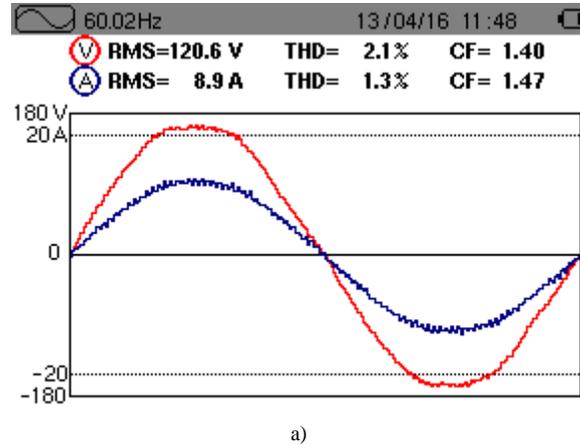


Fig. 7. a) RMS value and THD% of the grid voltage (v_s) and current (i_s)
b) power measurements at the AC grid side

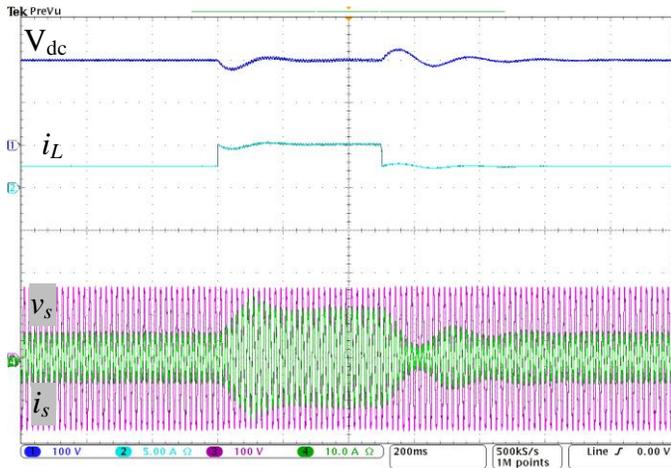


Fig. 8. Experimental results during 50% increase in the load

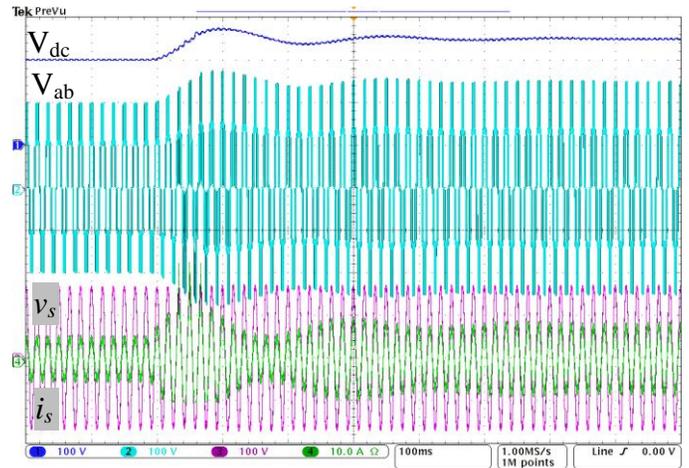


Fig. 10. Experimental results during 25% raise in the DC voltage reference

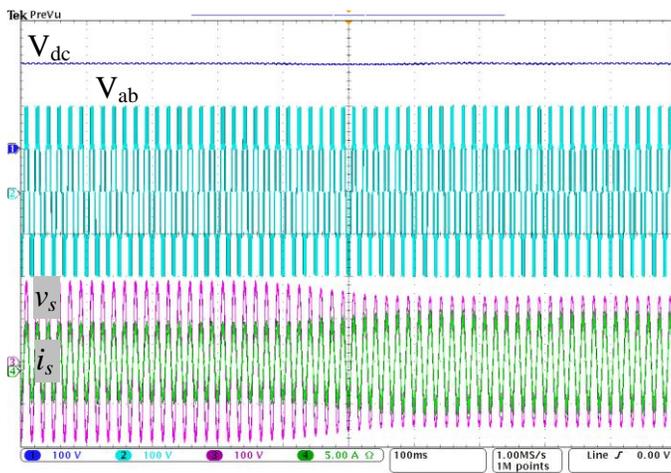


Fig. 9. Experimental results during AC source voltage variation

In another case, the input AC voltage has been changed as an unwanted problem in the utility. As illustrated in Fig. 9, the DC side power consumption ($V_{dc} \times i_L$) is not varied but v_s has been decreased, therefore i_s is increased proportional to the power delivered to the load smoothly. DC capacitors voltages have not been affected during such common voltage sag in the grid.

Eventually for the last test, the DC voltage reference (V_{dc}^*) has been increased by 25% from 200V to 250V to check the tracking performance of the controller. Results have been depicted in Fig. 10 in which all values except v_s have been increased accordingly. The controller tracked the new reference voltage value in less than 0.3s quickly.

Various conditions have been applied on the running system to investigate the dynamic performance of the proposed rectifier with implemented cascaded controller and switching technique. Low harmonic 5-level waveform of the rectifier as well as fixed switching frequency as an achievement of using multicarrier technique make this work interesting for power industries.

V. CONCLUSION

In this paper a reduced switch count 5-level boost PFC rectifier has been presented. A cascaded PI controller has been designed to regulate the output DC voltage and to ensure the unity power factor mode of the input AC voltage and current. Moreover, low harmonic AC current waveform has been achieved by the implemented controller and employing a small inductive filter at the input line. One of the main issues of switching rectifiers is the high switching frequency that has been reduced in this work using PWM technique through adopting multicarrier modulation scheme. Moreover, DC capacitors middle point has not been connected to the load that had required splitting the load to provide a neutral point. Using a single load with no neutral point makes this topology practical in real applications. Comprehensive experimental tests including change in the load, AC voltage fluctuation and generating different DC voltage values have been performed to ensure the good dynamic performance of the rectifier, adopted controller and switching technique. Moreover, the low THD of the input current has been measured to validate the advantage of multilevel waveforms in reducing harmonic contents and consequently diminishing the size of required filters at the input of the converters.

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