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Positive Envelope Feedback for Linearity Improvement in RFIC PAs

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***Abstract*—This paper introduces a dynamic biasing technique intended for Radio Frequency Integrated Circuit (RFIC) power amplifiers (PAs), using positive envelope feedback based on the instantaneous envelope signal at the output of the PA, for linearity improvement. Through the simulation, design and implementation of a 5.4 GHz SOI-CMOS PA, we demonstrate that the proposed positive envelope feedback technique allows extending the output 1 dB compression (P_{1dB}) point by 1.7 dB while meeting stability and noise requirements for a PA with P_{1dB} of 19.5 dBm. As a result, the same linearity performance is met at a higher power level, without resorting to device size increase and the associated current increase. Hence, the technique improves the efficiency/linearity trade-off. Moreover, the described technique requires negligible additional quiescent current, minimum additional chip area and has the potential for wide bandwidths, which makes it attractive for RFIC PAs.**

Keywords—Power amplifier; envelope; feedback; linearity; efficiency

I. INTRODUCTION

The instantaneous output power of RFIC PAs transmitting modulated signals may be several dBs higher than its average output power. This imposes stringent linearity/efficiency requirements over the entire range of the PA's transmitting power levels. Techniques aimed at linearity/efficiency performance improvement include Envelope Tracking (ET) [1], "ON/OFF" switching transistor matrices [2], tunable matching networks [3], and digitally-controlled PAs [4]. While these techniques yield significant performance improvement, they require the addition of sophisticated hardware that may not be fully implemented on a single RFIC PA die (e.g. supply modulators for ET and Digital Signal Processors). Hence, there is also a need for techniques that improve the efficiency/linearity trade-off, but are intended for full integration in a stand-alone, single-chip PA, and which may easily be integrated as a functional block into other PA architectures for performance enhancement.

In the latter context, techniques using dynamic biasing of the MOS transistor gate may be found in the literature. However, those reported are either dependent on the PA's *average* output power [5], require additional hardware [6], use external control signals [7] or still require extensive external signal processing [8]-[9]. Improvement in PA performances using on-chip envelope detector has also been shown [10]-[11]. These implementations rely on an approximation of the PA's output power (not the true envelope power), and hence do not account for load mismatch effects at the PA output. Input-envelope-based dynamic biasing also requires additional phase compensation [12]. Moreover, the small amplitudes of the PA's input envelope signal require using an envelope detector with high RF-Analog conversion gain followed by analog signal amplification, leading to noise degradation at the PA output.

In this paper, we introduce a PA linearization technique that does not come with the above-mentioned hardware complexity and noise issues, which is intended for full on-chip integration and which may easily be integrated into other architectures. It uses a novel *positive* envelope feedback scheme to implement dynamic biasing based on an actual signal flow from the PA's output to its bias input [13]. To the best of the authors' knowledge, positive envelope feedback has never been reported in any PA architecture. The dynamic biasing is therefore a function of the true instantaneous output envelope power. In contrast with *negative* envelope feedback (e.g. [14], [15], [16]), our approach does not require high loop gain, nor any loop stability compensation and requires only one envelope detector. This has a direct impact on noise performance and the feasibility of single-chip integration. The simplicity of the proposed technique and its feasibility for on-chip integration also facilities the possibility of using it in conjunction with other architectures that aim at enhancing RFIC PA performance [17].

Section II describes the theory for the proposed architecture. Measurement results are provided as proof of concept in Section III. Section IV gives simulation results showing possibilities for performance improvement and Section V contains the conclusion.

II. DESIGN OF DYNAMIC BIASING WITH POSITIVE ENVELOPE FEEDBACK

A. Proposed Dynamic Biasing Architecture

Fig. 1 shows the proposed PA linearization technique using positive feedback of the instantaneous output envelope for dynamic biasing. The dynamic bias signal V_{dyn} is applied to the gate of the power stage MOS transistor array in the multi-stage PA, and varies continuously as a function of the PA's true instantaneous output power. For low instantaneous output power, V_{dyn} is held at the PA's quiescent dc bias. For high instantaneous output power, an increase in the PA's output power results in a corresponding increase of V_{dyn}, which

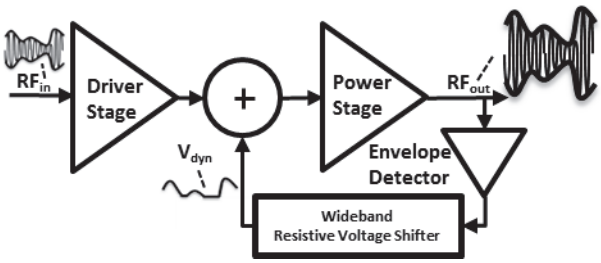

Fig. 1. Proposed PA with Positive Envelope Feedback.

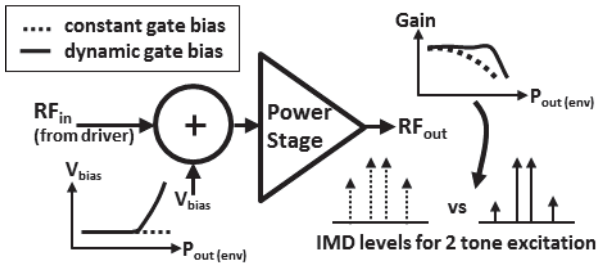

Fig. 2. Illustration of PA performances with/without dynamic gate biasing.

constitutes a positive feedback scheme. The envelope detector output is applied to a resistive voltage shifter to transform it to the required voltage values before injecting it back into the PA system as V_{dyn}. The voltage shifter is implemented using only resistors and a constant dc signal. The detector and the voltage shifter together have a wideband frequency response.

Fig. 2 illustrates the PA performance improvement sought using the proposed dynamic biasing. As the output envelope power increases, a higher value of the dynamic gate bias increases the transconductance g_m of the power stage transistors. This counteracts the PA's gain compression and allows linearizing its AM-AM response, therefore improving PA linearity. With a two-tone excitation, a decrease of the output inter-modulation (IMD) products is desired, as shown in Fig. 2. Alternately, using the proposed dynamic biasing, the same level of IMD may be met at higher output power levels. Note that under a constant biasing scheme, such performance improvement would require a higher DC gate bias and possibly larger MOS devices, which would translate into higher quiescent current consumption, therefore lower power efficiency (PAE) compared to the proposed dynamic biasing.

B. Design Criterion for Loop Gain and Loop Bandwidth

Given the well-known Nyquist stability criterion, it is generally considered that positive feedback is prone to instability. To ensure stability when using our technique, the loop gain of the positive feedback loop in Fig. 1 must remain below 0 dB at all frequencies, as per the Nyquist criterion. Accordingly, no loop compensation network is required for stability. The loop gain is composed of the conversion gain (from power stage transistor gate to PA output) and the gain through the envelope detector and resistive voltage shifter. Since the conversion gain may be high, the envelope detector is required to have an RF-Analog conversion gain that is well below 0 dB. The voltage swing typically required for the dynamic gate bias signal V_{dyn} being small (~0.1V), it allows comfortably meeting the above loop gain design criterion.

To ensure minimum delay between the PA's output signal and the dynamic bias signal, the feedback loop bandwidth in Fig. 1 has to be about five times the PA's maximum envelope frequency [11].

C. Noise Considerations

In contrast with other dynamic biasing schemes, the sub-zero dB RF-Analog conversion gain requirement for the detector in a positive envelope feedback scheme ensures that the PA noise performances is not degraded. High attenuation through the envelope detector and voltage shifter ensures that the PA's output noise is greatly attenuated before being injected back into the PA as part of the dynamic gate bias V_{dyn}.

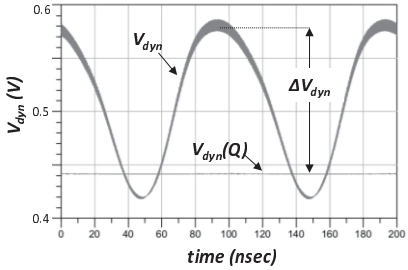

Fig. 3. Transient response of dynamic bias signal V_{dyn} (simulated in ADS™).

D. Transient Response of Dynamic Bias Signal

Fig. 3 shows the simulated transient response of the dynamic bias signal V_{dyn} when the PA in Fig. 1 is excited using a two-tone input RF signal. The curve shown corresponds to the case where the detector conversion gain is set to a high value, but that meets the stability conditions. For low PA instantaneous output power, V_{dyn} is in the vicinity of the PA's quiescent dc bias value $V_{dyn}(Q)$. When the PA's instantaneous output power increases significantly, there is a corresponding increase in the instantaneous value of the dynamic bias signal V_{dyn}. The results shown in Fig. 3 are obtained using a harmonic balance (HB) simulation of the circuit in Fig. 1, with Advanced Design System (ADS™) software by Keysight Technologies.

III. EXPERIMENTAL MEASUREMENTS

As proof of concept, measurements were carried out on a dual-IC module composed of a 5.4 GHz PA and an envelope detector. The schematic of the PA power stage and the envelope detector, as well as the prototype dual-IC module are shown in Fig. 4. The 5.4 GHz PA and the envelope detector are both fabricated using SOI-CMOS 0.18um technology from TowerJazz. The three-stage flip chip PA is interfaced to the PCB via a 6 layer multi-chip module (MCM). The envelope detector IC is a wire-bond design, and is interfaced with the PA output via a 0.5pF SMT capacitor (*C15* in Fig.4(b)). The PA die size is 2.800mm x 1.275mm, and the envelope detector die size is ~11% of the PA size. Note that a single chip integration would avoid the need for wire-bonding pads, and potentially allows the envelope detector and the resistor divider to be implemented using a much smaller chip area (estimated at about 5%). The detector's large input impedance ensures that the power loss at the PA's output is negligible. The voltage shifter is implemented using SMT resistors to allow tuning.

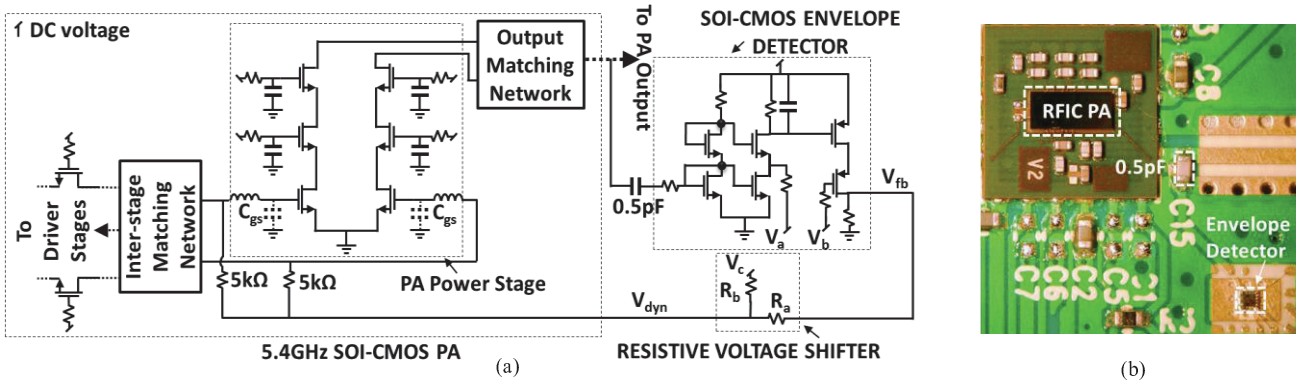

Fig. 4. (a) Simplified schematic showing PA power stage differential architecture (similar to [17, Fig. 7]), envelope detector (similar to [18]) and resistive voltage shifter in positive envelope feedback. (b) Prototype system with PA and Envelope Detector.

Design details of the circuit shown in Fig. 4(a) are given in the Appendix. Note, however, that details about the 5.4 GHz SOI-CMOS PA shown in Fig. 4(a) are not discussed. This PA design was provided by our industrial partner (Skyworks Solutions, Inc.) and providing specific PA design details (regarding component values, transistor sizes, matching circuits, etc.) is restricted due to potential future commercialization of this design. However, the PA design in Fig. 4(a) is similar to architectures discussed in [17] and the typical PA design parameters can be obtained from the designs discussed therein. Additionally, these details are not necessary here since this paper focuses on the validation of our proposed positive envelope feedback concept, which itself is independent of the specific PA design that is used.

A. Measurement Results

The total quiescent current of the system is 96mA, of which the detector consumption is only 1.2%. The detector remains biased for all the measurements. The supply voltage (V_{DD}) for the PA and the detector is 3.3V.

Fig. 5 shows the PA's AM-AM under CW excitation at 5.4 GHz in two states, i.e. with R_a in Fig. 4 open (constant gate bias) and R_a connected (dynamic gate bias). It is clear that under the same PA biasing and supply conditions, the PA's P_{1dB} is increased by 1.7 dB with the dynamic biasing. As shown in Fig. 5 for detector bias conditions that have been set experimentally, a 60mV increase of the gate bias signal V_{dyn} at P_{out}=20 dBm from its quiescent value $V_{dyn}(Q)$ at low output

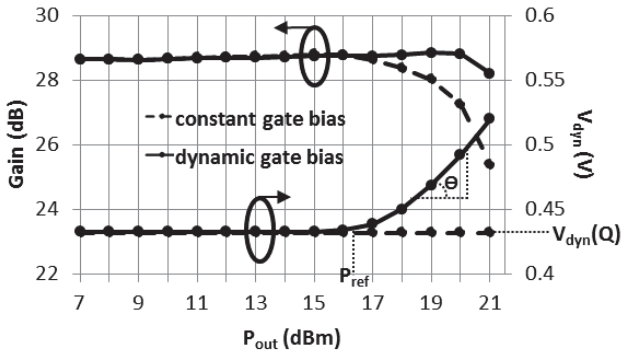

Fig. 5. *Gain vs* P_{out}, V_{dyn} *vs* P_{out} for 5.4 GHz CW excitation (V_{DD}=3.3V). The quiescent value of the V_{dyn} signal (given by $V_{dyn}(Q)$), the detector's sensitivity (defined by P_{ref}) and the detector's gain conversion slope (defined by Θ) are also indicated.

powers is adequate to sufficiently improve the PA's AM-AM. Such an increase in the gate bias is *not large enough* to cause a drastic change in the PA transistors' operation regime (such as a change from saturation to triode). Besides, the occurrence of such a drastic change in the PA transistors' operation would have translated into an excessive gain collapse and expansion in the measured *Gain vs* P_{out} response shown in Fig. 5.

Note that the swing of the V_{dyn} signal shown in Fig. 5 is a function of the detector sensitivity (defined by P_{ref} in Fig. 5), the gain conversion slope (defined by Θ in Fig. 5) and the resistive voltage shifter (implemented using resistors R_a and R_b in Fig. 4). Also, the quiescent value $V_{dyn}(Q)$ of the V_{dyn} signal is fixed using the DC voltage V_c and the resistors R_a and R_b in the resistor voltage shifter shown in Fig. 4. The values of all the components and DC voltages for implementing the SOI-CMOS

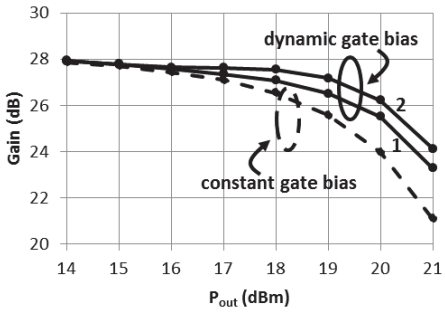

Fig. 6. Gain vs Pout for two-tone excitation at 5.4 GHz, under constant gate bias and two different Vdyn profiles (VDD=3.3V).

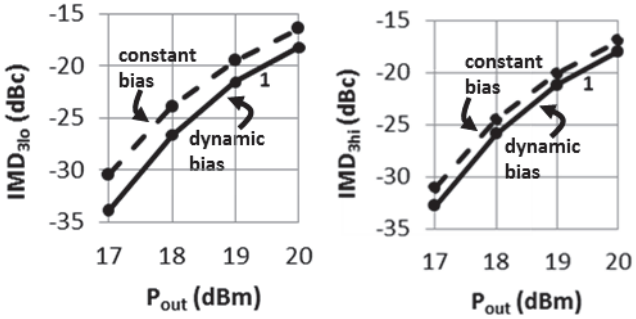

Fig. 7. IMD_3 for two-tone excitation at 5.4 GHz, under constant bias and with V_{dyn} corresponding to "1" in Fig. 6.

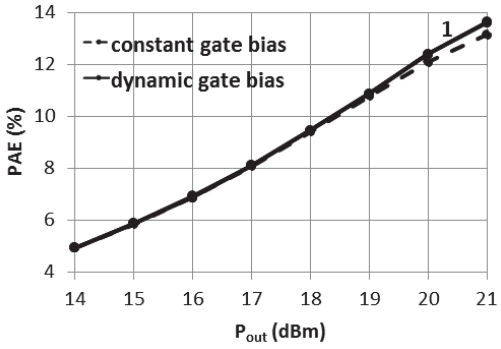

Fig. 8. PAE under constant bias and V_{dyn} corresponding to "1" in Fig. 6.

envelope detector and resistive voltage shifter shown in Fig. 4 are given in the Appendix.

Fig. 6 shows the PA's AM-AM under two-tone excitation at 5.4 GHz using 100 kHz frequency spacing in the same two states (constant gate bias and dynamic gate bias), but with two different V_{dyn} dynamic biasing profiles set by adjusting the detector sensitivity and gain conversion slope. The measurements in Fig. 7 show that the 1.7 dB increase in P_{1dB} translates into an improvement of up to 3.44 dB and 1.76 dB for IMD_{3lo} and IMD_{3hi} respectively, for P_{out} levels from 17 dBm to 20 dBm. The corresponding measurements in Fig. 8 show that there is no degradation in PAE with the dynamic biasing, but rather a slight increase that results from a Drain current reduction during the decreasing excursions of the envelope feedback signal. Although these IMD and PAE improvements are moderate for this prototype, they demonstrate that the technique improves the overall linearity/PAE performances.

B. Limitations of Measured Prototype

In this prototype, unwanted AM-PM as a function of the dynamic bias signal is introduced due to the large gate-source capacitance C_{gs} (Fig. 4) of the PA's power stage transistor, and compounded by a 5kΩ on-chip gate resistance initially required for investigations on biasing. Such AM-PM reduces the linearization effects of AM-AM compensation through the dynamic biasing. This also dictated the 100 kHz frequency spacing restriction for this proof of concept. Proper circuit techniques allow overcoming these limitations, as evidenced in Section IV.

IV. Simulations of Improved Design

Gate capacitance compensation techniques such as that described in the schematic of Fig. 3 in [19] have some inherent limitations. That is, despite the C_{gs} compensation effects within some back-off power range, there remains a sharp increase in the PA's IMD levels at output power levels above this range. As described in the analysis given in Section III of [19], this is because the PA's gain compression becomes predominant due to increased Drain current clipping for this range of higher PA output powers. Upon replacing the power stage 5kΩ gate resistors in our design (Fig. 4) with off-chip 15nH inductors to remove the R-C time-constant overloading on the dynamic biasing function, an improved AM-AM compensation over a much larger bandwidth has been obtained, as shown next.

The circuit including these 15nH inductors is simulated using the harmonic balance (HB) simulator in ADS™ software. The simulation results with a two-tone excitation at 5.4 GHz and *10 MHz* frequency spacing are shown in Fig. 9. Comparing the curves in the two states, i.e. in open loop (R_a in Fig. 4 open) and in closed loop (R_a connected and no other change), the simulation shows a significant AM-AM compensation. For output power levels higher than 21 dBm (where the PA's gain compression is predominant over the C_{gs} effects), this AM-AM compensation translates into an IMD_3 improvement of up to 3.5 dB. Obviously, more investigations are required to evaluate the full potential of the proposed positive envelope feedback concept in terms of IMD and bandwidth improvement, with respect to what is demonstrated here.

Simulations also confirm that the proposed architecture does not significantly degrade PA noise levels with respect to specifications for 5 GHz WLAN TDD systems as well as cellular FDD systems. Simulation results for the latter are shown in Table I, which show noise power levels in the Rx channel at ±20 MHz to ±50 MHz frequency offset. Under dynamic biasing, the slight degradation in noise levels at high output power is a result of the increased bias level Vdyn and consequent increase of the RF gain.

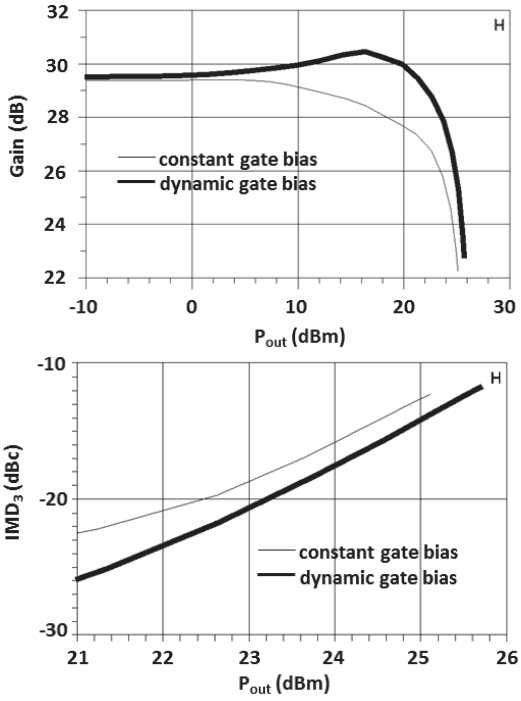

Fig. 9. Simulated AM-AM and corresponding IMD_3 *vs* P_{out} for two-tone excitation at 5.4 GHz, 10 MHz spacing and V_{DD}=3.3V.

TABLE I
Simulated Noise Power For Pout=23 dBm

BIASING TECHNIQUE	Noise Power (dBm) at ±Offset (Hz) from Carrier					
	-50 MHz	*-30 MHz*	*-20 MHz*	*+20 MHz*	*+30 MHz*	*+50 MHz*
Constant Bias	-147.2	-146.4	-145.2	-144.7	-146.0	-146.8
Dynamic Bias	-146.2	-145.3	-143.8	-143.2	-144.8	-145.8

V. Conclusion

This paper introduces a novel dynamic biasing technique for linearity improvement of RFIC PAs using positive envelope feedback based on the instantaneous envelope signal at the output of the PA. The proposed technique can be implemented with minimum additional circuitry, negligible quiescent current increase, minimum additional chip area and has the potential for wide bandwidths. The simplicity of the proposed technique makes it suitable for full on-chip integration and facilitates its integration into other existing RFIC PA architectures, as well as its use in conjunction with other state-of-the-art PA performance enhancement techniques. Simulation and measurements of an implementation of our proposed technique for a 5.4 GHz SOI-CMOS PA demonstrate the efficacy of the approach for improving the efficiency/linearity trade-off for RFIC PAs, with only a slight noise degradation.

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Appendix

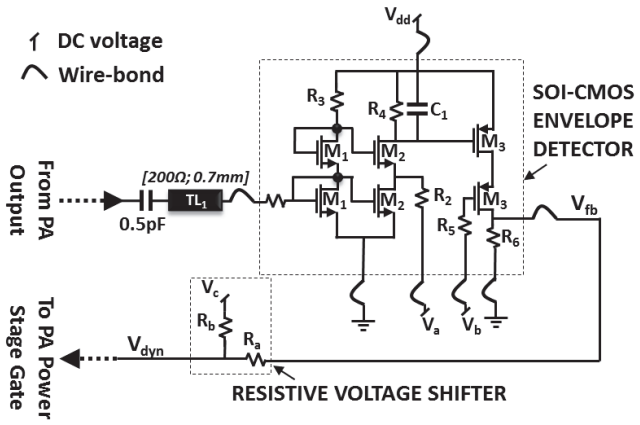

Fig. 10. Schematic of envelope detector and resistive voltage shifter (shown in Fig. 4) with labelled values for used components and DC voltages.

TABLE II
Values of Components shown in Fig. 10

Component	Value *W/L*	Component	Value
M_1	10um/0.28um	C_1	10pF
M_2	30um/0.28um	R_1	500Ω
M_3	500um/0.28um	R_2	170Ω
DC Voltage	**Value**	R_3	1.5kΩ
		R_4	750Ω
V_a	2.60V	R_5	5kΩ
V_b	1.60V	R_6	700Ω
V_c	0.55V	R_a	1.4kΩ
V_{dd}	3.30V	R_b	220Ω

References

[1] A. Zohny, J. Rascher, R. Weigel and T. Ussmueller, "A comparison of state-of-the-art efficiency enhancement techniques of fully integrated CMOS power amplifiers for handset LTE applications," *WAMICON 2013*, Orlando, FL, 2013, pp. 1-4.

[2] Bonhoon Koo, T. Joo, Y. Na and S. Hong, "A fully integrated dual-mode CMOS power amplifier for WCDMA applications," *2012 IEEE International Solid-State Circuits Conference*, San Francisco, CA, 2012, pp. 82-84.

[3] H. Hedayati et al., "A 2-GHz Highly Linear Efficient Dual-Mode BiCMOS Power Amplifier Using a Reconfigurable Matching Network," in *IEEE Journal of Solid-State Circuits*, vol. 47, no. 10, pp. 2385-2404, Oct. 2012.

[4] P. Asbeck, L. Larson, D. Kimball and J. Buckwalter, "CMOS handset power amplifiers: Directions for the future," *Proceedings of the IEEE 2012 Custom Integrated Circuits Conference*, San Jose, CA, 2012, pp. 1-6.

[5] K. W. Lau, Q. Xue and C. H. Chan, "A Novel Biasing Technique for Low Adjacent Channel Power in Microwave Power Amplifiers," *2007 Asia-Pacific Microwave Conference*, Bangkok, 2007, pp. 1-4.

[6] S. Forestier et al., "Joint optimization of the power-added efficiency and the error-vector measurement of 20-GHz pHEMT amplifier through a new dynamic bias-control method," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 52, no. 4, pp. 1132-1141, April 2004

[7] J. Nam and B. Kim, "The Doherty Power Amplifier With On-Chip Dynamic Bias Control Circuit for Handset Application," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 55, no. 4, pp. 633-642, April 2007.

[8] P. Medrel et al., "Time domain envelope characterization of power amplifiers for linear and high efficiency design solutions," *WAMICON 2013*, Orlando, FL, 2013, pp. 1-6.

[9] F. F. Tafuri, D. Sira, O. K. Jensen and T. Larsen, "Efficiency enhancement of an envelope tracking power amplifier combining supply shaping and dynamic biasing," *2013 European Microwave Conference*, Nuremberg, 2013, pp. 1491-1494.

[10] Po-Chih Wang et al., "A 2.4-GHz +25dBm P-1dB linear power amplifier with dynamic bias control in a 65-nm CMOS process," *ESSCIRC 2008 - 34th European Solid-State Circuits Conference*, Edinburgh, 2008, pp. 490-493.

[11] K. Onizuka, K. Ikeuchi, S. Saigusa and S. Otaka, "A 2.4 GHz CMOS Doherty power amplifier with dynamic biasing scheme," *2012 IEEE Asian Solid State Circuits Conference (A-SSCC)*, Kobe, 2012, pp. 93-96

[12] K. Moon et al., "Investigation of Intermodulation Distortion of Envelope Tracking Power Amplifier for Linearity Improvement," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 63, no. 4, pp. 1324-1333, April 2015.

[13] S. Sharma and N.G. Constantin, "Amplifier Architecture Using Positive Envelope Feedback", Provisional Application for Patent, 75900-50367PR; filed on 2017/01/06.

[14] S. C. Cripps, "Feedback Techniques" in *Advanced Techniques in RF Power Amplifier Design*, Norwood, MA: Artech House, 2002, pp. 111–151.

[15] N. G. Constantin, K. H. Kwok, H. Shao, C. Cismaru and P. J. Zampardi, "Formulations and a Computer-Aided Test Method for the Estimation of IMD Levels in an Envelope Feedback RFIC Power Amplifier," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 31, no. 12, pp. 1881-1893, Dec. 2012.

[16] M. Zargari, "The path towards Gb/s wireless LANs," *2012 IEEE Radio Frequency Integrated Circuits Symposium*, Montreal, QC, 2012, pp. 391-394.

[17] A. M. Niknejad, D. Chowdhury and J. Chen, "Design of CMOS Power Amplifiers," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 6, pp. 1784-1796, June 2012.

[18] F. Carrara, C. D. Presti, A. Scuderi, C. Santagati and G. Palmisano, "A Methodology for Fast VSWR Protection Implemented in a Monolithic 3-W 55% PAE RF CMOS Power Amplifier," in *IEEE Journal of Solid-State Circuits*, vol. 43, no. 9, pp. 2057-2066, Sept. 2008.

[19] Chengzhou Wang, M. Vaidyanathan and L. E. Larson, "A capacitance-compensation technique for improved linearity in CMOS class-AB power amplifiers," in *IEEE Journal of Solid-State Circuits*, vol. 39, no. 11, pp. 1927-1937, Nov. 2004.