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Packed E-Cell (PEC) Converter Topology Operation and Experimental Validation

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ABSTRACT This paper proposes a novel single-dc-source multilevel inverter called Packed E-Cell (PEC) topology to achieve nine levels with noticeably reduced components count, while dc capacitors are actively balanced. The nine-level PEC (PEC9) is composed of seven active switches and two dc capacitors that are shunted by a four-quadrant switch to from the E-cell, and it makes use of a single dc link. With the proper design of the corresponding PEC9 switching states, the dc capacitors are balanced using the redundant charging/discharging states. Since the shunted capacitors are horizontally extended, both capacitors are simultaneously charged or discharged with the redundant states, so only the auxiliary dc-link voltage needs to be sensed and regulated to half of the input dc source voltage, and consequently, dc capacitors' voltages are inherently balanced to one quarter of the dc bus voltage. To this end, an active capacitor voltage balancing integrated to the level-shifted half-parabola carrier PWM technique has been designed based on the redundant charging/discharging states to regulate the dc capacitors voltages of PEC9. Furthermore, using the E-cell not only reduces components count but also the proposed topology permits multi ac terminal operation. Thus, five-level inverter operation can be achieved during the four-quadrant switch fault, which confers to the structure high reliability. The theoretical analysis as well as the experimental results are presented and discussed, showing the basic operation, multi-functionality, as well as the superior performance of the proposed novel PEC9 inverter topology.

INDEX TERMS Nine-level Packed E-Cell (PEC), single-dc source inverter, single auxiliary dc-link capacitors, multilevel converter, PUC converter, active rectifier, active filter, grid-connected converter.

I. INTRODUCTION

Lately, Multilevel Voltage Source Inverters (MVSIs) have been emerged as a competitive power converter in various industrial applications including uninterruptible power supply, renewable energy integration, electrical drives, active power filters, etc [1], [2]. MVSIs comprise more semiconductor devices, auxiliary capacitors powered by DC sources. The latter not only produce more voltage levels but also capable of operating at high power ratio as switches endure lower voltage stress [3]. Neutral Point Clamped inverter (NPC), Flying Capacitors inverter (FC) and Cascaded H-Bridge (CHB) appeared as the first generation of MVSIs promising topologies for industry over bipolar VSIs due to EMI and dv/dt stress reduction, higher reliability and improved output voltage harmonic profile [4], [5].

Following development of MVSIs led by tremendous researches that were oriented toward new topologies mainly concentrated on increasing the number of output voltage levels [6]. As the primarily attempt and being inspired by conceptual of CHB, the hybrid structures of conventional MVSIs such as symmetrical and asymmetrical cascaded topology were utilized for HB, NPC and FC to increase the number of voltage levels and operate with higher efficiency [7]–[11]. The asymmetrical series connection of half and full bridge has been proposed in [12] for the wide variation of DC-link voltage and level doubling of the network. In [13], [14] asymmetrical cascaded of HB of NPC and conventional two-level inverters have been presented with advantages of low switching frequency operation for high voltage cell and high dynamic response. In [15] symmetrical and hybrid asymmetrical cascaded HB and NPC inverter have been compared to investigate their performance from different point of view. As well, a novel generalized circuit topology of the n-time quadrupled hybrid NPC converter and a new decomposed modulation method was proposed in [16], to multiply the number of output voltage levels of the 5L-HNPC through

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asymmetrical connection. In comparison to symmetrical cascaded MVSIs which benefit the simple circuit's topology as similar VSIs are combined, the asymmetrical ones have higher efficiency since more voltage levels are attained with less number of cells. Despite this, hybridizing the conventional MVSIs based on the symmetrical and asymmetrical cascaded connection does not optimize the final MVSIs design and it significantly increases number of components and separated DC sources and consequently manufacturing cost [15]. Recently, some novel inverter topologies have been introduced to be used as an individual cell in symmetrical and asymmetrical connections. In [17], [18] a square and an envelope T-Type module has been presented for asymmetrical MVSIs. The K-Type with two DC source has been also reported in [19] to be used as a module for multilevel structure. However, they suffer from large number of main DC source. Moreover, MVSIs with large number of DC sources are limited to PV applications particularly when they are configured in series [12], [20]. In [21]–[25] some innovative MVSIs have been proposed to produce notable number of levels as similar as sinusoidal waveform without using asymmetrical and symmetrical connections. But, they have complex structure because of the number of semiconductor devices, gate drivers, DC sources and voltage levels capacitors.

Hence, researchers have focused on establishing optimized MVSIs by making a tradeoff between number of components, voltage levels, structure complexity and replacement of DC sources by appropriate capacitors. Therefore, single-DC source multilevel inverters have been extensively investigated as a competitive and cost-effective topology over other MVSIs which are also the most suitable structure to be used in symmetrical and asymmetrical cascaded connection as each cell has only one DC source [26]–[28]. However, balancing auxiliary capacitors voltages in single-DC source inverter remains a challenge that must be considered in the design phase by providing adequate charging and discharging paths. In case of single DC source MVSIs, the compact topology has been recognized as a promising structure since the capacitor voltage balancing can be achieved in easier approach and they are much appropriate to be used as the individual cell for series connection [29]. Among the compact MVSIs, single-DC source well-known Packed U-Cell (PUC) inverter has been lately attracting lots of attention due to its advantages [30], [31]. PUC was introduced in [32], [33] as a hybrid topology combining the advantages of FC and CHB in which the U-Cell are placed in compact structure. PUC was optimally designed using six switches and one DC capacitor to achieve seven-level by adjusting the auxiliary capacitor to one third of DC input voltage, or achieving five-level output voltage while the capacitor voltage is self-balanced using redundant switching states [34]. The main complicated issue of PUC topology is capacitors voltages regulation when it is extended to employ an important number of U-Cells. Since U-Cells create individual auxiliary DC-link, capacitors are not simultaneously charging and/or discharging with the redundant states for a particular voltage level. Thus, utilization of a complex controller is inevitable to achieve the capacitor voltage balancing in the extended PUC [35]. Even in the case of external controller, as individual capacitors voltages should be adjusted to different voltage levels, separate sensors are needed to measure their voltages and consequently tuning the weighting factors of voltages regulator controllers becomes challenging.

In this paper, a novel single-DC source inverter is presented where the U-Cells are replaced by E-Cell in the packed structure; therefore, number of the auxiliary DC-link and components are reduced by horizontal extension of shunted capacitors. The proposed Packed E-Cell (PEC) inverter is a deep pivotal modification on previously introduced Packed U-Cell (PUC), which permitted to have higher capability in which two U-Cells are replaced by one E-Cell; so, not only nine voltage levels are achieved but also capacitors voltages are actively balanced by redundant switching states. As a result of using E-Cell and horizontal extension of capacitors, both DC-link capacitors are simultaneously charged or discharged with redundant states which can be effectively used to guarantee capacitors voltages regulation without need of external and complex controller. To this end, an active capacitor voltage balancing integrated into half parabola carrier has been designed to use the redundant state for capacitor voltage balancing. Moreover, only DC-link voltage needs to be regulated to half of input voltage and the capacitors voltages are inherently balanced to one quarter of main DC source voltage. Another interesting feature of PEC9 is its capability of operating during fault occurrence on four-quadrant switch as a five- or seven-level inverter depends on regulating DC-link to half or one third of the input voltage. This feature recognizes PEC as a reliable single-DC source converter as five/seven/nine-level can optimally be designed and achieved compared to other topologies. Therefore, in addition to the prominent and exclusive advantages of PEC inverter, it can also cover PUC operation and keeping its benefits because of having multi AC terminal access. The proposed Packed E-Cell inverter topology as well as the capacitors voltages balancing method integrated to the modulation technique have been filed as U.S. provisional patent application No. 62/728,734. The Packed E-Cell inverter topology and switching states are fully described in section II. Section III explains the proposed active voltage balancing algorithm integrated into PWM technique. A comparative component study on nine-level inverters is presented in section IV to prove the optimum design of PEC9. Experimental results are presented and discussed in section V meant to evaluate the capacitors active voltage balancing and converter performance under different operation conditions.

II. PROPOSED NINE-LEVEL PACKED E-CELL (PEC9)

A. PEC9 CIRCUIT TOPOLOGY

The proposed PEC9 structure is constituted by six active bidirectional current devices S1, S2, S3, S4, S5 and S6; one four-quadrant switch S7, one DC source Vdc, and two

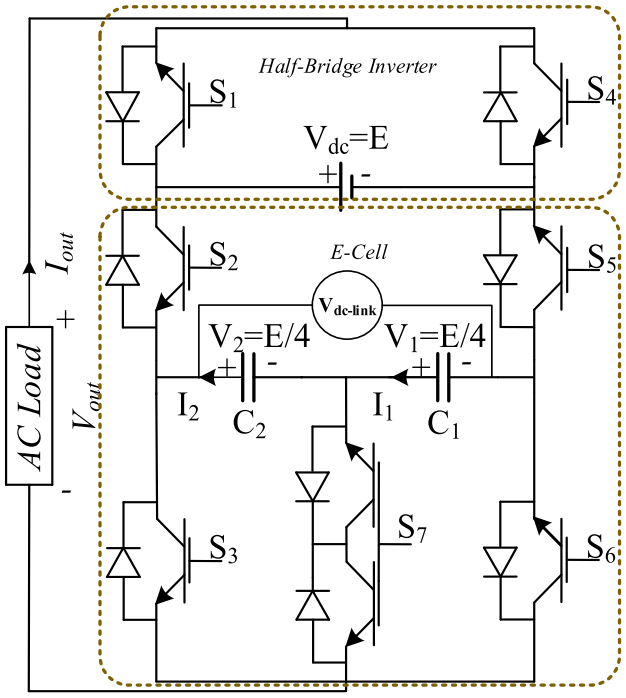

FIGURE 1. Proposed nine-level packed E-Cell (PEC9) inverter topology.

capacitors C1 and C2 to form nine-level single-phase converter topology. The designed topology is based on the idea of using E-Cell type of connection to develop the auxiliary capacitor in a row horizontal structure as depicted in Fig. 1. The four-quadrant type of switch is connected between the midpoint of two capacitors and the inverter AC terminal point. In E-Cell nine-level connection, DC capacitors are set in row to create single auxiliary DC-link that both capacitors can be charging and discharging accordingly. As a result, both capacitors are synchronized during charging or discharging with redundant states required balancing the auxiliary DC-link to inherently set the shunted capacitors voltages to the desired voltage level. E-Cell also makes multi-output voltage levels due to the four-quadrant switches that five, seven or nine-level are obtainable without changing the structure.

B. PEC9 SWITCHING STATES

With the right selection of switching states, each of C_1, C_2 capacitors voltages (V_1, V_2) is balanced to one quarter of DC input voltage (V_{dc}) so as PEC9 generates nine-level waveform. Table 1 shows switching states possibility of PEC9 inverter. Based on Table 1, switches (S_1, S_4), (S_2, S_5) as well as (S_3, S_6, S_7) are operating as complementary.

The mechanism of charging and discharging shunted capacitors C_1, C_2 depends on the load current direction. If the current flows into the capacitor from positive side, it is charging if not it is discharging. Also, the capacitor voltage does not change if it is bypassed. The states of capacitors voltages are illustrated in Table 1. They have one charging and discharging state in $\pm E/2$ as a result of horizontal extension of auxiliary DC-link. Indeed, this is one of the PEC advantages that can

TABLE 1. PEC9 Switching States (↑: Charging, ↓: Discharging, –: No effect).

State	(S_1, S_2, S_3, S_4, S_5, S_6, S_7)	I_{out}	C_1	C_2	V_{out}
1	1 0 0 0 1 1 0	> 0	–	–	V_{dc}=+E
2	1 0 0 0 1 0 1	> 0	↓	–	V_{dc}-V_1=+3E/4
3	1 0 1 0 1 0 0	> 0	↓	↓	V_{dc}-V_1-V_2=+E/2
4	1 1 0 0 0 1 0	> 0	↑	↑	V_1+V_2=+E/2
5	1 1 0 0 0 0 1	> 0	–	↑	V_2=+E/4
6	0 0 0 1 1 1 0	> 0	–	–	0
7	1 1 1 0 0 0 0	> 0	–	–	0
8	0 0 0 1 1 0 1	> 0	↓	–	-V_1=-E/4
9	0 1 0 1 0 1 0	> 0	↑	↑	-V_{dc}+V_1+V_2=-E/2
10	0 0 1 1 1 0 0	> 0	↓	↓	-V_1-V_2=-E/2
11	0 1 0 1 0 0 1	> 0	–	↑	-V_{dc}+V_2=-3E/4
12	0 1 1 1 0 0 0	> 0	–	–	V_{dc}=-E
13	1 0 0 0 1 1 0	< 0	–	–	V_{dc}=+E
14	1 0 0 0 1 0 1	< 0	↑	–	V_{dc}-V_1=+3E/4
15	1 0 1 0 1 0 0	< 0	↑	↑	V_{dc}-V_1-V_2=+E/2
16	1 1 0 0 0 1 0	< 0	↓	↓	V_1+V_2=+E/2
17	1 1 0 0 0 0 1	< 0	–	↓	V_2=+E/4
18	0 0 0 1 1 1 0	< 0	–	–	0
19	1 1 1 0 0 0 0	< 0	–	–	0
20	0 0 0 1 1 0 1	< 0	↑	–	-V_1=-E/4
21	0 1 0 1 0 1 0	< 0	↓	↓	-V_{dc}+V_1+V_2=-E/2
22	0 0 1 1 1 0 0	< 0	↑	↑	-V_1-V_2=-E/2
23	0 1 0 1 0 0 1	< 0	–	↓	-V_{dc}+V_2=-3E/4
24	0 1 1 1 0 0 0	< 0	–	–	V_{dc}=-E

provide same charging and/or discharging states for both capacitors by using the E-Cell. For output levels $\pm E/4$ *and* $\pm 3E/4$ one capacitor in charging or discharging condition, they are not affected by the switching states of the levels *0* and $\pm E$. Fig. 2 depicts the conducting paths of capacitors for the switching states of PEC9 as presented in Table 1. Note that the upper switches (S_1 & S_4) connected to the DC source are switched at low frequency. The other switches operate at the switching frequency. While two upper switches (S_1 & S_4) should withstand the DC input voltage, the auxiliary DC-link voltage that is half of the DC input across the E-Cells 6 remaining switches; so, similar lower voltage switches can be selected for high frequency part.

C. MULTI-LEVEL TERMINAL CAPABILITY OF PEC9 TOPOLOGY

As mentioned, E-Cell provides multilevel output AC terminal voltage where different number of voltage levels without changing in topology is attainable which make PEC9 a reliable configuration. For example, PEC9 can continue its operation if a fault occurs on four-quadrant switch. In this case, five or seven output voltage levels are achievable as DC-link voltage is balanced to half or one third of DC supplies input voltage. Assuming the open circuit state for four-quadrant switch during fault occurrences, the capacitors are assumed as one equivalent capacitor C_{eq} having half the value of C_1 and C_2 since they are connected in series. The DC-link voltage is regulated to half by redundant switching states for five-level inverter or to one-third using current controller to produce seven voltage levels.

III. PROPOSED PWM ACTIVE VOLTAGE BALANCING

A. E-CELL CAPACITORS VOLTAGES EQUATIONS

In order to design the voltage balancing control, the capacitors charging and discharging formulation is firstly expressed

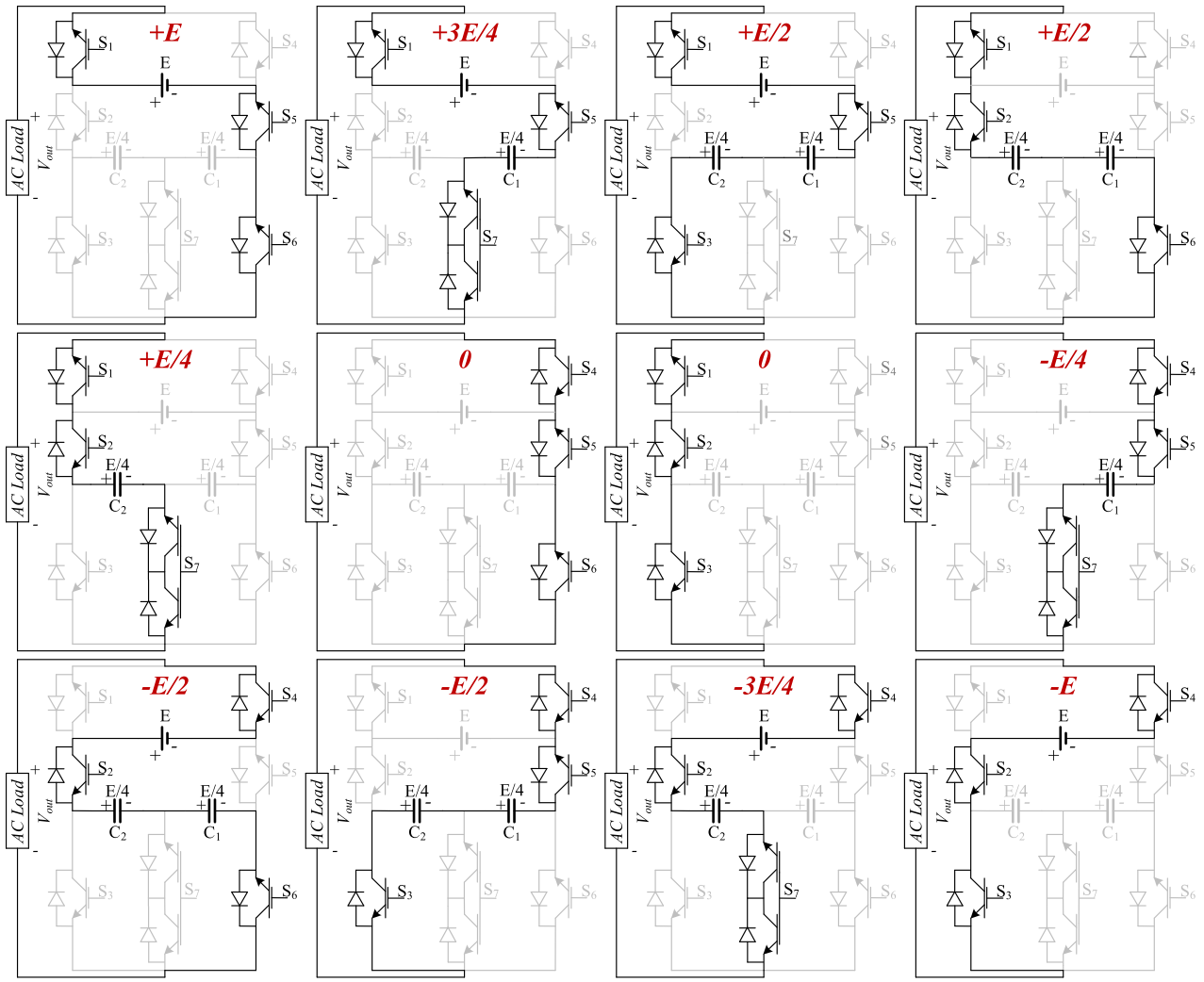

FIGURE 2. Operating sequences of PEC9 inverter showing devices, shunted capacitors and DC link connection during the 12 operating sequences forming according to the switching states possibility.

during one cycle for nine-level voltage operation. The capacitors voltages (V_1 & V_2) equations are formulized based on the output voltage (V_{out}), load current I_{out} and capacitors currents (I_1, I_2). Since load current flows into and out of the capacitors, during voltage levels ($\pm E/4$, $\pm E/2$, $\pm 3E/4$), I_{out} is then equal to I_1 and I_2 during these time intervals. Using Table 1, the capacitors charging and discharging states are shown for a predetermined nine-level waveform as it is depicted in Fig. 3. As C_1 and C_2 are forming the levels ($\pm E/2$, $+3E/2$, $-E/4$) and ($+E/4$, $\pm E/2$, $-3E/4$); then I_1 and I_2 can be obtained as follow:

$$\begin{cases} I_1(\mathrm{t}) = I_{out}(\mathrm{t}) : \begin{cases} (\alpha_2 < \mathrm{t} < \alpha_4)\&(\pi - \alpha_4 < \mathrm{t} < \pi - \alpha_2) \\ (\pi + \alpha_1 < \mathrm{t} < \pi + \alpha_3) \\ \qquad \&(2\pi - \alpha_3 < \mathrm{t} < 2\pi - \alpha_1) \end{cases} \\ I_2(\mathrm{t}) = I_{out}(\mathrm{t}) : \begin{cases} (\alpha_1 < \mathrm{t} < \alpha_3)\&(\pi - \alpha_3 < \mathrm{t} < \pi - \alpha_1) \\ (\pi + \alpha_2 < \mathrm{t} < \pi + \alpha_4) \\ \qquad \&(2\pi - \alpha_4 < \mathrm{t} < 2\pi - \alpha_2) \end{cases} \end{cases} \quad (1)$$

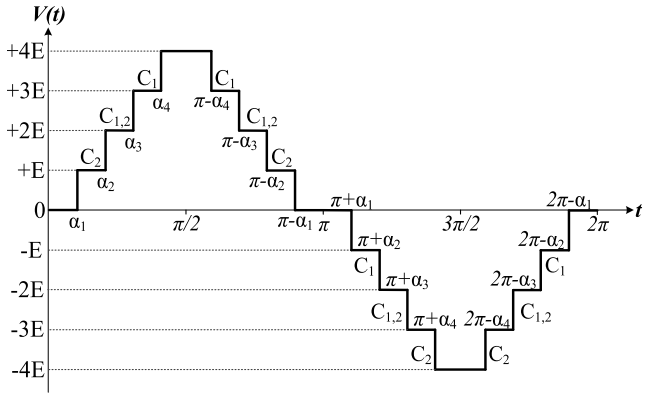

FIGURE 3. Split capacitors charging/discharging states in nine-level voltage.

Considering I_{out} is the division of the output voltage (V_{out}) and load impedance (Z) as V_{out}/Z. Where Z is considered generally as $Z{=}R{+}jL\omega$ which mean any value can

be assumed for the resistor and inductance. The angular frequency (ω) is also $\omega = 2\pi f$ and f is fundamental frequency which is assumed as *50* Hz or *60* Hz. The capacitors currents can also be computed as a function of I_{out} therefore Eq. (1) will become:

$$\begin{cases} C_1(\frac{dV_1(t)}{dt}) = \frac{V_{out}(t)}{Z} : \begin{cases} (\alpha_2 < t < \alpha_4) \& (\pi - \alpha_4 < t < \pi - \alpha_2) \\ (\pi + \alpha_1 < t < \pi + \alpha_3) \\ \qquad \& (2\pi - \alpha_3 < t < 2\pi - \alpha_1) \end{cases} \\ C_2(\frac{dV_2(t)}{dt}) = \frac{V_{out}(t)}{Z} : \begin{cases} (\alpha_1 < t < \alpha_3) \& (\pi - \alpha_3 < t < \pi - \alpha_1) \\ (\pi + \alpha_2 < t < \pi + \alpha_4) \\ \qquad \& (2\pi - \alpha_4 < t < 2\pi - \alpha_2) \end{cases} \end{cases} \tag{2}$$

Presuming the nine-level voltage of Fig. 3 as a quarter symmetry waveform, V_{out} is mathematically defined based on its harmonics amplitudes (H_n) using Fourier analysis as:

$$V_{out}(t) = \sum_{n=1}^{\infty} H_n \sin(n\omega t) \tag{3}$$

By substituting Eq. (3) into Eq. (2), the capacitors voltages are calculated by integrating Eq. (2) in time domain as Eq. (4).

$$\begin{cases} V_1 = \frac{1}{ZC_1} \int_{t_1}^{t_2} \sum_{n=1}^{\infty} (H_n \sin(n\omega t)) dt \\ V_2 = \frac{1}{ZC_2} \int_{t_1}^{t_2} \sum_{n=1}^{\infty} (H_n \sin(n\omega t)) dt \end{cases} \tag{4}$$

According to Eq. (4), both capacitors follow the same formulation and they can results in same voltage amplitude if the time duration of both integral functions are equal. Integration of the capacitors voltages V_1 and V_2 result into a constant value imposed by ripple, which should be controlled through proper switching states selections to keep both voltages convergent to the same value. To this end, the voltage ripple of both capacitors must have same value in first and second half cycles *([0,π] & [π, 2π])*, so as the capacitors can be appropriately adjusted to the desired amplitude to $V_{dc}/4$. The capacitors voltages ripple are obtained for two half cycles:

$$\begin{aligned} & V_1|_0^{\pi} \\ & = V_1|_{\pi}^{2\pi} \frac{2}{ZC_1} \Big(\underbrace{\sum_{n=1}^{\infty} \frac{-H_n}{n\omega} \cos(n\omega t) \Big|_{\alpha_2}^{\alpha_3}}_{C_1, C_2 \text{in} \frac{\pm E}{2}} + \underbrace{\sum_{n=1}^{\infty} \frac{-H_n}{n\omega} \cos(n\omega t) \Big|_{\alpha_3}^{\alpha_4}}_{C_1 \text{in} \frac{+3E}{4}} \Big) \\ & = \frac{2}{ZC_1} \Big(\underbrace{\sum_{n=1}^{\infty} \frac{-H_n}{n\omega} \cos(n\omega t) \Big|_{\pi+\alpha_1}^{\pi+\alpha_2}}_{C_1 \text{in} \frac{-E}{4}} + \underbrace{\sum_{n=1}^{\infty} \frac{-H_n}{n\omega} \cos(n\omega t) \Big|_{\pi+\alpha_2}^{\pi+\alpha_3}}_{C_1, C_2 \text{in} \frac{\pm E}{2}} \Big) \end{aligned} \tag{5}$$

$$\begin{aligned} & V_2|_0^{\pi} \\ & = V_2|_{\pi}^{2\pi} \frac{2}{ZC_1} \Big(\underbrace{\sum_{n=1}^{\infty} \frac{-H_n}{n\omega} \cos(n\omega t) \Big|_{\alpha_1}^{\alpha_2}}_{C_2 \text{in} \frac{\pm E}{4}} + \underbrace{\sum_{n=1}^{\infty} \frac{-H_n}{n\omega} \cos(n\omega t) \Big|_{\alpha_2}^{\alpha_3}}_{C_1, C_2 \text{in} \frac{\pm E}{2}} \Big) \\ & = \frac{2}{ZC_1} \Big(\underbrace{\sum_{n=1}^{\infty} \frac{-H_n}{n\omega} \cos(n\omega t) \Big|_{\pi+\alpha_2}^{\pi+\alpha_3}}_{C_1, C_2 \text{in} \frac{\pm E}{2}} + \underbrace{\sum_{n=1}^{\infty} \frac{-H_n}{n\omega} \cos(n\omega t) \Big|_{\pi+\alpha_3}^{\pi+\alpha_4}}_{C_2 \text{in} \frac{-3E}{4}} \Big) \end{aligned} \tag{6}$$

Since the time duration for integral functions of Eq. (5) and Eq. (6) is changed by changing the pulses width as a result of changing the modulation index of switching technique, the redundant switching state must be deal into a PWM technique to adjust the charging and discharging time and regulate the capacitors voltages to the desired amplitude level. As it shown in Eq. (5) and Eq. (6), controlling both capacitors voltages to the levels $\pm E/2$ leads to equal ripple values in both of half cycle that consequently guarantee voltage balancing. Indeed, both DC capacitors have same state for $\pm E/2$; however, only one of them is charged/discharged for $\pm E/4$ and $\pm 3E/4$. Since C_1 is charging in $+3E/4$ and discharging in $-E/4$; so, by regulating capacitors voltages in levels $\pm E/2$ using redundant switching states, charging and discharging of C_1 would be equal in the $+3E/4$ and $-E/4$; respectively. Same procedure occurs for C_2 that is charging in $-3E/4$ and discharging in $+E/4$. Therefore, the redundant switching states for middle levels ($\pm E/2$) adjust amount of charging and discharging time and with respect to Eq. (5) and Eq. (6) to keep capacitors voltages balanced to the desired DC levels during a full cycle. Therefore, it is proven that DC-link capacitors of PEC inverter are perfectly balanced if a PWM control is accordingly designed to integrate the redundant switching states particularly ones regarding to the middle levels ($\pm E/2$) with modulation technique.

B. PROPOSED ACTIVE CAPACITOR VOLTAGE BALANCING PWM TECHNIQUE USING SINGLE VOLTAGE SENSOR FOR AUXILIARY DC-LINK

It was mathematically discussed and proved in section III A that the redundant switching states regarding to the middle voltage levels ($\pm E/2$) are adequate to adjust the charging and discharging time of capacitors and regulate their voltages to one quarter of input DC voltage amplitude. Using the performed capacitors voltages analysis, the corresponding flowchart for active capacitor voltage balancing of PEC9 inverter has been drawn and shown in Fig. 4. Fig. 5 also shows the block diagram of proposed active capacitor voltage balancing algorithm approach integrated into the nine-level PWM technique to regulate the capacitors voltages to one quarter of DC input amplitude by controlling auxiliary DC-link voltage. According to the designed active voltage balancing PWM technique, the DC-link voltage that is the

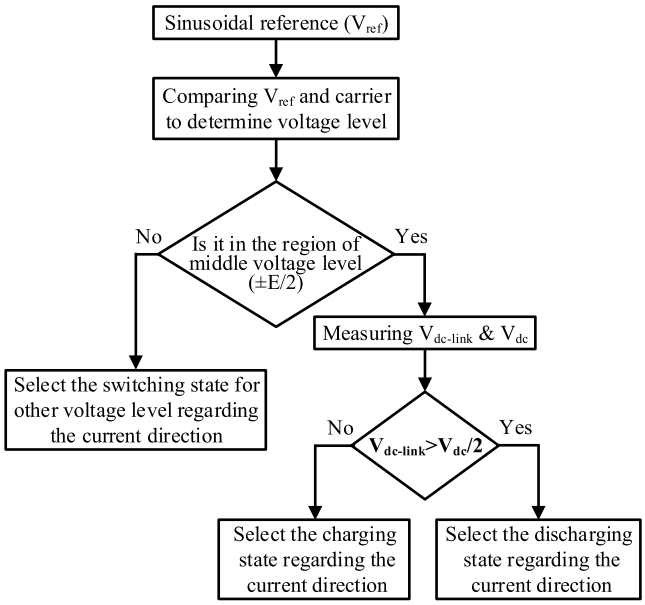

FIGURE 4. The designed flowchart for the active capacitor voltage balancing of PEC9 inverter.

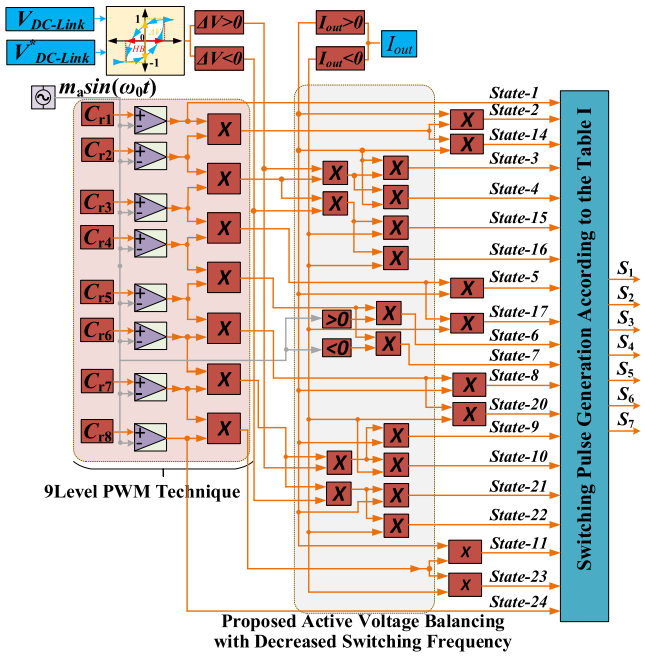

FIGURE 5. The block diagram of the proposed single sensor active voltage balancing method.

summation of both capacitors is measured by a single voltage sensor, and then compared to half of DC input reference voltage in order to find the error signal (ΔV). Therefore, it is not needed to control each DC capacitor separately. Using the redundant switching state would balance the DC-link voltage to E/2 and DC capacitors voltages are inherently regulated to E/4. According to the proposed method, if $\Delta V>0$ the discharging states (*3, 10, 16 & 21 for* $I_{out}>0$) and if $\Delta V<0$ the charging states (*4, 9, 15 & 22 for* $I_{out}<0$) are chosen

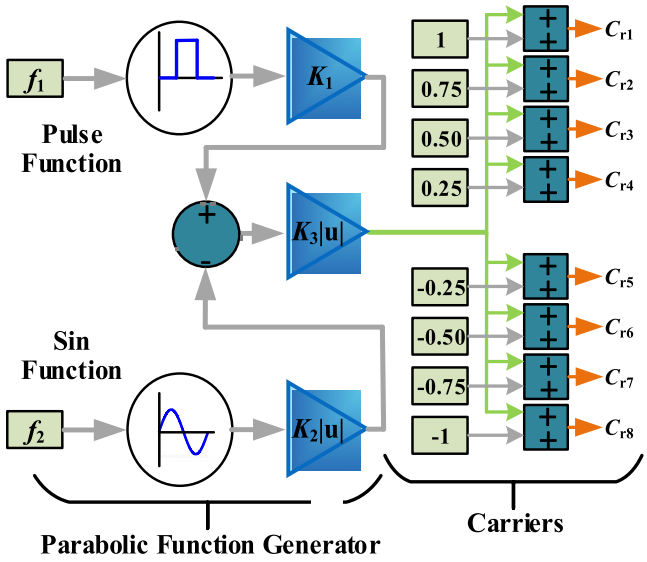

FIGURE 6. Parabolic waveforms generator using sinusoidal and pulse functions.

for the voltage levels $\pm E/2$. By fluctuating between charging and discharging in these two levels, the input DC voltage is equally shared between capacitors during one full cycle that each capacitor voltage is balanced to *E/4*. As well, since zero voltage level has redundant states, they are used to reduce the switching frequency. In this case, if the reference signal is positive the state 6 is chosen and if it is negative the state 7 is used to generate zero voltage level. It must be mentioned that for zero and $\pm E$ voltage levels the current direction is not considered because no capacitor is involved.

C. PWM TECHNIQUE USING HALF-PARABOLA CARRIER

New carrier waveform for PWM technique based on parabolic function has been designed to have better performance in controlling voltage profile harmonic distortion at lower switching frequency. Fig. 6 demonstrates the process of generating parabolic carrier signals that is defined using sinusoidal and pulse functions. Considering the frequency of pulse function f_1 two times greater than the sinusoidal function f_2 ($f_1=2f_2$) the half-parabola waveform is attained. However, based on the frequency ratio between f_1 and f_2, various types of parabolic functions can be generated. The factors K_1, K_2 and K_3 are also selected as *0.5*, *1* and *0.25*, respectively. Fig. 7 displays the nine hybrid level shift-PWM which consists of 8 carrier signals defined as half-parabolic function with switching frequency identified as C_{r1}, C_{r2}, C_{r3}, C_{r4}, C_{r5}, C_{r6}, C_{r7} & C_{r8} and sinusoidal reference signal with fundamental frequency as V_{ref}. Each carrier is used for the firing signals of one voltage level so as by comparing V_{ref} and C_{r1}, C_{r2}, C_{r3}, C_{r4}, C_{r5}, C_{r6}, C_{r7} and C_{r8} the related pulses for $+E$, $+3E/4$, $+E/2$, $+E/4$, $-E/4$, $-E/2$, $-3E/4$ and $-E$ are generated, respectively. Also, the zero level is generated when V_{ref} is between C_{r4} and C_{r5}.

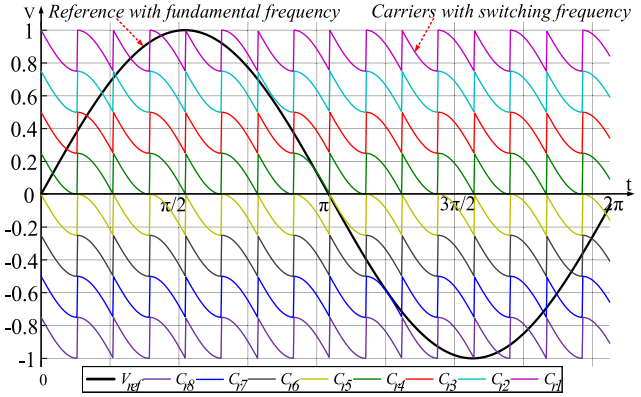

FIGURE 7. 9level hybrid PWM with half-parabola vertically shifted carriers.

TABLE 2. Component Comparison among 9Level converters and PEC9.

Inverter Type	DC Sources	Auxiliary Capacitor	Power Switch	Diode Clamped	Control Complexity
DSCC-HBC [36]	1	2	9	2	Low
Hybrid HB [37]	1	4	12	0	Low
DHANPC [38]	1	3	12	0	High
RDCANPC [39]	1	3	10	0	High
CSC [40]	1	1	10	0	Very high
CFC [41]	2	2	8	0	High
PUC9	1	3	10	0	Very High
PEC9	1	1	7	0	Low

IV. PEC VERSUS OTHER RECENTLY PRESENTED MULTILEVEL INVERTERS; COMPONENTS COMPARISON

Since PEC basic configuration has nine voltage levels, it is compared to the innovative single-DC source nine-level topologies which have been recently introduced. Table 2 lists the components comparison among nine-level topologies presented in [36]–[41] and PEC9. Based on Table 2, PEC9 has minimum number of active components (7 switches) and an auxiliary DC-link compared to other recent presented nine-level topologies. In comparison to nine-level PUC type, the PEC9 not only requires one less power switches and gate driver circuits, but also it reduces auxiliary DC-link and voltage sensors that has the advantages of active voltage balancing through redundant switching states without adding external complex current controllers.

Fig. 8 also presents a general comparison among PEC and other converters including CHB, NPC, FC and PUC as well as some novel topologies in terms of total number of passive and active components in comparable operation type of multilevel structure. The comparative study for number of components is done based on the number of levels (m) generated at the converter output. Figures 8-a and 8-b display the number of components and DC-link in PEC and other studied converters, respectively. As a result of horizontal extension capacitors through four-quadrant switch, the PEC inverter requires minimum auxiliary DC-link, semiconductor devices, and gate deriver circuits when it is configured to generate more than nine-level as shown in Fig. 8. As a comparison among CHB, NPC, FC and PEC, the latter makes use

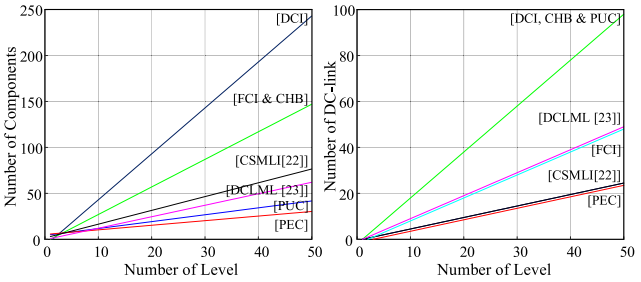

FIGURE 8. Component comparison among multilevel topologies and PEC, (a) number of active devices and gate driver circuits (b) number of DC-link.

of fewer components, which decrease manufacturing cost. As well, while PEC regulates the floating capacitors voltages by redundant switching states, the NPC and FC need to use complex controllers when operating with extended number of levels. As for the CHB, one can notice that not only more active devices are required; but also isolated DC-sources are employed which confines it to renewable energy applications. On the other hand, floating capacitors expansion in the form of E-Cell notably decreases the number of auxiliary DC-link. This will also lead to simultaneous capacitors charging or discharging with redundant states that effectively guarantee active voltage regulations with no need to complex additional external voltage controllers. As the number of levels increase, there will be more switching states as the result of E-Cell connection, which enhance the reliability of the PEC structure.

V. EXPERIMENTAL VALIDATION AND ANALYSIS OF PEC9

In this section, the proposed PEC inverter topology and designed active voltage balancing PWM technique has been analyzed through experimental analysis. A prototype of PEC9 inverter has been built and practically tested as an Uninterruptible Power Supply (UPS) application to evaluate its performance under different operating conditions including with and without voltage balancing method, switch fault condition, changing modulation index, increased or decreased of DC input voltage amplitude, and output load variations. The considered output load is constituted of an R-L circuit. The dSpace 1104 has been used as a fast prototyping real time controller with sampling time $T_s = 20\mu$s to implement the proposed active voltage balancing algorithm integrated into PWM technique designed by half-parabola carrier waveforms. Load current, main and auxiliary DC-link voltages are sensed by OPAL-RT high voltage/current measurement and sent to ADC of dSpace 1104. The experimental system parameters of PEC9 are listed in Table 3.

TABLE 3. PEC9 Parameters used for Experimental Tests.

DC bus voltage (V_{dc})	200 V
Fundamental and switching frequency	*60 Hz & 1500 Hz*
Auxiliary capacitor capacitance (C_1 & C_2)	*2500 μF*
Linear load; resistor and inductor (R & L)	*(40, 80) Ω & 50 mH*

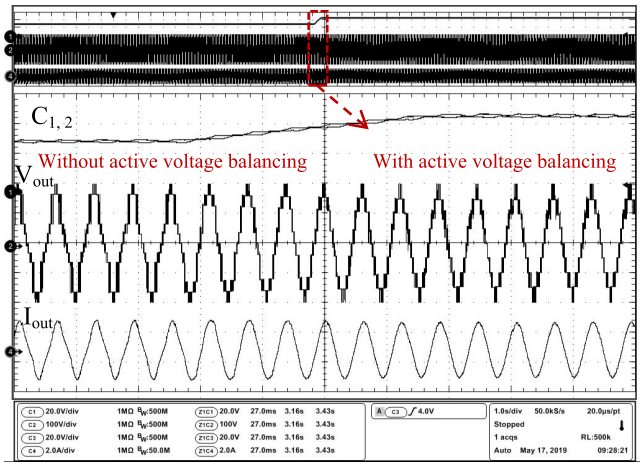

FIGURE 9. Experimental results of PEC9 operations with and without designed active voltage balancing PWM technique.

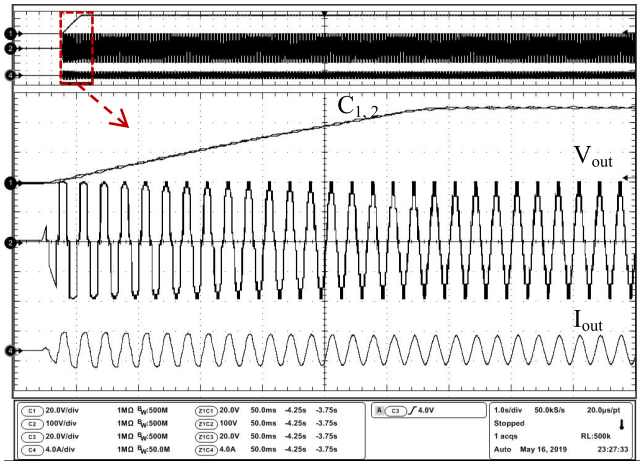

FIGURE 10. Experimental results of start-up mode of PEC9 operation controlled by the proposed active voltage balancing PWM technique.

A. TEST1: MULTILEVEL VOLTAGE OPERATION

In order to ascertain the excellent performance of the proposed active voltage balancing PWM method in regulating the capacitors voltages to the desired level, PEC9 has been operated with and without the designed technique under same amplitude modulation index (*MI=0.85*). Fig. 9 illustrates the experimental results of output voltage and current and C_1, C_2 voltages for nine-level PEC inverter. As it was discussed in section III A, the proposed active voltage balancing method has been accordingly designed to control the DC-link voltage to $V_{dc}/2$ by adjusting the charging and discharging time so as the capacitors voltages are inherently balanced to $V_{dc}/4$. As can be seen from Fig. 9, the capacitors voltages are less than desired level when the active voltage balancing is not applied; however, they are accurately tracks the determined amplitude and a perfect nine-voltage level waveform is then shaped when PEC9 is run by the designed technique.

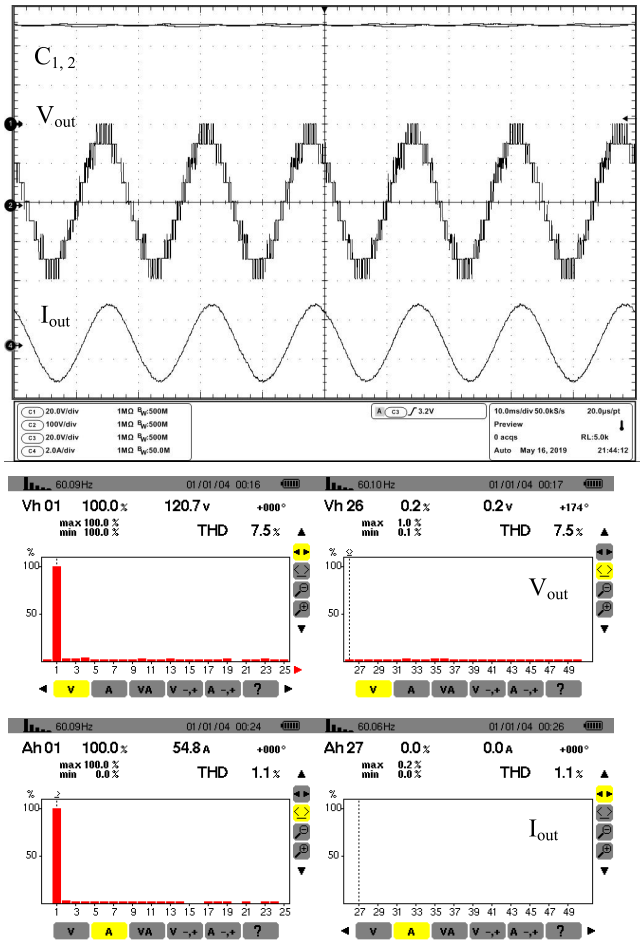

FIGURE 11. Steady state nine-level voltage waveform along with harmonic spectrum of nine- level output voltage and load current.

Afterwards, the start-up mode of PEC9 has been demonstrated in Fig. 10 to prove that the proposed active voltage balancing PWM technique is able to regulate the capacitors voltages to $V_{dc}/4$ as auxiliary DC-link is charged up to $V_{dc}/2$. The acquired results illustrates no pre-charged capacitors is needed for the PEC topology with the proposed control technique. Fig. 11 also shows the zoom of Fig. 10 which confirms that the capacitors voltages ripple is less than 5%. Also, output voltage and current harmonic contents are depicted when PEC is controlled by the proposed half-parabola PWM technique with modulation index equal to *0.85* and an output load $R=80\Omega$ and $L=50mH$. The detail amplitude of every voltage and current harmonic order of nine-level PEC inverter has been shown in Table 4.

As it was mentioned, PEC9 has the ability of generating multilevel voltage waveforms by applying appropriate switching patterns. To further illustrate highly capability of multilevel voltage operation PEC inverter, it has been tested under switch fault condition by which the four-quadrant switch is set to OFF state so nine-level PEC operates as five-level inverter. Fig. 12 demonstrates the experimental

TABLE 4. The amplitude of harmonic spectrum of nine- level output voltage and load current of Fig. 11.

Voltage Harmonic						Current Harmonic					
	(%)		(%)		(%)		(%)		(%)		(%)
H01	100.0	H19	1.8	H37	0.5	H01	100.0	H19	0.1	H37	0.1
H02	0.2	H20	0.5	H38	0.5	H02	0.1	H20	0.1	H38	0.1
H03	0.5	H21	0.5	H39	1.2	H03	1.2	H21	0.0	H39	0.2
H04	0.7	H22	0.5	H40	0.1	H04	0.1	H22	0.0	H40	0.1
H05	0.4	H23	0.7	H41	0.7	H05	0.3	H23	0.1	H41	0.3
H06	0.5	H24	0.4	H42	1.2	H06	0.4	H24	0.1	H42	0.1
H07	1.3	H25	0.9	H43	0.7	H07	0.4	H25	0.1	H43	0.2
H08	1.0	H26	1.9	H44	0.6	H08	0.3	H26	0.2	H44	0.1
H09	1.1	H27	1.3	H45	1.6	H09	0.5	H27	0.1	H45	0.2
H10	0.9	H28	0.9	H46	0.8	H10	0.4	H28	0.1	H46	0.1
H11	1.1	H29	1.5	H47	1.7	H11	0.3	H29	0.1	H47	0.1
H12	0.5	H30	0.9	H48	4.4	H12	0.2	H30	0.2	H48	0.3
H13	0.9	H31	1.2	H49	0.3	H13	0.1	H31	0.3	H49	0.1
H14	0.4	H32	0.6	H50	0.3	H14	0.1	H32	0.1	H50	0.2
H15	0.3	H33	0.9			H15	0.2	H33	0.2		
H16	0.2	H34	1.2			H16	0.2	H34	0.1		
H17	1.2	H35	2.5			H17	0.2	H35	0.3		
H18	0.1	H36	1.1			H18	0.1	H36	0.2		

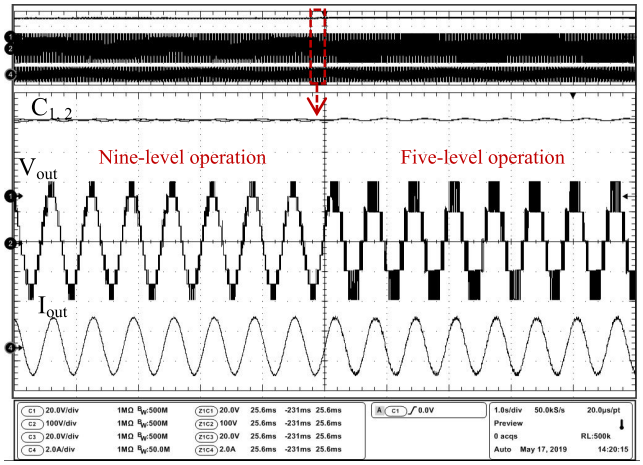

FIGURE 12. Experimental results of dynamic changes from nine- to fivelevel voltages of PEC9 inverter under faulty four-quadrant switch condition.

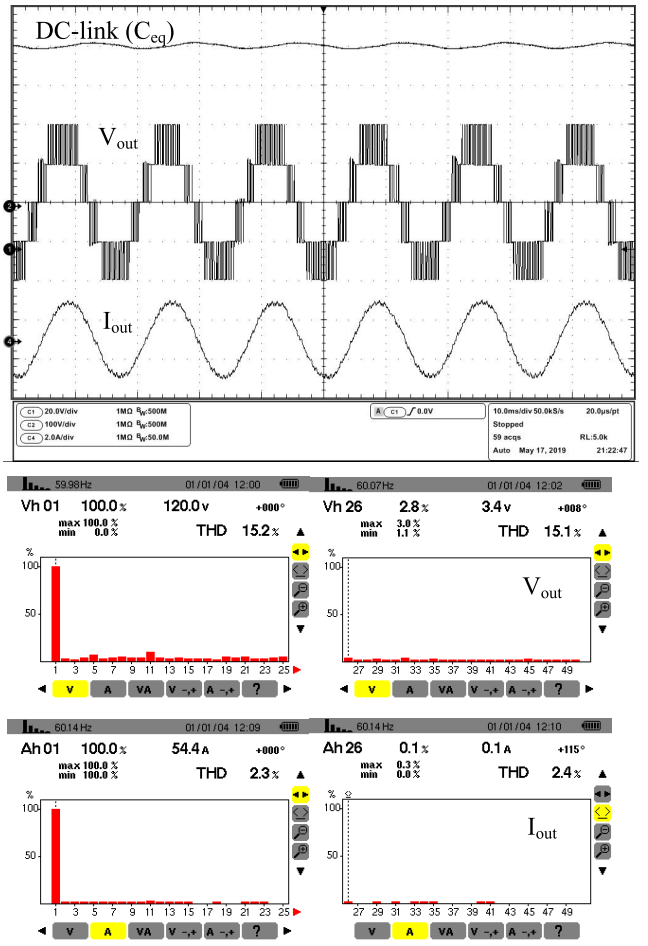

FIGURE 13. Steady state five-level voltage operation of PEC inverter along with output voltage and load current harmonic spectrum.

TABLE 5. The amplitude of harmonic spectrum of five- level output voltage and load current of Fig. 13.

Voltage Harmonic						Current Harmonic					
	(%)		(%)		(%)		(%)		(%)		(%)
H01	100.0	H19	1.5	H37	1.0	H01	100.0	H19	0.5	H37	0.2
H02	1.1	H20	0.9	H38	1.6	H02	0.0	H20	0.3	H38	0.4
H03	1.4	H21	0.5	H39	1.8	H03	1.1	H21	0.1	H39	0.3
H04	3.0	H22	1.7	H40	3.1	H04	1.6	H22	0.3	H40	0.4
H05	2.3	H23	0.8	H41	4.9	H05	0.9	H23	0.2	H41	0.2
H06	1.0	H24	1.4	H42	2.4	H06	0.8	H24	0.2	H42	0.4
H07	1.9	H25	0.4	H43	1.0	H07	0.7	H25	0.2	H43	0.3
H08	1.2	H26	1.5	H44	0.3	H08	0.1	H26	0.3	H44	0.3
H09	4.3	H27	3.1	H45	2.8	H09	1.4	H27	0.2	H45	0.2
H10	1.7	H28	0.9	H46	2.1	H10	0.6	H28	0.2	H46	0.4
H11	3.0	H29	1.7	H47	1.7	H11	1.0	H29	0.2	H47	0.1
H12	1.6	H30	0.8	H48	1.5	H12	0.1	H30	0.1	H48	0.2
H13	2.7	H31	1.5	H49	1.7	H13	0.9	H31	0.2	H49	0.0
H14	1.4	H32	0.5	H50	8.7	H14	0.3	H32	0.1	H50	0.5
H15	1.2	H33	0.2			H15	0.4	H33	0.2		
H16	0.6	H34	1.4			H16	0.1	H34	0.2		
H17	1.9	H35	2.4			H17	0.5	H35	0.1		
H18	0.4	H36	0.3			H18	0.1	H36	0.2		

results of dynamic PEC9 operation including output voltage and current as well as DC capacitors voltages waveforms when the inverter immediately changes from nine-to five-level operations. By turning OFF the four-quadrant switch, both series connected capacitors C_1 and C_2 are considered as one and consequently five-level voltage is achieved when DC-link voltage is kept balanced to $V_{dc}/2$. There is no transient between five- and nine-level output voltage operations of PEC inverter and the capacitors voltages are balanced to $V_{dc}/4$ in both cases operations. In addition, experimental results of five-level operation of PEC inverter shows variables of Fig. 12 as well as the voltage and current harmonics spectrum are depicted in Fig. 13. The details amplitude of each voltage and current harmonic order of five-level operation of PEC inverter are listed in Table 5. Furthermore, it needs to be mention that seven and eleven voltage levels are also achievable through PEC9 topology; but, it requires an external current controller to adjust the auxiliary DC-link voltage to one third and two fifth of input DC voltage, respectively. As can be seen from harmonic spectrum analysis of five-and nine-level voltages, the THD has been obtained as *15.2%* and *7.4%*; respectively, when switching frequency is *1500 Hz*. It must be noticed that S_1 and S_4 are switched at the fundamental frequency; whereas the remaining S_2, S_3, S_5, S_6, S_7, are fired at the switching frequency.

B. TEST2: MODULATION INDEX AND DC INPUT VOLTAGE VARIATIONS

In order to investigate the reliability of the proposed active voltage balancing method, the PEC9 inverter has been tested for pulse width and input voltage changes. Fig. 14-a shows PEC9 experimental results of output voltage, load currents

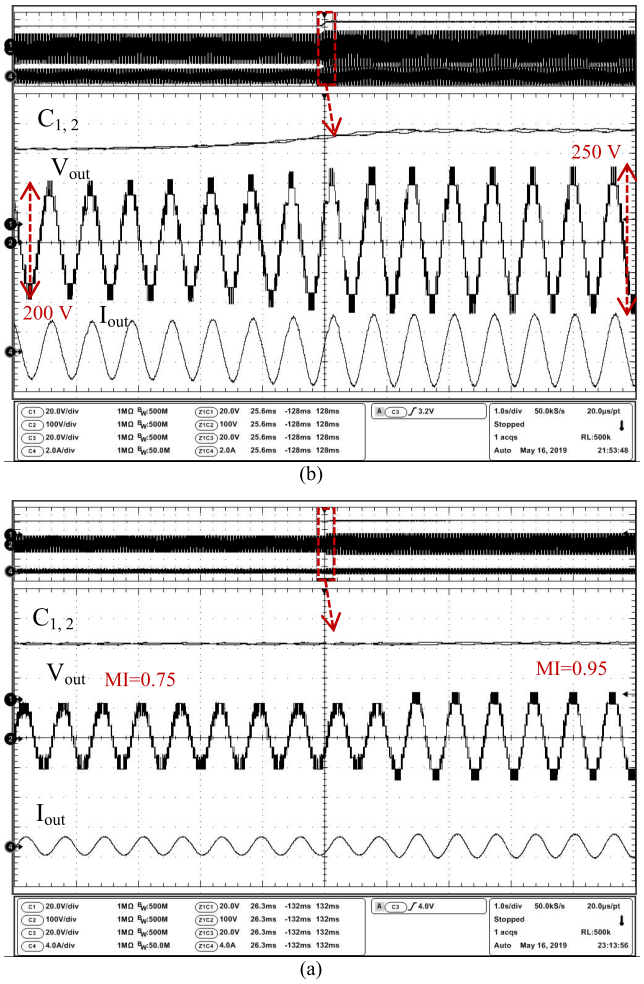

FIGURE 14. Experimental results of nine-level voltage (V_{out}), load current (I_{out}) and split DC capacitors voltages ($C_{1,2}$) of PEC9, (a) modulation index changes, (b) DC input variations.

and floating capacitors voltages while modulation index changes from *0.75*-to-*0.95* and the DC input voltage is fixed to *200 V*. As it is clear from Fig. 14-a, seven voltage levels are obtained when modulation index (MI) is set to 0.75 since the reference sinusoidal signal is lower than last carrier signals (C_{r1} and C_{r8}) to generate the ninth level that is obtained for MI higher than 0.95. Moreover, the input current is increased by changing modulation index from 0.75-to-0.95 as the output voltage changes from seven-level to nine-level. Despite modulation index changes, one can notice capacitors voltages perfectly track their references and remain balanced and equal to $V_{dc}/4$ without being affected by transient while the capacitors voltages ripple is kept below 5%. Fig. 14-b displays the same results of PEC9 when MI=0.85 kept constant, and DC source voltage increased from *200V* to *250V*. As depicted in Fig. 14-b, once again the capacitors voltages inherently track their reference of $V_{dc}/4$ with voltage ripple below 5% which is acquired by controlling the DC-link voltage to $V_{dc}/2$ using redundant switching states.

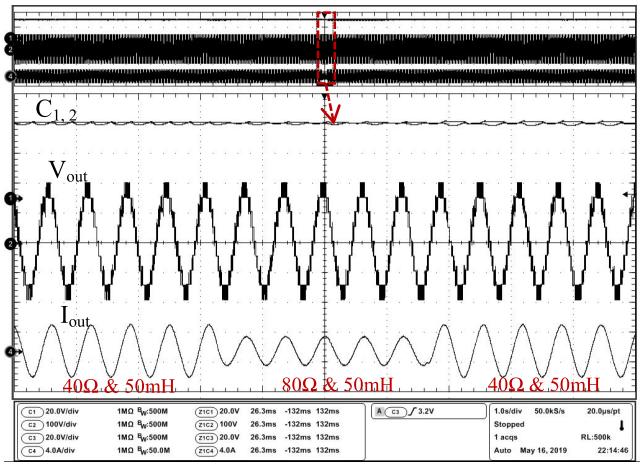

FIGURE 15. Experimental results of nine-level voltage (V_{out}) load current (I_{out}) and split DC capacitors voltages ($C_{1,2}$) of PEC9 for load changes from 40 Ω to-80 Ω and back to40 Ω.

C. TEST3: OUTPUT LOAD CHANGES

The floating capacitors regulated voltages has been tested for output loads power and frequency variations to scrutinize proposed active voltage balancing PWM based half-parabola type of carrier signal. Fig. 15 shows experimental results of output voltage, load current and floating capacitors voltages when the load resistance changes from *40*Ω to *80*Ω and then back to *40*Ω, while the inductive component remains constant equal to *50 mH*. According to Fig. 15, output load variations do not affect the split capacitors voltages regulations neither the voltage ripple as they are balanced and equal to the desired reference amplitude $V_{dc}/2$ with ripple less than 5%. Moreover, no transition or changing in DC capacitors voltages ripple during the load variation can be observed.

VI. CONCLUSION

In this paper, a novel nine-level single-DC source Packed E-Cell (PEC9) topology has been introduced as a promising candidate for single-phase inverter suitable for symmetrical and asymmetrical series of connection. The presented structure is indeed an optimized compact design topology which permits the reduction of auxiliary DC-link and components count by using E-Cell type of connection. Moreover, by horizontal extension of auxiliary DC-link, in the form of E-Cells, simultaneous charging or discharging with redundant state are achieved that guarantees floating capacitors voltage balancing under all operating conditions. An active voltage-balancing algorithm was integrated to the half parabola carrier PWM based technique to efficiently regulate floating capacitors voltages. It was also demonstrated that different output stepped voltage waveforms are achievable without changing in converter circuit design. The presented experimental results of PEC9 validated its reliable performance in keeping capacitors voltages balanced under different load and source conditions that can emerge as a competitive topology for various industrial standalone and grid-tied applications.

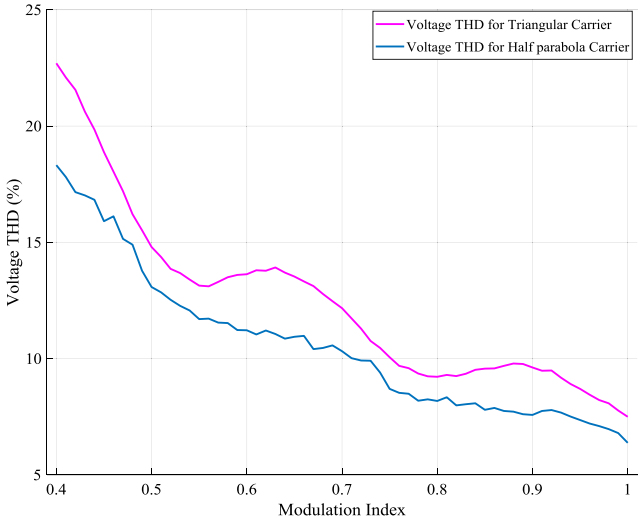

FIGURE 16. Voltage THD comparison of PEC9 inverter when triangular and proposed half parabola carriers are separately used for PWM technique.

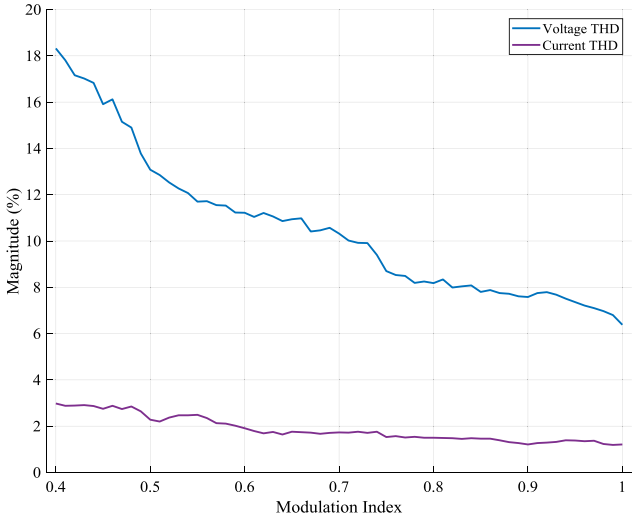

FIGURE 17. The obtained THD of voltage and current of PEC9 inverter for wide range of modulation index when it is controlled by proposed half parabola PWM technique.

APPENDIX

A. CONVENTIONAL TRIANGULAR CARRIER VERSUS PROPOSED HALF PARABOLA CARRIERS

In this paper, the half parabola waveform has been used as the carrier signal in the designed active voltage balancing PWM technique. Although any other carrier waveform could be utilized, half parabola has some interesting advantages. In comparison to the conventional triangular carriers, half parabola leads to improve the total harmonic distortion of voltage and current waveform. Fig. 16 displays the output voltage THD obtained over a wide range of modulation index when the half parabola and triangular carriers are used with the same frequency in the proposed active voltage balancing PWM technique to control PEC9 inverter. The inverter is connected to the linear R-L load (R=80Ω and L=50mH) in both case of operation. The results show that using half parabola carrier reduces the voltage THD compared to the traditional triangular one.

B. PEC9 VOLTAGE AND CURRENT THD

In order to evaluate the quality of generated voltage/current waveform of PEC9 inverter using the designed half parabola carrier for the switching method, their THD value has been surveyed for a wide range of modulation index and different power factors. Fig. 17 illustrates the voltage and current THD while the modulation index changes from 0.4 to 1. The result demonstrates that voltage and current THD are decreased as modulation index is increased which confirms the performance of the proposed half parabola PWM technique.

Fig. 18 also shows the current THD for different values of linear resistor-inductance type of load. The value of resistor (R) is *80* Ω and the inductance values (L) have been considered as (*10, 20, 30, 40 & 50*) *mH* and the current THD has been obtained for each of these load condition when modulation index is *0.8, 0.85, 0.9, 0.95* and*1*. As it is clear in Fig.18, the current THD is significantly decreased by raising amplitude modulation index as well as increasing the inductance load value which acts as a filter.

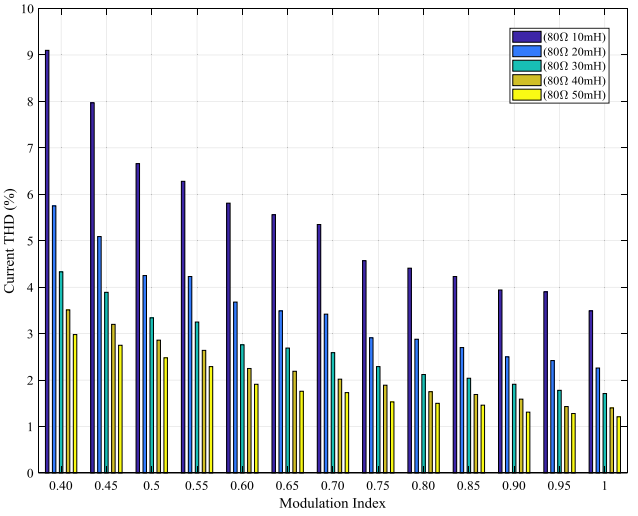

FIGURE 18. The attained current THD of PEC9 for different loads condition and modulation index.

C. DC-LINK CAPACITORS VOLTAGES RIPPLE

An active capacitor voltage balancing based half parabola PWM technique was designed to guarantee the desired regulation performance of DC-link capacitors voltages of PEC9 by adjusting the charging and discharging time using the redundant switching states of middle voltage level ($\pm E/2$). The various experimental tests of PEC9 illustrated that the proposed balancing technique is perfectly able to balance the capacitor voltage to one quarter of input DC voltage with acceptable voltage ripple below *5%* under different operation conditions. Fig. 19 displays simulation results of

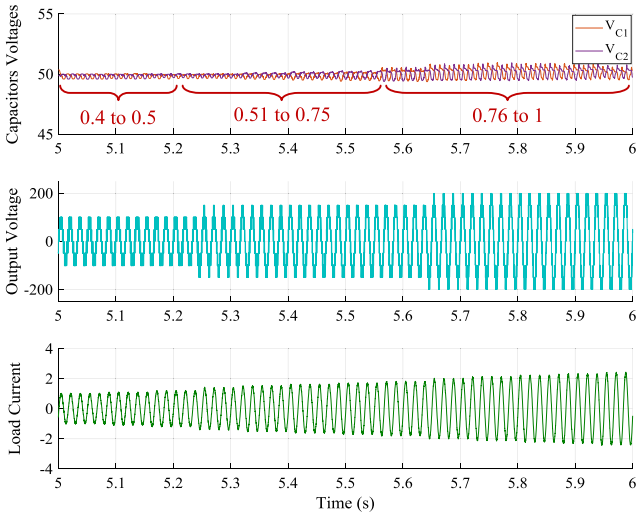

FIGURE 19. **The capacitors voltages ripple of PEC9 while the modulation index changes from 0.4 to 1.1.**

PEC9 inverter including DC capacitors voltages, output voltage and current when the modulation index varies for a vast range from *0.4* to *1*. As it is clear, the capacitor voltages are balanced with voltage ripple kept less than *5%* while the modulation index changes in a wide range. Number of voltage levels has been increased from five- to seven- and to nine-level as a result of raising modulation index. The output current has been also increased consistent with rising of number of voltage levels.

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