A Novel Multilevel Multi-Output Bidirectional Active Buck PFC Rectifier

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Abstract—**This paper presents a new family of buck type PFC (power factor corrector) rectifiers that operates in CCM (continuous conduction mode) and generates multilevel voltage waveform at the input. Due to CCM operation, commonly used AC side capacitive filter and DC side inductive filter are removed from the proposed modified packed U-cell rectifier structure. Dual DC output terminals are provided to have a 5-level voltage waveform at the input points of the rectifier where it is supplied by a grid via a line inductor. Producing different voltage levels reduces the voltage harmonics which affects the grid current harmonic contents directly. Low switching frequency of the proposed rectifier is a distinguished characteristic among other buck type rectifiers that reduces switching losses and any high switching frequency related issues, significantly. The proposed transformer-less, reduced filter and multilevel rectifier topology has been investigated experimentally to validate the good dynamic performance in generating and regulating dual 125V DC outputs terminals as telecommunication boards feeders or industrial battery chargers under various situation including change in the loads and change in the in main grid voltage amplitude.**

Index Terms—**Packed U-Cell, PUC5, HPUC, Buck PFC rectifier, multilevel converter, power quality.**

I. INTRODUCTION

NOWADAYS DC power supply is a big demand of industries to charge up batteries especially for uninterruptible power supplies (UPS), electric vehicles (EV), feeding communication boards and to use in various power applications [1]. Regulated constant voltage at the output in addition to low harmonic and unity power factor current at the input should be ensured in such equipment to comply with harmonic standards defined by different association like IEEE and IEC [2, 3]. PFC rectifiers have been proposed many years ago to overcome the input AC voltage and current power factor issue. Such converters can be divided into two main categories based on their output DC voltage amplitude. If the output DC voltage level is less than the input AC peak voltage value, it is called a PFC buck rectifier and conversely, a PFC boost rectifier generates a DC voltage greater than the AC peak voltage [4].

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PFC buck rectifiers are mainly known with their discontinuous conduction mode (DCM) which complicates formulating the output voltage. On the other hand, DCM operation makes the output DC voltage control depending on the load impedance and also makes it inevitable to use large inductive filters at DC side [5, 6]. Moreover, high switching frequency e.g. 65 kHz and more is a normal operating point in reported topologies that increases switching losses significantly [7, 8]. Large-size LC filters at the output as well as non-removable AC side filters are inherent disadvantages of PFC buck rectifiers. Detailed problems associated with such rectifiers are investigated in the literature [9, 10]. Another configuration to generate a reduced DC voltage is combination of diode-bridge and dc-dc buck converter in which the AC voltage is rectified by that diode-bridge and then DC voltage is stepped down at a desired level by the chopper. Such two-stage structures present more power losses, low efficiency and high manufacturing costs in medium and high power applications due to using many semiconductors and reactive components [11].

Regarding above-mentioned facts, PFC buck rectifiers are not so much welcome in industrial applications compared to boost type of those PFC rectifiers. Such boost types do not require bulky filters at AC or DC sides since ensuring harmonic suppression of input current, unity power factor operation of the system and constant DC voltage at the output terminal. To have a reduced DC voltage at the output, bridgeless PFC boost rectifiers are usually connected to the main grid after a step-down transformer [12]. Therefore, to have a 125 V DC at the output terminal of a PFC boost rectifier from a 120V RMS grid, a transformer should be used to reduce the grid peak voltage to less than 125 V that has its own disadvantages.

In this paper, a new family of bidirectional bridgeless buck PFC rectifiers is introduced which is an efficient cure to all above-mentioned issues. The proposed HPUC (Hani Packed U-Cell) rectifier operates in boost mode while splitting the output voltage terminals to have multiple-output with reduced voltage levels as buck mode. Supplying multiple-output terminals result in producing a multilevel voltage waveform at the rectifier input that reduces the harmonic content of the rectifier voltage and consequently the grid current harmonic without using large inductive filters at the AC side [13]. Boost mode operation of the overall system helps removing bulky filters from both sides specially the DC side inductor. Moreover, CCM operation is guaranteed in a whole period. The topology and operation of the HPUC rectifier is explained in section II. Integrated voltage control into switching

technique as well as implemented controller are presented in section III and IV, respectively. Power balance analysis of the HPUC rectifier is studied in section V. Eventually low harmonic content of the input 5-level voltage waveform, unity power factor and low harmonic AC current waveform of the proposed rectifier is validated through experimental tests. Results are illustrated and discussed in section VI to prove the good dynamic performance of the proposed rectifier in various situations including change in the loads or input AC voltage amplitude.

II. PROPOSED PFC BUCK RECTIFIER TOPOLOGY AND OPERATION PRINCIPLE

The proposed rectifier topology has been shown in figure 1. It has 6 active switches and two output DC terminals. The output terminals are providing voltages V_1 and V_2 to loads that should be identical as E to have a five-level voltage waveform at the rectifier input. Rectifier input voltage is measured at points 'a' and 'd' as V_{ad}. The switching states associated to the introduced rectifier have been listed in table I.

The proposed HPUC rectifier is a modification to the well-known PUC converter [14, 15] in which the lower U-cell components are connected in reverse direction. The PUC converter was proposed as an inverter to generate 7-level voltage waveform while using a single isolated DC source and a controlled capacitor [16]. Moreover, it has been tested as a 7-level rectifier supplying a DC load in boost mode of operation [17]. Another similar structure with cascaded cells was proposed in [18] but as an inverter application with no control that only requires too many isolated DC sources. The idea of the HPUC is to introduce a rectifier by utilizing the similar structure of PUC with slight modification working in buck mode to supply DC loads with lower voltages than the grid where no transformer and additional filter would be required.

It is clear from table I that each pair of switches S_1-S_4, S_2-S_5 and S_3-S_6 is working in complementary manner. All switching states and associated conducting paths are shown in figure 2 which will be used in voltage regulator design section.

By controlling output DC voltages, V_{ad} would have five levels including ±2E, ±E, 0 that the maximum value is +2E. The principal concept of proposing this topology as a buck rectifier relies on this maximum value of V_{ad} which should be more than the AC source peak value ($v_{s\ max}$). The following relations can be written, accordingly.

$$V_{ad} \geq v_s \rightarrow 2E \geq v_{s\ max} \rightarrow E \geq \frac{v_{s\ max}}{2} \quad (1)$$

For instance, if RMS voltage of the AC source is 120V, then the maximum value would be 170V and the following relations would be obtained. To maintain the stable operation of the converter in buck mode, the maximum generating DC voltage is set at $v_{s\ max}$ which would be 170 V here.

$$\frac{v_{s\ max}}{2} \leq E \leq v_{s\ max} \rightarrow 85V \leq E \leq 170V \quad (2)$$
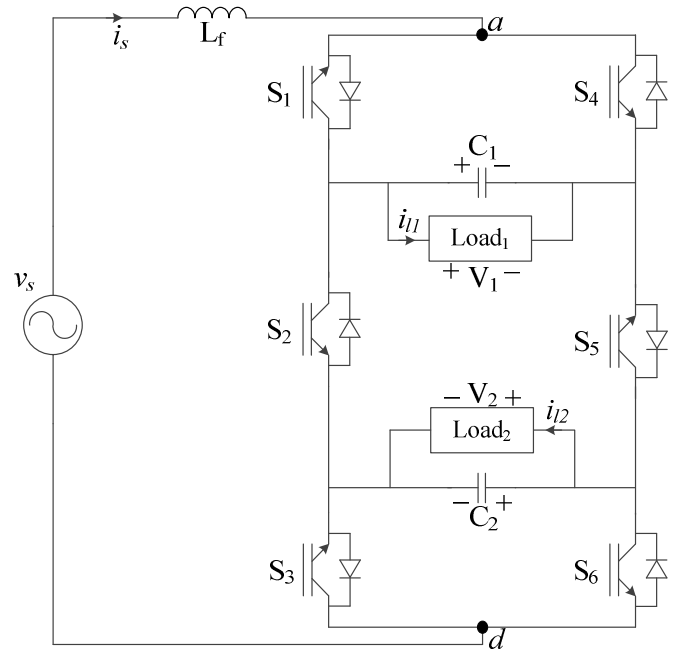

Fig. 1.   Proposed HPUC five-level buck PFC rectifier

TABLE I
SWITCHING STATES OF THE PROPOSED
HPUC FIVE-LEVEL BUCK PFC RECTIFIER

Switching State	S_1	S_2	S_3	S_4	S_5	S_6	V_{ad}	V_{ad} voltage levels
1	1	0	1	0	1	0	V_1+V_2	+2E
2	1	0	0	0	1	1	V_1	+E
3	0	0	1	1	1	0	V_2	+E
4	1	1	1	0	0	0	0	0
5	0	0	0	1	1	1	0	0
6	1	1	0	0	0	1	$-V_2$	−E
7	0	1	1	1	0	0	$-V_1$	−E
8	0	1	0	1	0	1	$-V_1-V_2$	−2E

As mentioned above, this rectifier is a boost converter in grid point of view due to generating peak voltage of V_1+V_2 at the input (V_{ad}) which is always equal or greater than the $v_{s\ max}$. On the other hand, by splitting the produced DC voltage between two output terminals, each one would have half voltage amplitude so their amplitude are always less than or equal to the $v_{s\ max}$ that guarantees the buck mode operation of proposed rectifier from loads points of view. It could be concluded that by using two output terminals, the grid is deluded by the converter.

Therefore, the stepped down DC voltages are achieved however the overall rectifier is in step-up mode. As results, the bulky inductor at DC side as well as the capacitor filter at AC side of conventional PFC buck rectifiers would be removed. Moreover, low harmonic V_{ad} and also low THD line current (i_s) are attained even when the proposed rectifier is running at low switching frequency leads to low power losses and high efficiency [19].
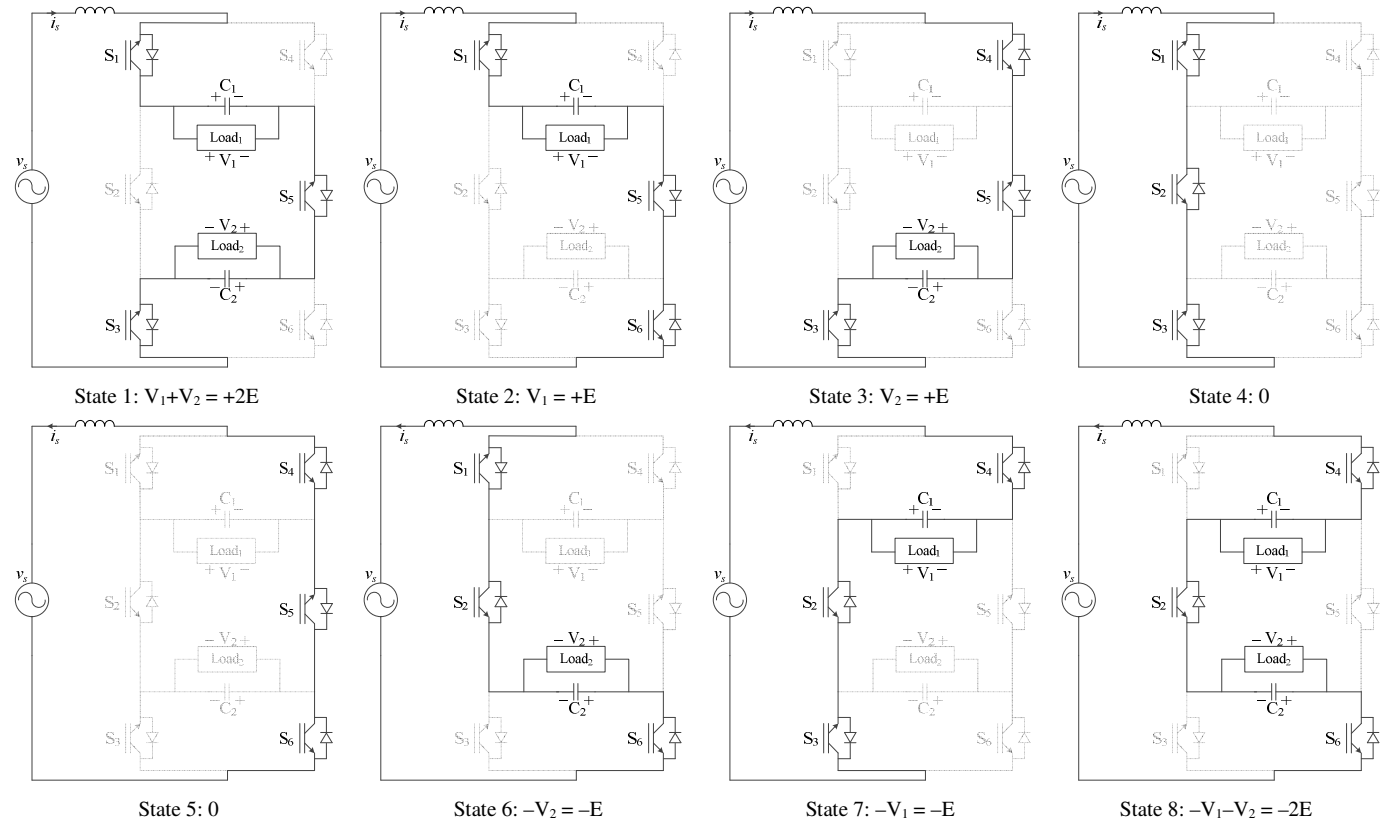
Fig. 2.   Operating sequences and conducting paths of proposed HPUC 5-level buck rectifier

III.   SWITCHING TECHNIQUE AND INTEGRATED VOLTAGE REGULATOR

Due to utilizing more than one DC capacitor in multilevel converter topologies, regulating and balancing their voltages is the most challenging part of the controller [15, 20, 21]. Redundant switching states can play an important role in facilitating the controller duty of regulating the output DC terminals voltages. In this regard, the switching states should be analyzed precisely to find the charging and discharging path for capacitors. Table II lists such investigation results on the proposed rectifier switching states.

Noticing table II, it is clear that redundant switching states of 2, 3, 6 and 7 can help regulating capacitors voltages beneficially. Hence, the switching pattern of the PWM block would be modified in order to decide between switching states 2 or 3 when the line current is positive and the +E voltage level should be generated at the output. It means that if V_1 is less than V_2 then switching state 2 would be applied to switches and if V_1 is more than V_2 then the output pulses would be generated by switching state 3. The same process is defined to choose between switching states 6 or 7 when line current is negative and output voltage should be –E.

All these actions are taken inside the PWM block shown in figure 3. Moreover, the reference signal is first modulated by 4 vertically shifted carriers in order to determine the associated voltage level and then the required pulses are sent to the switches considering capacitors voltages and redundant switching states [22, 23].

TABLE II
EFFECT OF SWITCHING STATES ON OUTPUT DC CAPACITORS

Switching State	Line Current Sign	V_{ad}	V_{ad} voltage levels	Effect on C_1	Effect on C_2
1	$i_s > 0$	V1+V2	+2E	Charging	Charging
2	$i_s > 0$	V1	+E	Charging	Discharging
3	$i_s > 0$	V2	+E	Discharging	Charging
4	$i_s \geq 0$	0	0	Discharging	Discharging
5	$i_s \leq 0$	0	0	Discharging	Discharging
6	$i_s < 0$	-V2	–E	Discharging	Charging
7	$i_s < 0$	-V1	–E	Charging	Discharging
8	$i_s < 0$	-V1-V2	–2E	Charging	Charging

All these procedures are to simplify regulating DC voltage terminals. Therefore, the voltage control loop would generate less error due to balancing the DC voltages by the redundant switching states. Figure 3 depicts the PWM block input/output signals in detail.
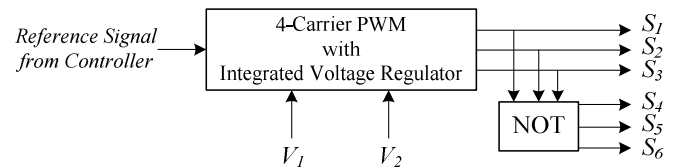

Fig. 3.   Input/output signals of PWM block with integrated voltage regulator

IV.   IMPLEMENTED CONTROLLER

A cascaded PI controller has been applied to regulate the three state space variables including capacitors voltages (V_1 & V_2) as well as grid current (i_s) and to provide a unity power

factor operation of the five-level rectifier [24]. Figure 4 shows the block diagram of the implemented controller. A phase lock loop (PLL) block is used to extract the voltage angle and generate the synchronized current reference i_s^* which should be drawn by the rectifier in order to ensure the power factor correction. The outer loop of the cascaded controller includes the voltage regulator which its output goes to the current controller (inner loop) as the reference signal amplitude. Therefore, to have balanced voltages at the output DC terminals, sum of the DC voltages are regulated using a PI controller. Each DC voltage reference is assumed as V_{ref}, thus the total DC voltage reference would be $2V_{ref}$. PI regulator minimizes the total DC voltages at $2V_{ref}$ as shown in Figure 4. Afterwards, the voltage balancing technique integrated into the switching method (as described in section III) is applied to ensure equal voltage amplitude ($V_1 = V_2 = V_{ref}$) at DC buses. Concluding that the controller is regulating total DC voltage as $2V_{ref}$ using the flowing current through the converter while the switching technique and redundant states would charge and discharge the capacitors equally to have identical voltage levels (V_{ref}) at the DC output terminals. That decoupled voltage control helps balancing capacitors voltages even in faulty conditions where the switching actions could not balance two DC voltages while the sum of DC voltages is regulated at $2V_{ref}$. This mode helps preventing any uncontrolled charging up of the capacitors to an unlimited level.
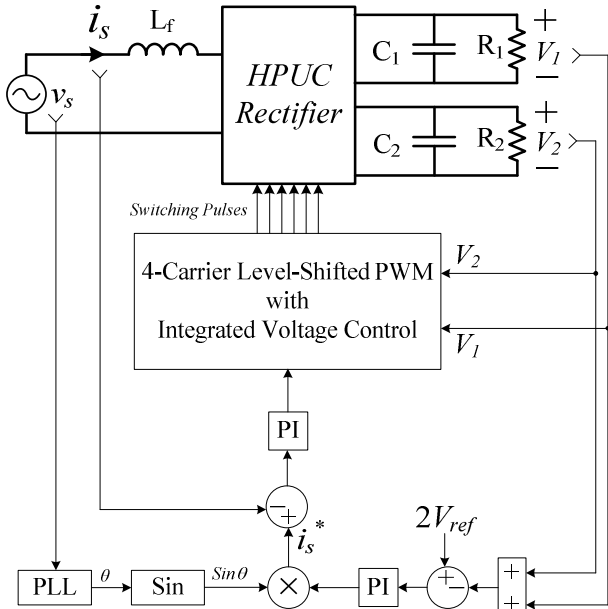

Fig. 4. Block diagram of the HPUC rectifier and Implemented controller

It should be noted for the inner loop (current control) PI controller have good performance where the input signal frequency is low (e.g. outer loop as DC voltage regulator); while it shows some steady-state error when the input is a time-varying signal, like a sinusoidal current, leads to tracking error in the line current [25]. To ensure the possible minimum error on the output current, the integral gain of the current control PI block should be small enough which makes the

inner loop faster than outer loop as well as not that small which is required to eliminate steady state error and consequently results would be acceptable [26].

V. POWER BALANCE ANALYSIS

Noticing to the HPUC rectifier configuration in the figure 1, it is clear that S_2 and S_5 have voltage rating of two times more than the other four switches (S_1, S_3, S_4, and S_6).

Therefore, S_2 and S_5 can be split into two series switches in order to suffer equal voltage rating as shown in figure 5. The point (m) is chosen to split two cells which are kind of full-bridge modules. Similarly to the work performed on cascaded H-bridge (CHB) multilevel converter [27, 28], the following analysis is done to show the power balance ratio between two independent loads connected to the proposed rectifier.
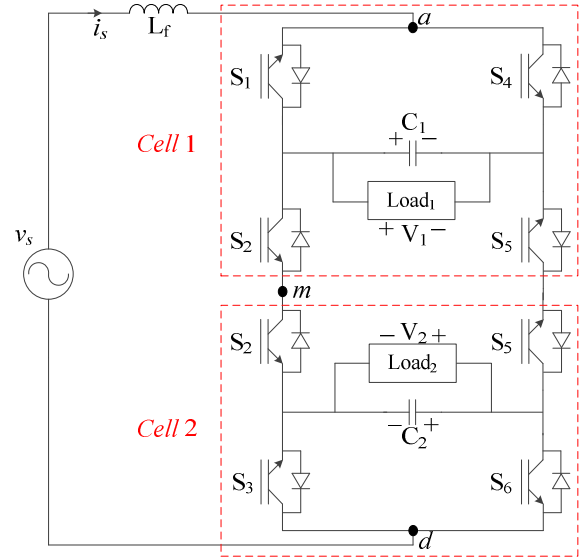

Fig. 5. Split configuration of the HPUC rectifier into two cells for power balance analysis

The following equation is visible on the rectifier structure:

$$V_{ad} = V_{am} + V_{md} \tag{3}$$

Therefore an extended representation of the HPUC rectifier topology shows that the latter is formed by two series cells (Cell 1 and Cell 2). Each cell generates a DC voltage to supply the load; however the common switches and current paths do not allow each cell to operate separately. To continue with the analysis, following definitions are provided:

v_f = RMS (V_{ad}) : rectifier RMS voltage

v_s = Grid RMS voltage

v_L = RMS (V_L) : Line Inductor RMS voltage

Moreover, since each cell voltage (V_{am} & V_{md}) are 3-level waveforms including 0 and ±E volts, their RMS values are defined as:

v_1 = RMS (Vam) = $0.7797 \times m_1 \times V_1$

v_2 = RMS (Vmd) = $0.7797 \times m_2 \times V_2$

Where, m_1 and m_2 are the modulation indexes of each cell that are between 0 and 1. So their maximum value would be defined as:

$v_{max1} = 0.7797V_1$

$v_{max2} = 0.7797V_2$

It should be noticed that these maximum values of RMS voltages are obtained in case of two separately working cells. The one line diagram of the HPUC rectifier can be drawn as shown in figure 6-a. By neglecting circuit power losses and capacitor energy consumption, it can be said that the power consumed in Cell 1 is P_1 and similarly for Cell 2 power is P_2. The total power is drawn from the grid as P. They can be formulated as below:

$$P_1 = \frac{V_1^2}{R_1} \;, \; P_2 = \frac{V_2^2}{R_2}$$
$$P = v_s i_s = P_1 + P_2 \tag{4}$$

From Eq. (4) and since DC voltages are controlled, this yield to Eq. (5):

$$\frac{P_1}{P_2} = \frac{R_2}{R_1} \tag{5}$$

In the HPUC rectifier, the buck mode of operation is proposed where $V_1 + V_2 = Max(V_{ad})$. Therefore considering RMS values, the following relation is achieved:

$$v_1 \leq v_f \;, \; v_2 \leq v_f \;, \; v_1 + v_2 = v_f \tag{6}$$

Based on voltage relations, the phasor diagram of the rectifier can be drawn as in figure 6-b.
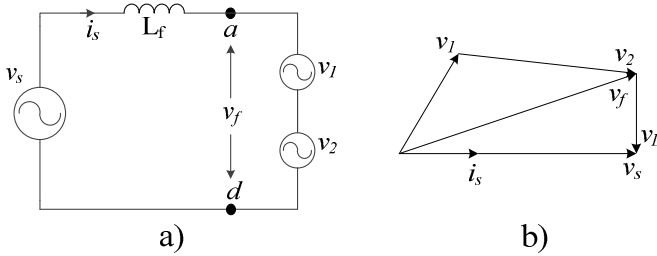

a)   b)

Fig. 6. a) one line diagram of the HPUC rectifier   b) Phasor diagram of the system voltages

Moreover, for the maximum voltage of each cell the following relation can be written [28]:

$$v_{max1} \leq v_f \;, \; v_{max2} \leq v_f \;, \; v_{max1} + v_{max2} \leq v_f \tag{7}$$

The maximum voltages that can be generated by each cell would produce the maximum power that can be delivered to the loads (P_1 & P_2) in a stable operation. Thus, the diagram shown in figure 7-a is obtained and the shaded area shows the area where maximum power can be delivered to loads while the rectifier works in stable mode. It means that the DC voltages are equally balanced and the input grid current is locked to the grid to deliver only active power.

Based on figure 7-a, v_1 and v_2 can be placed in the shaded area so the boundary would be the maximum and minimum limits for those voltages that gives the maximum and minimum power generated by each cell. Since the rectifier should always draw active power from the grid, therefore the

minimum and maximum limits are projected on the x-axis to ensure the unity power factor operation as 0° phase shift with current which is illustrated in figure 7-b.

Paying attention to the x_1-axis, the minimum power drawn by the Cell 1 is the left vertical dashed line which is due to the lowest RMS voltage (v_1). Therefore by assuming an equal current through the converter, the remained power ($v_s i_s - P_1$) is consumed in Cell 2. Since P_1 is at the minimum level, P_2 would be the maximum. Similarly, the maximum power limit of Cell 1 is the right vertical dashed line so the voltage vectors on x_2-axis are obtained.
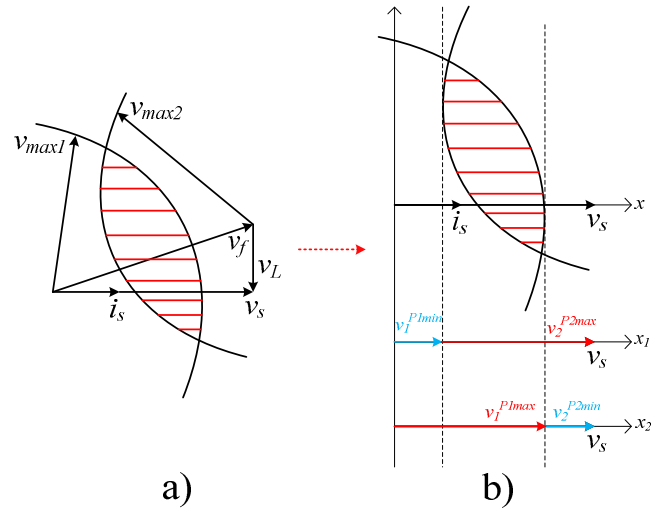

a)   b)

Fig. 7. a) stable operation area of the HPUC rectifier   b) Minimum and maximum power generated by each cell and associated voltages

Based on above explanation and figure 7, power relations are extracted for each cell power as Eq. (8).

$$P_{1\;max} = \frac{v_1^{P_1\;max}}{v_s} P$$
$$P_{1\;min} = \frac{v_s - v_2^{P_2\;max}}{v_s} P$$
$$P_{2\;max} = \frac{v_2^{P_2\;max}}{v_s} P \tag{8}$$
$$P_{2\;min} = \frac{v_s - v_1^{P_1\;max}}{v_s} P$$

Where, $v_1^{P_1\,max}$ is the cell voltage with maximum possible power delivering to the load. Other variables have the same definitions. Since two DC voltages are identical, minimum/maximum powers of two cells would be equal. Assuming $V_1 = V_2 = 125V$, the following values would be obtained:

$$P_{1\;max} = P_{2\;max} = \frac{125 \times 0.7797}{120} P = 0.8121P$$
$$P_{1\;min} = P_{2\;min} = \frac{120 - 125 \times 0.7797}{120} P = 0.1878P \tag{9}$$

Based on the above values, it can be concluded that each cell can have a specific maximum and minimum power as a portion of the input total power. Therefore, the highest difference between two cells power would be in a situation where the Cell 1 takes P_{1min} (or P_{1max}) and the Cell 2 consumes P_{2max} (or P_{2min}). Thus, the maximum power ratio between two cells and consequently the power ratio between two DC loads can be obtained as:

$$\frac{R_2}{R_1} = \frac{P_{2\ max}}{P_{1\ min}} = 4.32 \tag{10}$$

Due to symmetrical configuration of the HPUC rectifier, this ratio can be used for R_1/R_2 similarly.

To validate the performed analysis on the power balance of the HPUC rectifier, some simulations have been done in Matlab/SPS and three different values have been used for R_1 while R_2 was fixed at 43Ω to show the stable and unstable operation of the proposed rectifier. It should be noted that all simulation parameters except loads were same as experimental ones listed in Table III. As shown in figure 8, three steps have been applied.

At first step, $R_1 = R_2 = 43Ω$ so $R_2/R_1 = 1$ and rectifier works in stable mode drawing almost 750W from the grid as shown in figure 8-a (1^{st}s to 2^{nd}s). Grid voltage and current are in-phase and the rectifier voltage has 5 identical levels with low voltage ripple on DC capacitors as illustrated in figure 8-b.

At second step, R_1 is reduced to 15Ω to validate the capability of the rectifier to supply different loads yet in stable area and near the limit. As illustrated in figure 8-a (2^{nd}s to 3^{rd}s), 1400W power is delivered to various independent loads with equally balanced voltages but different ripples due to supplying smaller load on upper terminal (V_1). Grid voltage/current as well as the rectifier 5-level voltage waveform with identical levels have been provided in figure 8-c.

Eventually, at third step (3^{rd}s to 4^{th}s), R_1 is reduced to 8Ω forcing the rectifier to fall into the unstable area where $R_2/R_1 = 5.3$. As can be seen from figure 8-a at that time, the reduced load needs more power (about 1950W) but the converter cannot provide the requested amount of current and consequently the voltage drops down undesirably. Simultaneously, the other load voltage is increased unwantedly (because of the fact that PI regulator tries to keep the sum of DC voltages at 250V) so it draws more current leads to increase in the input power to 1650W. It is illustrated that two voltages are not balanced anymore. On the other hand, the line current is still controlled to be synchronized with grid voltage. Those Unbalanced voltage levels are observable in 5-level waveform of figure 8-d. Such unbalanced levels impose undesirable harmonics into the current waveform which requires larger filter to eliminate.
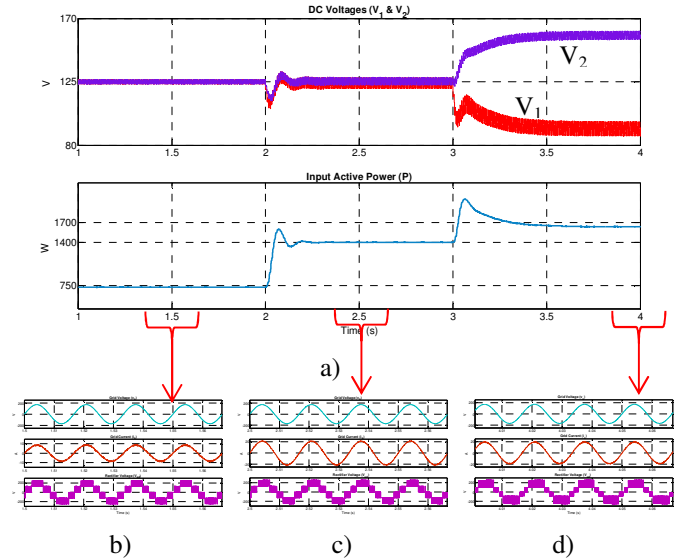

Fig. 8. Stable and unstable operation of the HPUC rectifier a) DC voltages and input active power during changes in the loads b) grid voltage/current and rectifier 5-level voltage when $R_1 = R_2 = 43Ω$ c) grid voltage/current and rectifier 5-level voltage when $R_1 = 15Ω$ and $R_2 = 43Ω$ d) grid voltage/current and rectifier 5-level voltage when $R_1 = 8Ω$ and $R_2 = 43Ω$

VI. EXPERIMENTAL RESULTS

A laboratory setup of proposed five-level buck converter has been built using 6 MOSFETS. The controller and switching technique has been implemented on dSpace1103 real-time controller with 20μs fixed sampling time to generate and send the firing pulses to turn on and off the switches. The rectifier has been connected to 120V RMS grid as real condition.

Output DC voltages have been set on 125V as buck mode operation; useable in industries to charge up batteries or in feeding telecommunication boards. Some changes are made in the operating condition such as load variation and AC source voltage fluctuation to validate the good dynamic performance of the proposed rectifier and implemented voltage regulator integrated into switching technique. All system parameters have been listed in table III.

TABLE III
EXPERIMENTAL SYSTEM PARAMETERS

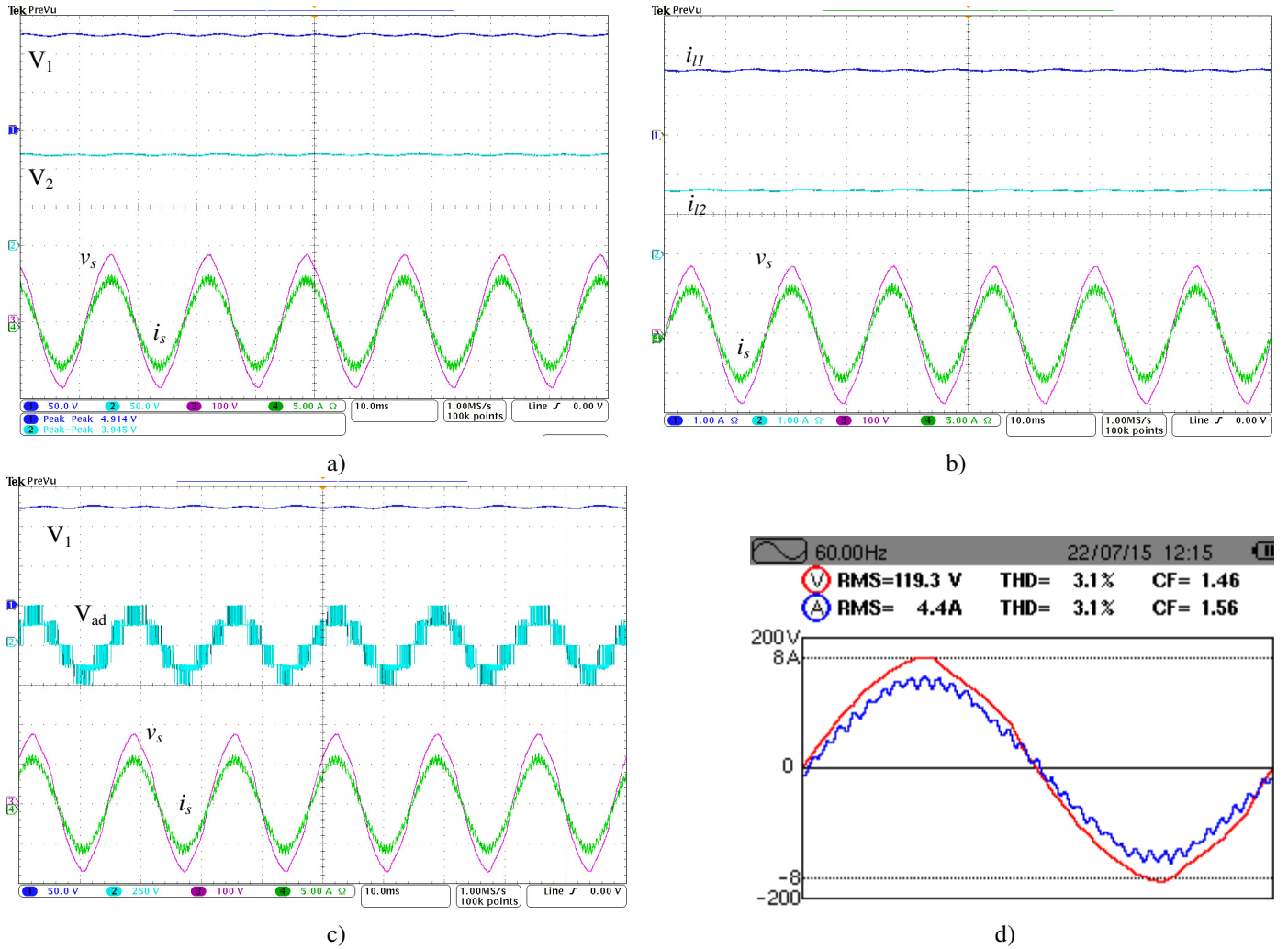|	
AC Grid Voltage	120 V RMS
AC Grid Frequency	60 Hz
Interface Inductor	2.5 mH
DC voltages (V_1&V_2)	125 V
DC Capacitors (C_1&C_2)	2500 uF
DC Load 1	53Ω
DC Load 2	80Ω
Switching Frequency	2 kHz
Current Controller Gains	$k_p = 0.8$, $k_i = 0.1$
Voltage Controller Gains	$k_p = 0.01$, $k_i = 5$

a)

b)

c)

d)

Fig. 9. Experimental results of the proposed HPUC rectifier connected to 120V RMS AC grid and supplying two DC loads at 125V DC. a) Output DC voltages regulated at 125V with grid side synchronised voltage and current b) DC loads currents with grid side synchronised voltage and current c) 5-Level voltage waveform at the input of the HPUC rectifier d) RMS and THD values of the AC side synchronised voltage and current waveforms

At first the steady state results are captured when the rectifier is converting 170V peak AC to 125V DC at two output terminals (in buck mode) and is supplying two loads with values mentioned in table III. All results including loads voltages/currents, grid voltage/current and rectifier input voltage in steady state is illustrated in figure 9. Figure 9-a shows the DC loads voltages regulated at 125V with acceptable voltage ripples (measured by scope at the bottom of the photo) as buck mode of operation. Loads currents are depicted in figure 9-b proportional to the DC voltages and loads impedances. Respectively, the 5-level waveform at V_{ad} is illustrated in figure 9-c which is made by regulated output voltages at desired level including 0, ±125V and ±250V. Since the maximum voltage is 250V, the whole system works as boost mode while it is split into two terminals with half voltage (125V) as buck mode of operation. Low switching frequency operation (2 kHz) is clear in that figure results in low power losses and high efficiency. The main objective of this paper is to demonstrate the HPUC topology performance as a multilevel buck PFC rectifier that are observed in figures 9-a and 9-c. Finally, figure 9-d has been captured by AEMC

power analyzer demonstrating RMS and THD values of the AC side voltage and current. The THD value of the current waveform is lower than standard limits while using a small inductive filter in AC line. The higher harmonic amplitude devotes to the 33rd order which is at the switching frequency (2 kHz) with 2.9% of the fundamental component. The active power delivered to the load equals to 525W and the power factor of the input AC voltage and current waveforms is almost 1 that ensures the unity power factor operation of the proposed multilevel buck rectifier with implemented voltage/current controller.

In continue, to validate the good dynamic performance of the voltage regulator integrated into switching sequences and adopted controller in driving the proposed buck PFC rectifier to supply DC loads at unity power factor, DC loads and input AC voltage are changed separately.

At first, the change has been intentionally made in $Load_1$. As it is clear from figure 10, two output DC voltages and $load_2$ current (i_{l2}) do not vary during change in $load_1$. DC voltages are regulated successfully as well as DC current reduction in

figure 10 proves the change in load$_1$ while the second load voltage/current is not affected remarkably.
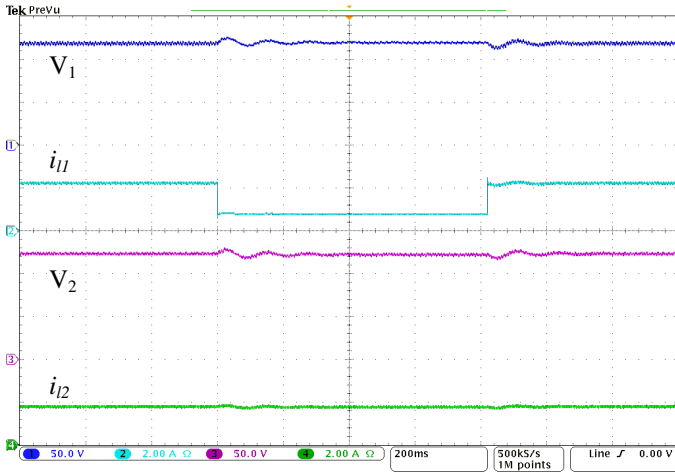

Fig. 10.   Test results during 200% increase in Load$_1$ from 53Ω to 160Ω

Similarly, a change has been made on second load to investigate the effects on the rectifier performance and the upper output DC terminal. In this case, load$_2$ is changed from 80Ω to 40Ω (50% decreases) and results are saved from both output terminals. Figure 11 includes captured waveforms of the load$_2$ that demonstrate changes in current during load reduction while the terminal voltage is fixed at 125V. Similar to the previous test, no effect is recorded on load$_1$ voltage/current during change in load$_2$.
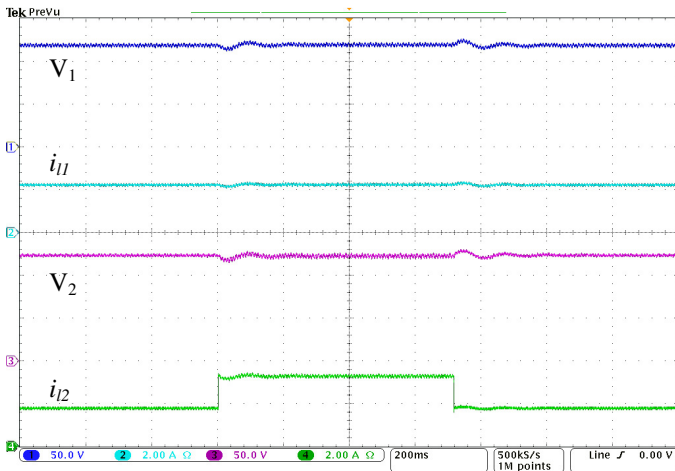

Fig. 11.   Test results during 50% decrease in Load$_2$ from 80Ω to 40Ω

Eventually, a test has been performed to validate the good dynamic performance of the proposed rectifier in unbalanced grid condition. Thus, since the rectifier is supplying loads, the input AC peak voltage is 25% increased from 162V to 200V (115V RMS to 142V RMS) and results confirm no influence on output DC voltages that are regulated at 125V DC.

Clearly seen in figure 12, during change in the input AC voltage, output DC voltages are successfully kept constant at reference level (125V) forming a 5-level quasi-sine wave at the rectifier input. Moreover, the input current is slightly decreased to balance the delivered power and prevent the load over-voltage and over-current issues.

Provided results in changing conditions prove the good dynamic performance of the proposed HPUC 5-level buck PFC rectifier in generating DC voltage from AC grid.
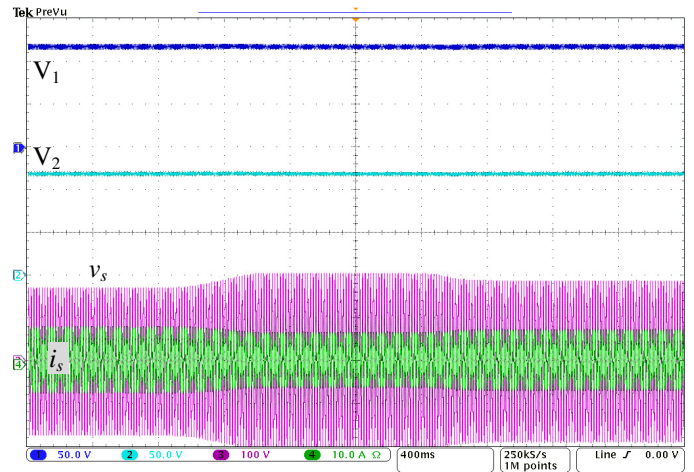

Fig. 12.   Supply voltage variation while the output DC voltages are regulated at 125V as buck mode of operation.

Provided results in changing conditions prove the good dynamic performance of the proposed HPUC bridgeless 5-level buck PFC rectifier in generating DC voltage from AC grid. It can be concluded that the HPUC topology can operate as a universal PFC rectifier in buck mode of operation at low switching frequency results in low power losses and high efficiency interesting for industrial applications.

VII. CONCLUSION

In this paper a 5-level rectifier operating in buck mode has been proposed which is called HPUC as a slight modification to PUC multilevel converter. It has been demonstrated that the proposed rectifier can deceive the grid by generating maximum voltage level of 250V at AC side as boost mode while splitting this voltage value at its two output terminals to provide buck mode of operation with 125V DC useable for battery chargers or telecommunication boards' feeder. Although it has more active switches than other buck rectifier topologies and some limitations on power balance between loads, overall system works in boost mode and CCM which results in removing bulky AC and DC filters that usually used in conventional buck PFC rectifiers. Moreover, generating multilevel waveform leads to reduced harmonic component of the voltage waveform and consequently the line current. It also aims at operating with low switching frequency and small line inductor that all in all characterizes low power losses and high efficiency of the HPUC rectifier. Comprehensive theoretical studies and simulations have been performed on power balancing issue of the HPUC rectifier. Full experimental results in steady state and during load and supply variation have been illustrated to prove the fact that HPUC topology can be a good candidate in a new family of buck bridgeless PFC rectifiers with acceptable performance. Future works can be devoted to developing robust and nonlinear controllers on the proposed rectifier topology.

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