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Wideband Cascaded and Stacked Receiver Front-Ends Employing an Improved Clock-Strategy Technique

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Abstract: A wideband cascaded receiver and a stacked receiver using an improved clock strategy are proposed to support the software-defined radio (SDR). The improved clock strategy reduces the number of mixer switches and the number of LO clock paths required to drive the mixer switches. This reduces the dynamic power consumption. The cascaded receiver includes an inverter-based low-noise transconductance amplifier (LNTA) using a feed-forward technique to enhance the noise performance; a passive mixer; and an inverter-based transimpedance amplifier (TIA). The stacked receiver architecture is used to reduce the power consumption by sharing the current between the LNTA and the TIA from a single supply. It utilizes a wideband LNTA with a capacitor cross-coupled (CCC) common-gate (CG) topology, a passive mixer to convert the RF current to an IF current, an active inductor (AI) and a $1/f$ noise-cancellation (NC) technique to improve the noise performance, and a TIA to convert the IF current to an IF voltage at the output. Both cascaded and stacked receivers are simulated in 22 nm CMOS technology. The cascaded receiver achieves a conversion-gain from 26 dB to 36 dB, a double-sideband noise-figure (NFDSB) from 1.4 dB to 3.9 dB, S_{11} <-10 dB and an IIP3 from -7.5 dBm to -10.5 dBm, over the RF operating band from 0.4 GHz to 12 GHz. The stacked receiver achieves a conversion-gain from 34.5 dB to 36 dB, a NFDSB from 4.6 dB to 6.2 dB, S_{11} <-10 dB, and an IIP3 from -21 dBm to -17.5 dBm, over the RF operating band from 2.2 GHz to 3.2 GHz. The cascaded receiver consumes 11 mA from a 1 V supply voltage, while the stacked receiver consumes 2.4 mA from a 1.2 V supply voltage.

Keywords: wireless receiver; wideband; cascaded; stacked; harmonic recombination; N-path receiver; LNTA

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1. Introduction

Wireless standards operate over a wide frequency spectrum spanning tens of GHz and employ various modulation schemes. Wireless applications have led to the rapid growth of wireless devices in all sectors of the internet of things (IoT), such as health monitoring, agriculture, and smart cities. A wideband system such as the software defied radio (SDR) is a well-suited architecture to address several wireless standards in a single receiver module. Conventional SDRs required a high specification analog-to-digital converters (ADCs), which increased the power consumption and complexity of the design [1] . In [2], down conversion is proposed to reduce the power consumption.

In wideband operation, the wanted signal at the local oscillator (LO) frequency down-converts to the baseband, along with other components of the LO harmonics. This degrades the error vector magnitude (EVM) performance. Harmonic recombination using the N-path receiver architecture is employed to overcome this problem [3–6]. One of the drawbacks of N-path receivers is that they require a high-frequency driving clock (e.g., 8× the LO frequency) to generate the clock phases that are needed to down-convert the signal at the desired LO frequency, and they reject the harmonics of the LO signal . Similarly, the

N-path passive mixer-first topologies that offer input matching without using external components and high-quality filtering can be used [7–9]. However, they consume high power to achieve a low noise figure (NF). In addition, mixer-first topologies are not suitable for wideband applications. An N-path ultra-low-power mixer-first receiver is presented in [10]. Although very low power consumption is achieved, it requires an off-chip inductor and achieves a low modulation bandwidth of 3.5 MHz. A feed-forward technique with tuned LO phase was employed in [11] to reject the LO harmonics. However, the phase-correction circuit increases the complexity of the design and reduces accuracy. A harmonic recombination technique that down-converts the signal at 3× the LO frequency is used in [12]. This technique removes all of the other harmonics at the LO frequencies such as the 1st, 2nd, 4th, and 5th harmonics. However, it consumes a significant amount of power in the baseband harmonic recombination circuitry. In addition, it uses a low noise transconductance amplifier (LNTA) with two inductors that occupy a relatively large area. Our earlier work [13] overcame the problems mentioned above. It employed a clock strategy technique to down-convert the signal at 4× the LO frequency while removing all of the other harmonics at the LO frequencies (i.e., 1st , 2nd, 3rd, 5th, 6th, and 7th harmonics). To reduce the power consumption, a current-reuse receiver topology was used. It employed the common-gate LNTA topology with a single to differential balun. In addition, an active inductor was used to improve the receiver sensitivity at higher RF. However, the clock strategy technique proposed in that prior work can be improved to reduce the mixer design complexity and the number of switches. In addition, the technique suffers from low-frequency noise due to the direct coupling of the LNTA noise to the output through the active inductor (AI).

To overcome the limitations mentioned above, this work proposes an improved clock strategy technique that reduces the number of mixer switches and the number of LO clock paths required to drive the mixer switches. This reduces the dynamic power consumption. The clock strategy technique down-converts an RF signal at 4× the LO frequency. The proposed clock strategy is verified through simulations in both cascaded and stacked receiver front-ends. In the cascade receiver front-end, very high RF bandwidth, low noise figure, and good linearity are achieved compared to the stacked receiver front-end at the cost of higher power consumption. The $1/f$ noise problem of [13] is resolved in this work by using a $1/f$ noise-cancellation (NC) technique. Current mode harmonic recombination is used to reduce the power consumption by avoiding the use of additional harmonic recombination circuitry.

The paper presents the clock strategy in Section 2, the cascaded receiver front-end design and its simulation results in Section 3, the stacked receiver front-end design and its simulation results in Section 4, and the comparison and discussion in Section 5. This is followed by a conclusion.

2. Clock Strategy Technique

The harmonic recombination technique has been used for wideband receiver front-ends to suppress the harmonics of the LO frequency that they down-convert to the baseband along with unwanted signals and noise. A harmonic rejection mixer using a parallel mixing path with a gain ratio of $1 : \sqrt{2} : 1$ is proposed in [14] to reject the third and fifth harmonics at the cost of using two frequency generator circuits that consume area and power. Another approach [15] achieved higher harmonic rejection using a digital adaptive-interference-cancelling (AIC) technique to enhance harmonic rejection. However, it requires high power. In addition, it requires 4× the LO frequency to generate 8-phase clocks to down-convert the signal at the LO. In [16], a 32-phase non-overlapping LO clock is used to achieve very good harmonic rejection (HR) after LO clock-phase calibration. However, it consumes 30 mW, and it requires harmonic selective TIAs, which increases the area and power consumption. Figure 1a shows the conventional harmonic recombination technique that down-converts a wanted signal at f_{LO} and rejects all of the LO harmonics (i.e., $2\times f_{LO}$, $3\times f_{LO}$, ..., where $f_{LO} = CLKIN/4$). This requires a CLKIN signal that is equal to 4×

of the LO frequency, increasing the complexity and power draw of the clock generation circuit, due to the high clock frequencies required. To overcome these issues, this work proposes a harmonic recombination technique, shown in Figure 1b, that employs a clock strategy to down-convert the wanted signal at $4 \times f_{LO}$ and reject signals at f_{LO}, $2 \times f_{LO}$, $3 \times f_{LO}$, $5 \times f_{LO}$ etc. For instance, using a CLKIN at 10 GHz, an RF input at 10 GHz is down-converted to baseband. This relaxes the requirements to design the LO clock generation circuits. Figure 1c shows the circuit diagram of the clock divider to generate 8-phase clocks (PH0, PH45, ..., PH316) for conventional harmonic recombination. OR-gates are used to combine the mentioned clocks to generate LO_1 and LO_2. The proposed clock strategy technique reduces the number of switches in the mixer to two in comparison to eight in the conventional harmonic recombination technique. This reduces the dynamic power consumption in the LO clock paths. In addition, the simplified LO routing on the chip reduces clock signal leakage to the substrate and improves signal integrity.

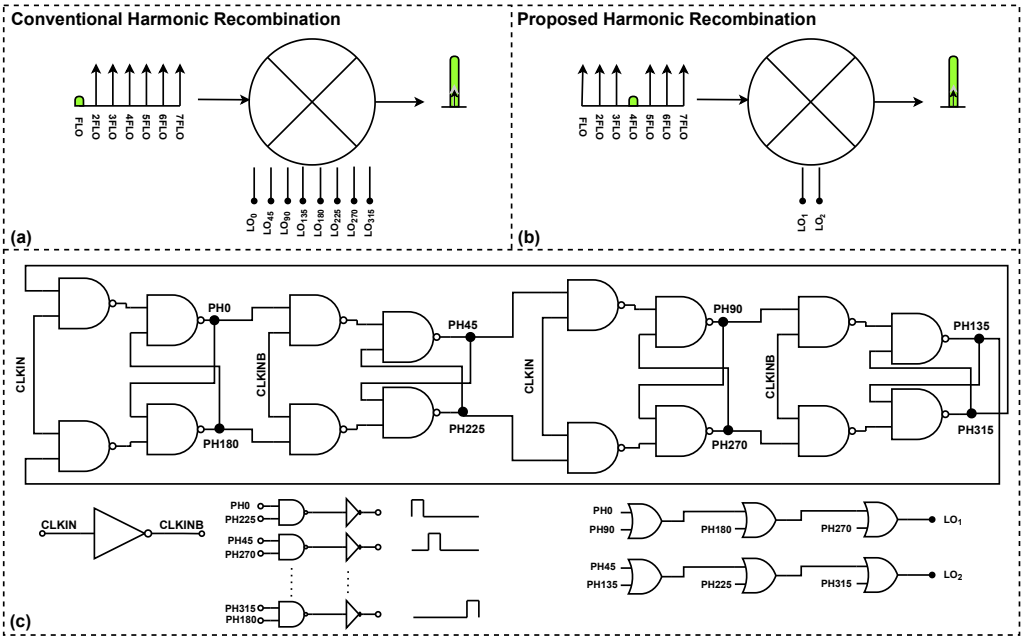

Figure 1. Harmonic recombination techniques: (**a**) cascaded approach, (**b**) stacked approach, and (**c**) clock generation circuitry.

To evaluate the proposed recombination strategy, the Fourier series coefficients are calculated using

$$\begin{cases} a_0 = \frac{2}{N}\sum_{k=1}^{N} s[k] \\ a_n = \frac{2}{N}\sum_{k=1}^{N} s[k].cos[\frac{2\pi}{N}nk] \\ b_n = \frac{2}{N}\sum_{k=1}^{N} s[k].sin[\frac{2\pi}{N}nk] \end{cases} \quad (1)$$

where N is the pulse period, k is the sample number, n is the harmonic number, and $s[k]$ is the signal given by

$$s[k] = \sum_{m=1}^{M} (-1)^m P_m[k] = \sum_{m=1}^{M} (-1)^m (u[k - \frac{(m-1)\pi}{4}] - u[k - \frac{m\pi}{4}]) \quad (2)$$

where $u[k]$ is the step function and M is the number of each shifted single pulses. The coefficients are calculated based on (1), where a_0 and a_n are zero for all harmonics, and b_n for harmonics $n = 4, 12, ..., 4(2i-1)$ is calculated by $\frac{16}{n\pi}$. Table 1 shows the calculated Fourier series coefficients of the proposed harmonic recombination technique for seven harmonics. It also presents the example scenario that a signal at 4 GHz is down-converted while the other LO harmonics are rejected.

Table 1. Fourier series coefficients of the proposed method.

b_n	b_1	b_2	b_3	b_4	b_5	b_6	b_7
Value (dB)	−Inf	−Inf	−Inf	2.2	−Inf	−Inf	−Inf
Freq. (GHz)	1	2	3	4	5	6	7

3. Cascaded Receiver Front-End Using the Proposed Clock Strategy

The functionality of the proposed harmonic recombination technique is verified using a cascaded receiver front-end architecture where the LNTA, passive mixer, and TIA are cascaded. Despite previous N-path receiver architectures that use complex and power-consuming circuits to combine the signals at the mixer output [4,17], the proposed receiver performs harmonic recombination in current-mode at the mixer output followed by a single TIA shown in Figure 2.

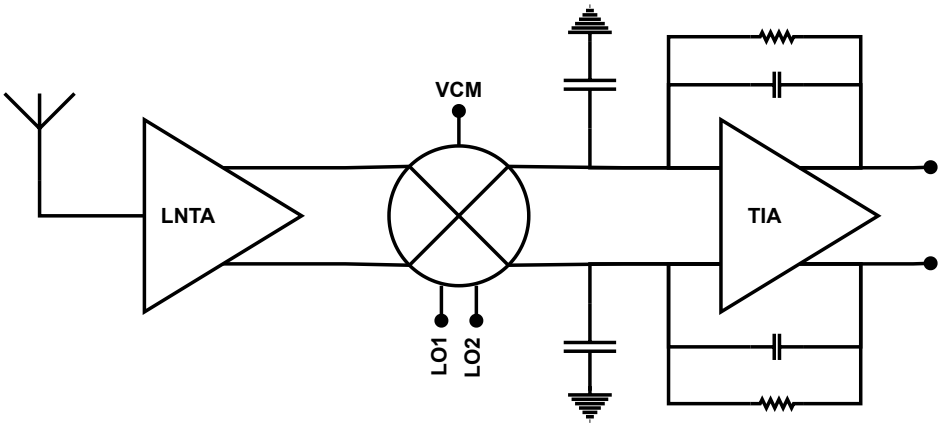

Figure 2. Cascaded receiver diagram.

3.1. LNTA Design

Conventionally, a wideband low noise amplifier (LNA) is used followed by a g_m-stage, down-conversion mixer and transimpedance amplifier (TIA). This helps reduce the NF but also amplifies blockers, which can saturate the following stages of the receiver[18]. The LNTA is an alternative that can be used to convert the RF voltage to an RF current that is then down-converted to the IF or BB current through a passive mixer. In this fashion, the receiver is not compressed by blockers due to the inherent low-voltage gain [15]. This work employs a low noise and wideband LNTA proposed in [19], shown in Figure 3.

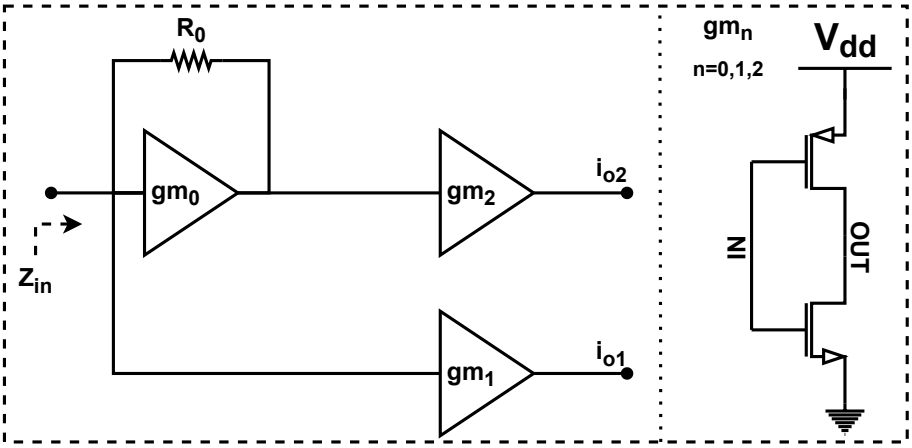

Figure 3. LNTA circuit diagram.

The first transconductance stage (gm_0) provides the input impedance matching, which is given by

$$Z_{in} \cong \frac{1}{gm_0}(1 + R_0/r_0) \tag{3}$$

where R_0 is the feedback resistor and r_0 is the output resistance of the gm_0 circuit.

Thanks to the feed-forward technique that provides noise-cancellation, the LNTA can achieve a low NF given by

$$NF \cong 1 + \frac{gm_2}{gm_1} + \frac{\lambda}{gm_1 R_s} \tag{4}$$

where λ is the short-channel effect coefficient, which can be reduced by increasing the transistor lengths. It can be seen the NF is independent of gm_0 and can be reduced by increasing the gm_1 value.

The total transconductance gain is approximated and given by

$$G_m \cong \frac{1}{2}\left[\left(\frac{gm_0 R_0 - 1}{1 + R_0/r0}\right)gm_2 + gm_1\right] \tag{5}$$

Transconductance gm_0 provides gate biasing for the gm_1 and gm_2 inverters along with bulk biasing of the PMOS and NMOS transistors since flip-well devices are used in a fully depleted silicon on insulator (FDSOI) CMOS technology. This reduces the area and parasitic capacitance of the AC-coupling capacitors at the input of gm_1 and gm_2.

3.2. Mixer Design

The mixer is responsible for down-converting the RF signal to the IF signal using the LO signal. There are two well-known mixer architectures: the passive and the active mixer. The passive mixer is preferred over the active mixer due to its high linearity performance yielded by the current-mode operation. In the passive mixer, switches are biased in a linear region. The gate of the switches are biased to make sure that the LO signal is able to turn on the mixer switches when it toggles between 0 V and the supply voltage. The circuit diagram of the mixer is shown in Figure 4. The mixer input is ac-coupled using a capacitor to separate the LNTA biasing and block low-frequency noise. The drain and source of the mixer switches are biased by the TIA common-mode voltage.

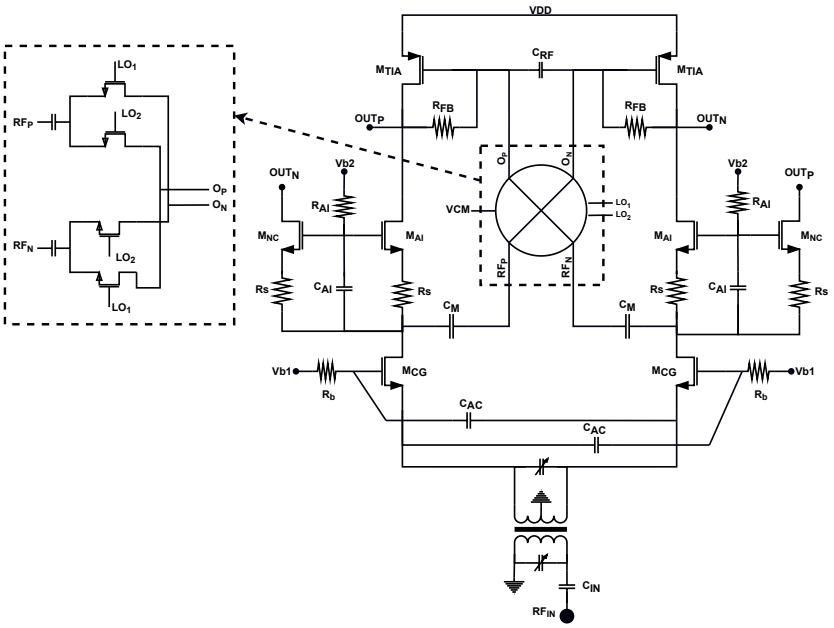

Figure 4. Stacked receiver circuit diagram.

3.3. TIA Design

The transimpedance amplifier (TIA) is used after the passive mixer to convert the IF current to an IF voltage at the output. In addition, it provides low-input impedance that improves the linearity. This work employs an inverter-based TIA using a feedback resistor to control the gain and a capacitor bank to define the IF bandwidth, shown in Figure 5. The current reuse inverter using both PMOS and NMOS enhances the overall transconductance without consuming extra power.

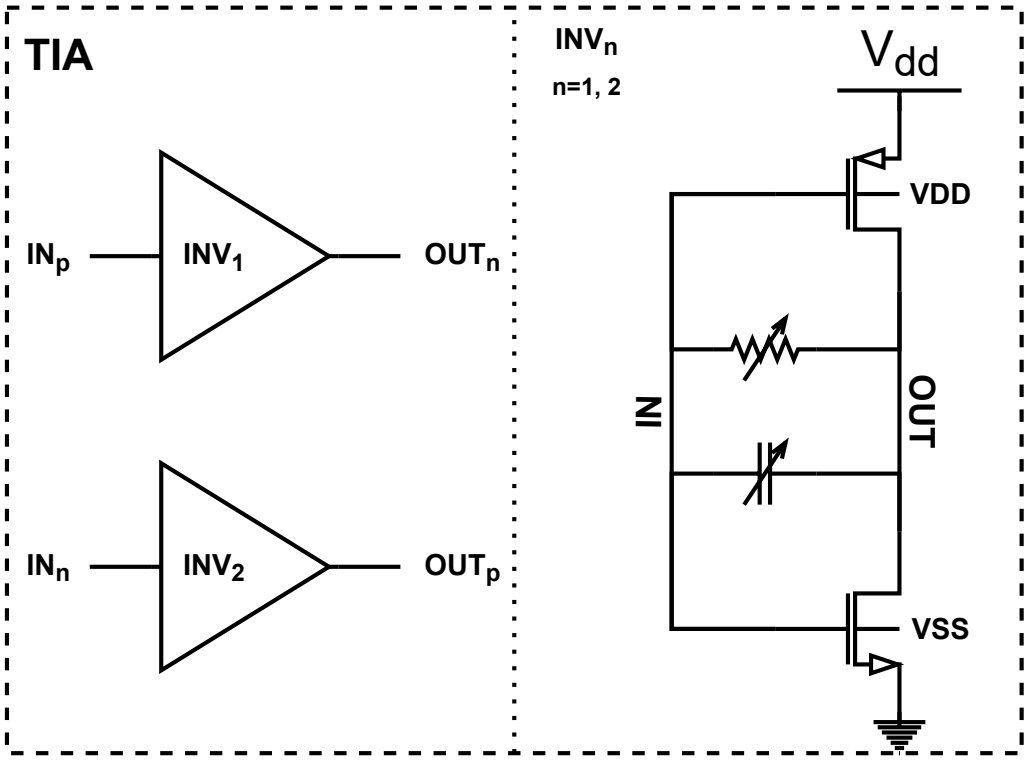

Figure 5. TIA circuit diagram.

The input impedance looking into the INV_n input is given by

$$Z_{in} = \frac{R}{g_m R_{out}} + \frac{1}{g_m} \tag{6}$$

where R is the feedback resistor and g_m is given by $g_{mp} + g_{mn}$.

The conversion-gain of the proposed receiver can be calculated as

$$CG \cong \frac{2}{\pi} \frac{Sin(\pi d)}{2d} g_m R_{FB} \tag{7}$$

where d is the clock duty-cycle that is 12.5% in this work.

3.4. Simulation Results of the Cascaded Receiver Front-End

The wideband receiver front-end using the clock strategy was designed and simulated in a 22 nm CMOS technology. The receiver consumes 11 mA from a 1 V supply voltage. The LNTA and TIA consume 4 mA and 7 mA, respectively.

The wideband input matching (S_{11}) of the LNTA is shown in Figure 6, showing an S_{11} of less than −10 dB at up to 13 GHz, which is suitable for ultra wideband applications.

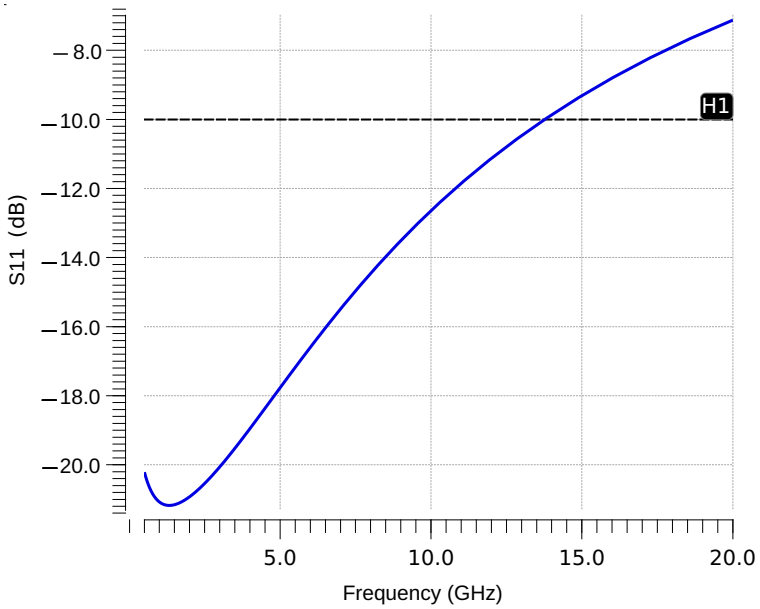

Figure 6. The cascaded received input matching (S11) performance versus RF.

The receiver-performance, integrated double-sideband noise-figure (NFDSB) from 10 kHz to 100 MHz, conversion gain and input-referred third-order intercept point (IIP3) versus f_{LO}, which is equivalent to an input RF signal having a frequency of $4 \times f_{LO}$, from 400 MHz to 12 GHz, is shown in Figure 7 . It shows the NFDSB is increasing in frequency from almost 1.4 dB to 3.9 dB. On the other hand, the conversion gain reduces from almost 36 dB to 26 dB as f_{LO} is increased. A constant value of feedback resistor is used in the TIA. To perform the IIP3 simulation, a two-tone signal at $4 \times f_{LO} + 10$ MHz and $4 \times f_{LO} + 11$ MHz is applied at the input of the LNTA. This generates two third-order intermodulation products at 9 MHz and 12 MHz along with two fundamental products at 10 MHz and 11 MHz. The IIP3 performance varies over f_{LO} from -10.5 dBm to -7.5 dBm.

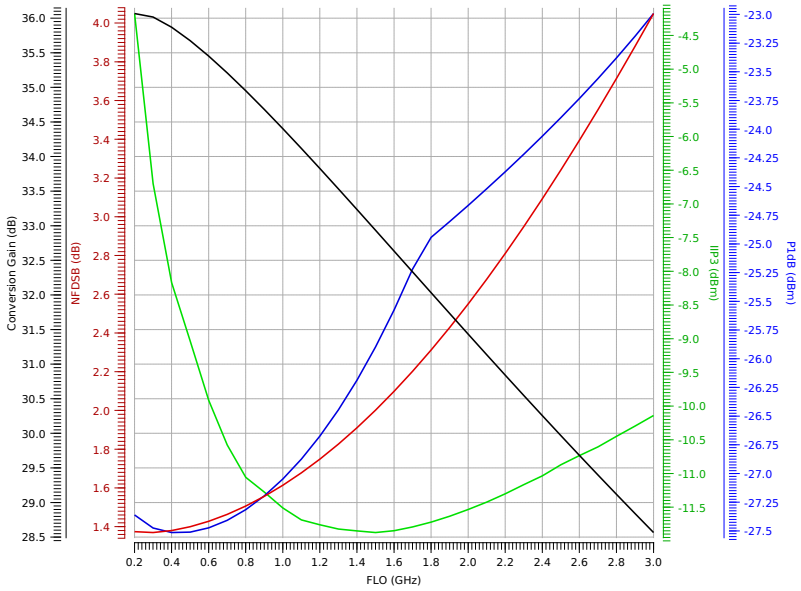

Figure 7. The cascaded receiver NFDSB, conversion gain, and IIP3 performances versus f_{LO}.

The TIA bandwidth can be configured with four settings using two capacitors. Figure 8 shows the receiver bandwidth can be configured from 250 MHz to almost 1 GHz. This can be changed using different values of feedback capacitors and also the shunt capacitors

after the mixer, which are 2 pF in this work. It shows that the receiver is suitable for very wideband baseband modulation.

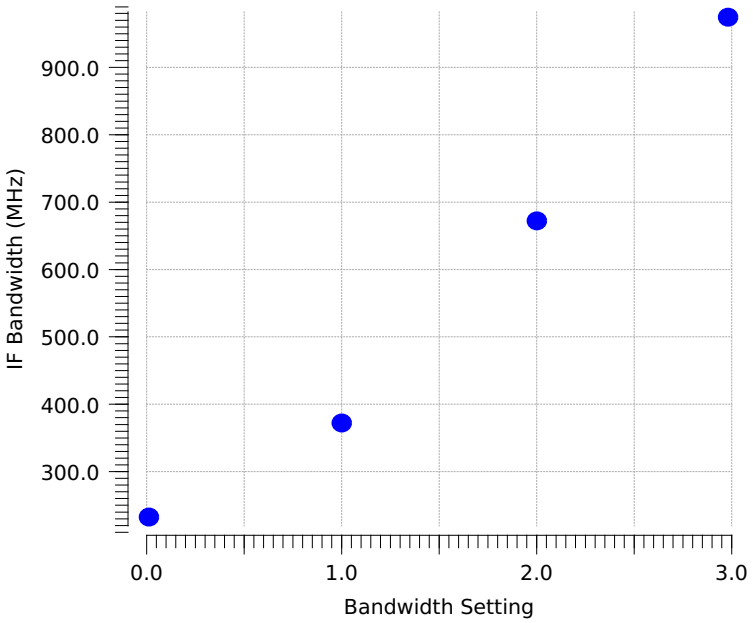

Figure 8. The cascaded receiver bandwidth versus the bandwidth settings.

The harmonic rejection can be affected by the transistor process and mismatch variations. The effect of the transistor process and mismatch variation is verified using Monte-Carlo simulation over 100 runs, and the results are shown in Figure 9. The HR1, HR2, ... HRn (n = 7) are the 1st, 2nd, ... nth harmonics rejected relative to the 4th harmonic, which is the wanted signal in this work. This shows that very good harmonic rejection is achieved at all harmonics with a minimum rejection of 134 dB in HR7 using a 3× sigma calculation.

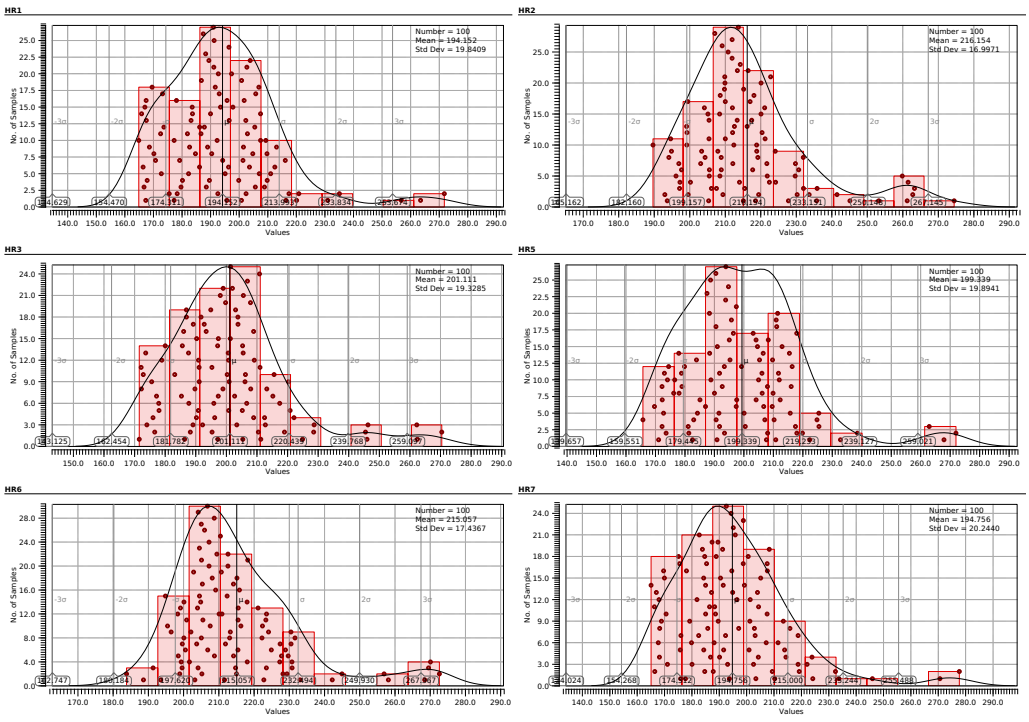

Figure 9. HR_n performance of the cascaded receiver over 100 runs.

4. Stacked Receiver Front-End Using the Proposed Clock Strategy

By scaling down the CMOS technology node , the threshold voltage (V_{TH}) is lowered, enhancing the frequency of operation and enabling new low-power design techniques that have emerged. One effective low-power design technique is the current-reuse or stacked technique by means of stacking different circuits such as LNTA, mixer, and TIA to share the biasing current from a single supply. Thus, in the stacked receiver front-end, the LNTA, mixer, and TIA are stacked.

Although this reduces power consumption, it still has drawbacks. The LNA, mixer, and voltage controlled oscillator (VCO) are staked in [20] to improve the power efficiency, but the circuit may suffer from the injection locking of the VCO due to the large blockers. Moreover, it has high NF. An unbalanced single to differential LNA, active mixer, and baseband circuitry are cascoded to reduce power consumption in [21]. However, the active mixer degrades the linearity performance and increases the voltage headroom requirements. A simultaneous input matching and $1/f$ NC technique is employed in [22] that results in a very low NF of less than 2 dB. However, the use of the common-source (CS) LNTA topology reduces the RF bandwidth. In addition, due to the receiver topology that connects the mixer input to the output node, the receiver is not able to operate at high frequency. Our earlier works [13,23,24], overcome the problems mentioned above. However, the mixer circuit in [13] needs to be improved to reduce the number of mixer switches. In addition, it suffers from $1/f$ noise that does not allow the receiver to operate at low frequency with good NF performance.

To overcome the limitations mentioned above, this work proposes a stacked receiver front-end, shown in Figure 4. It includes an on-chip balun to convert the single-ended antenna to a differential signal at the input of the LNTA, a capacitive cross-coupled common-gate (CG) LNTA topology to convert the RF voltage to an RF current, an active inductor (AI) and a $1/f$ noise-cancellation (NC) technique to isolate the mixer input and enhance low-frequency noise performance, a passive mixer to down-convert the RF current to an IF current, and a TIA to convert the IF current to an IF voltage at the output. The TIA and LNTA share the current using a single supply, reducing the power consumption.

4.1. LNTA Design

Two well-known LNTA topologies, common-gate (CG) and common-source (CS), can be used. The CS LNTA is suitable for very-low-noise applications at the cost of a narrow RF bandwidth. It is also very susceptible to non-idealities related to fabrication and packaging. On the other hand, the CG topology is used for wideband matching, and it is more reliable. The input impedance looking into the CG LNTA is 1/gm. Very high current and large device sizes are required to achieve the 1/gm = 50 Ω. To overcome this, a capacitor cross-coupled (CCC) technique is used to boost the effective g_m by two times without consuming extra power. It also improves the NF. The LNTA circuit is formed by M_{CG}, R_b, and C_{AC}. The noise factor of the LNTA is given by

$$F = 1 + \frac{\gamma}{R_S \times g_m}, \tag{8}$$

where R_S is the source impedance and γ is the short-channel effect coefficient, and can be reduced by increasing the transistor lengths.

4.2. Active-Inductor and $1/f$ Noise-Cancellation Design

In [22], the mixer input is connected to the output node. This increases the RF signal loss, and it does not allow the circuit to maintain its performance at high RF. To overcome this, the proposed AI circuit isolates the mixer input from the output. The impedance looking into the AI circuit is low at DC, while it increases at RF. In this case, the signal loss is then limited to parasitic capacitors. M_{AI}, C_{AI}, and R_{AI} form the AI circuit. The small R_s is used to boost the impedance at high frequencies with minimal impact at low frequencies. The impedance looking into the AI circuit is approximately given by

$$Z_{AI}(s) \cong \frac{g_{m,AI}R_S(R_{AI}C_{AI}s+1)+R_{AI}C_{AI}s}{g_{m,AI}R_SC_{AI}s+g_{m,AI}+C_{AI}s} || \frac{1}{sC_{par}}, \quad (9)$$

where C_{par} is the parasitic capacitance at the mixer input.

The stacked receiver front-end suffers from high low-frequency noise due to the direct coupling of the noise through the AI circuit. To overcome this issue, a $1/f$ NC circuit is formed by the M_{NC} transistors. It provides the signal path to the output with the opposite polarity to cancel the low-frequency noise and push the $1/f$ corner to a lower frequency. The functionality of the $1/f$ NC circuit is being verified in Figure 10. It shows the $1/f$ noise corner is pushed to a very low IF when the $1/f$ NC circuit is enabled, while the thermal noise remains almost constant.

4.3. TIA Design

The transimpedance amplifier (TIA) is used to convert the IF current to an IF voltage at the output. The TIA circuit is formed by transistors M_{TIA} and feedback resistors R_{FB}, where an additional harmonic recombination circuit is not required. The length of M_{TIA} should be large enough to enhance the output impedance. The conversion gain of the proposed stacked receiver can be calculated using Equation (7).

4.4. Simulation Results of the Stacked Receiver Front-End

The wideband stacked receiver front-end using a clock strategy was designed and simulated in a 22 nm CMOS technology. The receiver consumes 2.4 mA from a 1.2 V supply voltage.

The wideband input matching (S_{11}) of the LNTA is shown in Figure 11, showing an S_{11} of less than -10 dB over a wide frequency range by switching the capacitor bank at the input balun. The capacitor bank uses 16 binary weighted codes. The rest of the simulations in this work are verified using code 8.

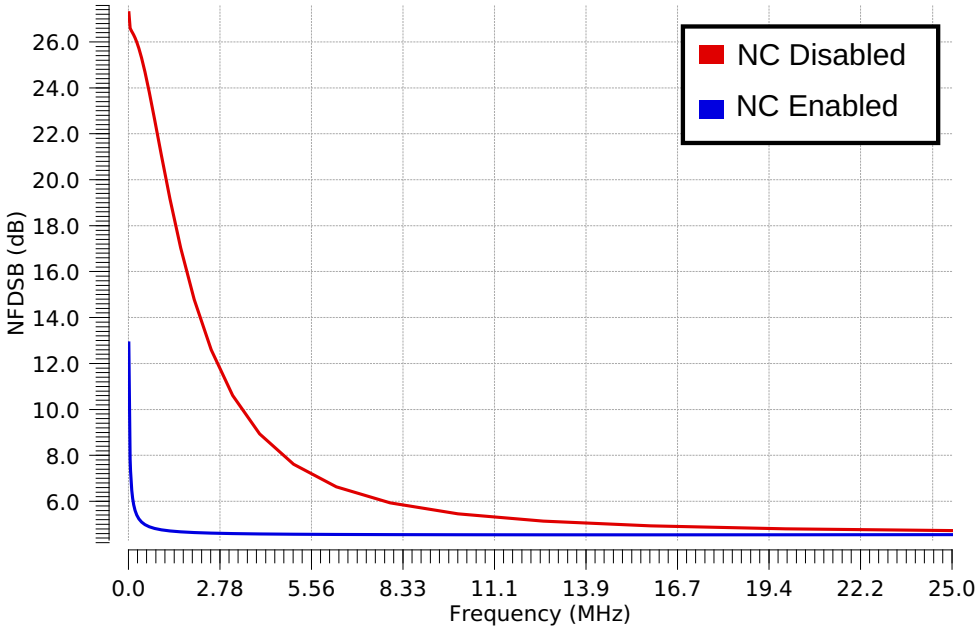

Figure 10. NFDSB of the stacked receiver with the $1/f$ NC circuit enabled and disabled.

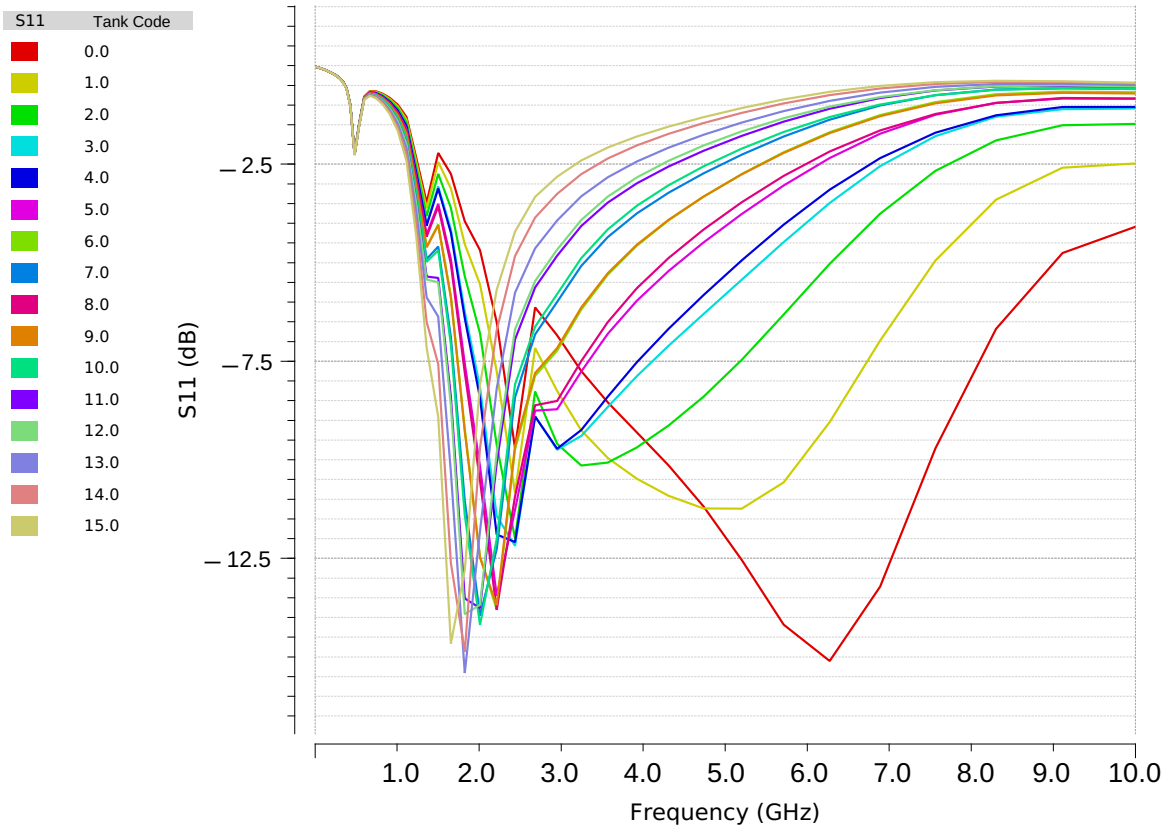

Figure 11. The stacked receiver input matching (S11) performance versus RF.

The receiver-performance, integrated NFDSB from 100 kHz to 50 MHz, conversion gain and input-referred third-order intercept point (IIP3) versus f_{LO}, which is equivalent to an RF input signal of $4 \times f_{LO}$, from 2.2 GHz to 3.2 GHz, is shown in Figure 12 . It shows that the NFDSB varies in terms of frequency from almost 4.5 dB to 6.3 dB. On the other hand, the conversion gain varies from almost 34.5 dB to 36 dB as f_{LO} is increased. A constant feedback resistor is used in the TIA. To perform IIP3 simulation, a two-tone signal at $4 \times f_{LO} + 10$ MHz and $4 \times f_{LO} + 11$ MHz is applied at the input of the LNTA. This generates two third-order intermodulation products at 9 MHz and 12 MHz, along with two fundamental products at 10 MHz and 11 MHz. The IIP3 performance varies over f_{LO} from -21 dBm to -17.5 dBm.

The harmonic rejection can be affected by transistor and layout mismatch. The effect of the transistor process and mismatch variation is verified using Monte-Carlo simulation over 100 runs, and the results are shown in Figure 13. The HR1, HR2, ... HRn (n = 7) are the 1st, 2nd, ... nth harmonics rejected relative to the 4th harmonic, which is the wanted signal in this work. The harmonic rejection in the stacked receiver front-end architecture is much less than the cascaded receiver architecture. The minimum rejection is achieved in HR5 with a 61 dB rejection using a $3\times$ sigma calculation.

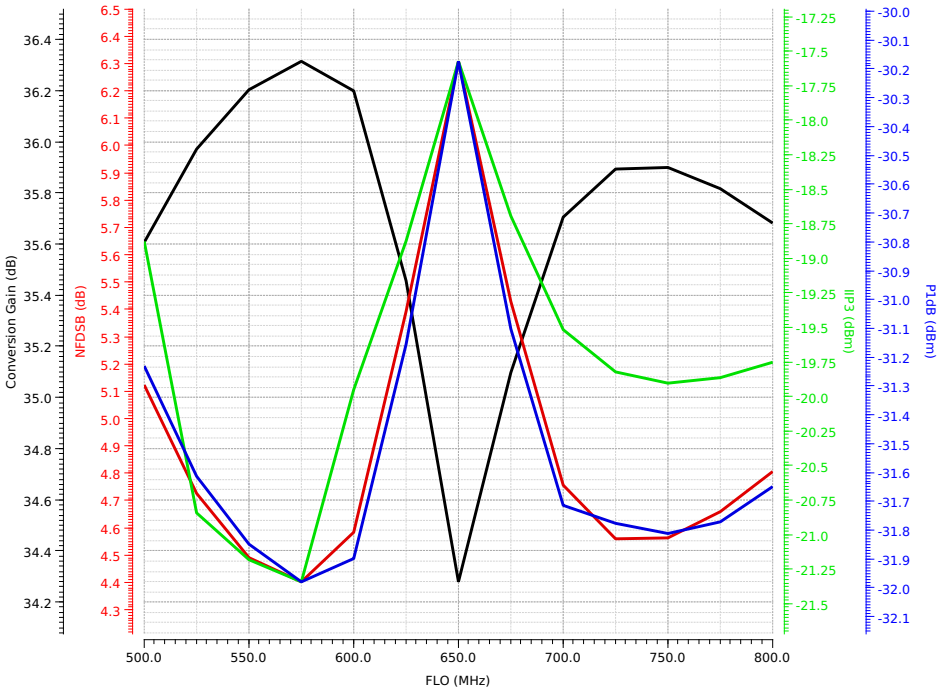

Figure 12. The stacked receiver NFDSB, conversion gain, and IIP3 performances versus f_{LO}.

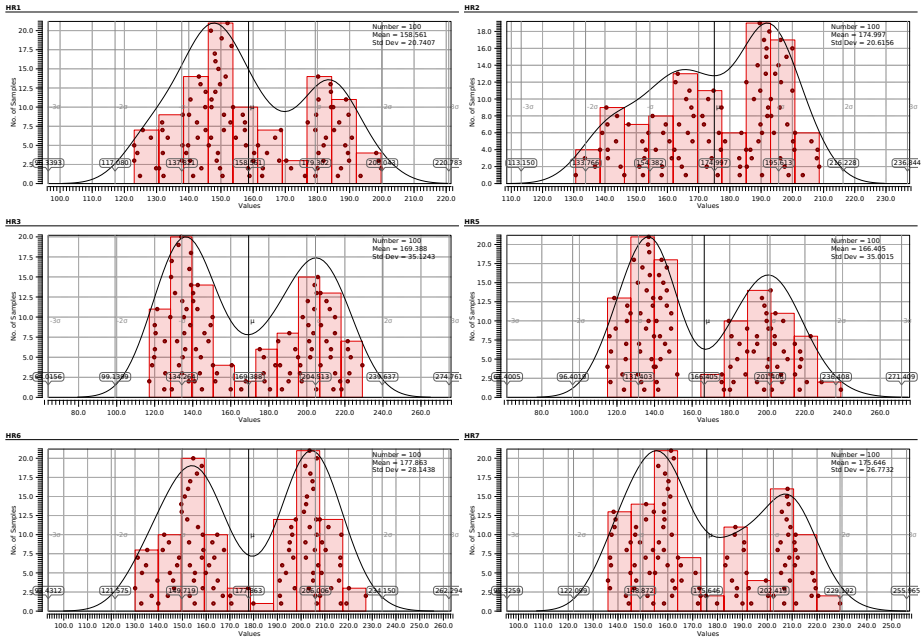

Figure 13. HR_n performance of the stacked receiver over 100 runs.

5. Discussion

Table 2 provides a performance summary and comparison of the cascaded and stacked receiver front-end using the clock strategy proposed in this work and compare them to the state-of-the-art. The cascaded receiver front-end with the clock strategy achieves a higher RF bandwidth, IIP3, and lower NF compared to the staked receiver front-end proposed in this work, while consuming almost four times current but operating at a slightly lower supply voltage of 1 V. The cascaded receiver architecture also achieved a higher RF bandwidth than work in [3,9,16] while consuming much lower power. Overall, both circuits presented in this work are suitable for wide modulation bandwidth application. The NF, IIP3, and bandwidth performance compare well with the state-of-the-art considering the power

consumption of the presented receivers. The harmonic recombination technique verified by both receiver architectures validates the viability of the technique for different receiver architectures. The minimum harmonic rejection ratio of the cascaded, stacked receiver, refs [3,4,12,16] are approximately 134, 61, 35, 51, 80, and 52 dB, respectively. The stacked receiver architecture is better suited to very low power wireless applications with relaxed performance requirements such as Bluetooth Low Energy, while the cascaded receiver architecture can be used for a wide range of higher performance applications.

Table 2. Performance summary and comparison.

Parameters	**This Work Cascaded** ⊖	**This Work Stacked** ⊖	[12] ⊖	[4] ⊕	[16] ⊕	[10] ⊕	[9] ⊕	[3] ⊕
Process node	22 nm CMOS	22 nm CMOS	65 nm CMOS	65 nm CMOS	28 nm CMOS	28 nm CMOS	65 nm CMOS	28 nm CMOS
Freq. (GHz)	0.4–13	2–6	5.7–7.2	0.15–0.85	0.5–3	1–2	0.5–2	0.1–3.3
S11 (dB)	<-10	<-10	<-10	<-10	<-10	<-10	<-10	N/A
Gain (dB)	26–36	34.5–36	36.4	51	42	29.4	36	N/A
NF (dB)	1.4–3.9	4.6–6.2	4.4	5.4	2.4–5	5.7	2.2–4.2	1.7
IIP3 (dBm)	-10.5–7.5	-21–17.5 *	-18.9 *	-12 *	4^{+}	-10 *	-11 *	11.5^{+}
P_{DC}	11	2.9	13	7.5	21	0.141	41–65	36.8–62.4

* In-band IIP3 $^{+}$ out-of-band IIP3; ⊕ measurement results; and ⊖ simulation results.

6. Conclusions

Wideband cascaded and stacked receiver front-ends employing a clock strategy to down-convert an RF signal at 4× the f_{LO} frequency were designed in a 22-nm CMOS process for SDR applications. The simulation results are presented showing the benefits of both architectures. The cascaded receiver front-end achieved higher bandwidth, lower NF, and better linearity performance than the stacked receiver front-end at the cost of higher power consumption. In the cascaded receiver front-end, low NF was achieved thanks to the feed-forward noise cancelling technique of the LNTA. The LNTA used by the cascaded receiver front-end operates over a frequency range from 0.4 GHz to 13 GHz. In the stacked receiver front-end, the low power consumption was achieved by sharing the current between the TIA and the LNTA using a single supply. The noise performance was also improved by using an AI and $1/f$ noise-cancellation technique.

Thanks to the current mode harmonic recombination, both receivers do not require additional circuits for harmonic recombination, reducing the power consumption. Dynamic power consumption is ultimately reduced thanks to the clock strategy technique that down-converts an RF signal at $4 \times f_{LO}$, reducing the clock frequency requirements. In the stacked receiver architecture, the CCC technique boosts g_m by two times without consuming additional power. The LNTA and balun can be tuned over an input frequency range from 2 GHz to 6 GHz.

The wideband operation and performance metrics of the proposed front-ends make them very suitable for SDR receivers that require a wideband frequency response and good harmonic rejection performance.

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Abbreviations

The following abbreviations are used in this manuscript:

ADC	Analog-to-digital converter
AI	Active inductor
AIC	Adaptive interference cancelling
CG	Common-gate
CCC	Capacitor cross-coupled
CMOS	Complementary metal–oxide semiconductor
CS	Common-source
ÉTS	École de technologie supérieure
FDSOI	Fully depleted silicon on insulator
HR	Harmonic rejection
IF	Intermediate frequency
IIP3	Third-order intercept point
IoT	Internet of things
LNA	Low-noise amplifier
LNTA	Low-noise transconductance amplifier
LO	Local-oscillator
NF	Noise figure
NC	Noise cancellation
NFDSB	Double side-band noise figure
RF	Radio frequency
SDR	Software-defined radio
TIA	Transimpedance amplifier
VCO	Voltage-controlled oscillator
V_{TH}	Voltage-threshold
g_m	Tranconductance

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