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Input Resistance Boosting for Capacitive Biosignal Acquisition Electrodes

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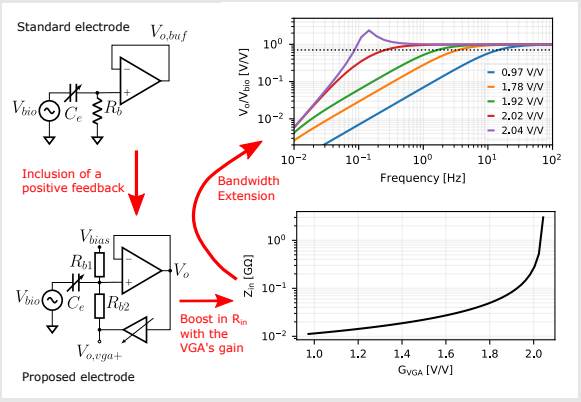
***Abstract*— Capacitive electrodes are a promising alternative to conventional wet Ag/AgCl electrodes in the acquisition of biological signals. They consist of a metallic sensing layer covered by an insulating material that contacts the human body. They have the advantage of measuring biopotentials in humans through clothing, hair, and small air gaps. The electrode capacitance creates a high-pass filter with the analog front-end's input resistance. Hence, the bandwidth of the system, especially the low cut-off frequency, depends on the dielectric layers and the characteristics of the body-electrode contact. Moreover, capacitive electrodes suffer from motion artifacts (MAs) that also modify the electrode capacitance. This paper proposes an electrode topology with boosted input resistance and compensation for the electrode capacitance changes. To achieve such characteristics, the proposed circuit comprises a negative impedance converter that increases the input resistance, which allows the addition of a capacitor in series with the electrode capacitance to reduce the effects of capacitance changes. The proposed electrode's cut-off frequency was investigated in a controlled test bench. For the worst-case scenario of electrode capacitance (1 pF), the proposed topology achieved a cut-off frequency of 1.5 Hz while the reference circuit had a cut-off frequency of 72 Hz. The proposed topology also outperformed the reference electrode in common-mode rejection ratio (CMRR) and through clothing ECG acquisition.**



Keywords: Biopotential, Capacitive Electrodes, ECG

I. Introduction

BIOPOTENTIAL monitoring is an essential tool in modern medicine. Electroencephalography (EEG), Electromyography (EMG), and Electrocardiography (ECG) allow physicians to assess the health of the brain, muscles, and heart, respectively [1]. These techniques measure the difference of potential between distinct points on the human body, with each point connected to the measuring device through an electrode. The acquired signals are then compared to reference waveforms to diagnose diseases or evaluate the health of a patient.

The common aspect of these methods is the electrode. Generally, the disposable Ag/AgCl electrode with conductive gel is the preferred choice, because it provides high-quality and reliable signals at a low cost. Yet, this kind of electrode has the disadvantage of requiring direct contact with the skin, the presence of a professional to attach it to the patient, skin reactions such as allergies and irritation, and decreased performance during long-term monitoring due to the gel drying out [2], [3]. Moreover, such devices are normally located at medical facilities and are not available for the general public use.

To overcome these limitations, researchers shifted their focus to dry electrodes, which could be integrated into daily life objects such as beds and car seats or wearable devices [4]. Here, we focus on the capacitive type: an active dry electrode formed by a sensing surface (commonly the bottom layer of a printed circuit board (PCB)), a fixed dielectric such as the PCB's solder mask, changeable dielectric (air, hair, clothing) and the patient's body [5].

Under ideal operating conditions, capacitive electrodes provide the necessary bandwidth with unitary gain and can replace the standard wet electrode. In this situation, the electrode is modeled as a capacitor (C_e) of hundreds of pF which interacts with the amplifier's input impedance. However, the electrode capacitance depends on the contact characteristics, such as the fabric of the person's clothing, pressure, air gaps, and area. Further, the capacitive electrodes do not stick to the skin and the patient's movements lead to disturbances, called motion artifacts (MAs) [6].

MAs can be split into two problems [7]. One is the change in C_e due to a change in pressure or the creation of air gaps [8]. The other is the accumulation of static charges in the electrode's surface due to triboelectricity, which leads to large voltages that may saturate the input [9]. In this paper, for simplicity, the decrease of C_e is called the "capacitance artifact" and the large triboelectric voltage is referred to as the "voltage artifact".

The low cut-off frequency of a capacitive electrode is given by a high-pass RC filter formed by C_e and the electrode's input

resistance (R_{in}). Therefore, as C_e changes, due to different layers of clothing, pressure, and MA, so does the cut-off frequency. For an ambulatory ECG the low cut-off frequency requirement is $0.5\,\mathrm{Hz}$ (or $0.67\,\mathrm{Hz}$) and for diagnostic ECG it is $0.05\,\mathrm{Hz}$. The electrode capacitance ranges from $1\,\mathrm{nF}$ and $1\,\mathrm{pF}$. Hence, the input resistance must be as high as $3.2\,\mathrm{T\Omega}$ for diagnostic ECG.

The requirement of ultra-high input resistance is challenging [10]. In discrete designs, ultra-high resistors exist and can properly bias the amplifier's input. However, they are expensive and inaccurate. The bootstrapped bias circuit can boost the bias resistance and has been widely reported [11]. In integrated designs, pseudo-resistors provide ultra-high resistances, and if needed, they can be included within a bootstrapped bias circuit [12]. However, the bootstrapped bias circuit cannot compensate for the operational amplifier's input resistance and the short-channel gate leakage in short-channel transistors. Positive feedback is also commonly used to improve the input impedance of integrated designs, such as in chopper amplifiers and similar structures [13], [14].

According to [15], low-frequency common-mode signals lead to artifacts many times larger than the actual ECG signal for electrodes with mismatched low cut-off frequencies ($0.25\,\mathrm{Hz}$ and $0.4\,\mathrm{Hz}$). A common design strategy in capacitive electrodes is selecting the input resistance according to the minimum C_e expected to ensure enough bandwidth. Then, each channel (or the differential signal) passes through a high-pass filter to remove artifacts in the extra/excessive frequency band. However, in this design technique, each electrode input node possesses a slow time constant when the electrode capacitance is high. For example, if C_e is $1\,\mathrm{nF}$ and R_{in} (R_b) is $320\,\mathrm{G\Omega}$ in Fig. 1a, the time constant τ is $320\,\mathrm{s}$. Therefore, a large MA can saturate the amplifier's input and the electrode's signal becomes unavailable for a long period. To quickly discharge the input node, two options are available: adding a controlled switch to the input node (adds an extra I/O) or diode-based circuits (clipping for signals greater than the forward voltage).

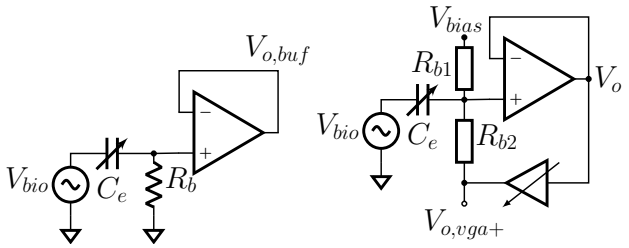
In this paper, we demonstrate the design of an analog front-end (AFE) for capacitive electrodes with optimized cut-off frequency stability. First, the input resistance is boosted by a negative impedance converter (NIC). It is shown that this technique works in both transistor-level and discrete designs. The boosted input resistance allows the inclusion of a small capacitor (C_s) in series with C_e to reduce the fluctuations of the low cut-off frequency. Furthermore, we propose modifications to the bootstrapped bias circuit to reduce the MA detection range and improve linearity.

The paper is organized as follows. Section II introduces the proposed techniques to boost the input resistance and the circuit design. Section III presents and discusses the simulation and measurement results. The circuit based on transistors used the TSMC 65 nm technology and the results were obtained from post-layout simulations. The measured circuit relied on discrete components. The conclusions are drawn in Section IV.

II. Development

The equivalent impedance formed between the sensing layer and the surface of the human skin is modeled as a pure capacitance C_e. In the schematics displayed in this section, the signal source V_{bio} represents the biopotential measured by a single electrode.

The simplest AFE (base circuit) that allows the measurement of biological signals from the human body through a capacitive interface is displayed in Fig. 1a [16]. It consists of an op-amp in a buffer configuration and a bias resistor (R_b). Internally, the op-amp contains input resistances ($R_{in,op}$) and input capacitances ($C_{in,op}$), connected from each input to the circuit's ground, which are not shown in Fig. 1a.



(a) Base circuit (b) Simplified proposed circuit

Fig. 1: Simplified circuit schematics

The op-amp's input requires a path to ground to allow the flow of a bias current [4]. $R_{in,op}$ is usually too high to provide this current, hence a bias resistor (R_b) in parallel is required. By assuming that the overall input resistance (R_{in}) is $R_{in,op}||R_b$, that the buffer has unity closed-loop gain, and that the total input capacitance is C_{in}, the transfer function from V_{bio} to $V_{o,buf}$ is:

$$\frac{V_{o,buf}}{V_{bio}} = \frac{C_e}{C_e + C_{in}} \times \frac{s}{s + \dfrac{1}{R_{in}(C_{in} + C_e)}} \tag{1}$$

the midband gain is:

$$\left|\frac{V_{o,buf}}{V_{bio}}\right|_{\text{Midband}} = \frac{C_e}{C_e + C_{in}} \tag{2}$$

and the buffer's cut-off frequency ($f_{c,buf}$) is:

$$f_{c,buf} = \frac{1}{2\pi R_{in}(C_{in} + C_e)} \tag{3}$$

The circuit presents a high-pass behavior. The cut-off frequency (3) depends on R_b, C_{in} and C_e while the midband gain (2) is a simple capacitive voltage divider between C_e and C_{in}. Voltage division is minimized if C_{in} is much smaller than C_e. In this condition, $f_{c,buf}$ can be approximated as $1/2\pi R_{in} C_e$.

A. Conductance Neutralization

A simplified schematic of the proposed circuit is shown in Fig. 1b. It comprises an operational amplifier in voltage follower configuration, two resistors at the non-inverting input, and a variable gain amplifier (VGA) with gain G. The electrode capacitance is represented by C_e and the voltage that is meant to be sensed is V_{bio}.

The electrode capacitance blocks DC currents flowing from the amplifier to the body, hence, the resistor R_{b1} sets the

input DC voltage to V_{bias}. The VGA creates positive feedback through R_{b2}. For simplicity, it is assumed that $R_{in,op}$ is too large to bias the input, hence $R_{in,op}||R_{b1} \approx R_b$. Moreover, to simplify the equations, it considered that $R_{b2} = R_b$. In a proper design, $C_{in} << C_e$ to avoid voltage division according to (2), thus C_{in} is neglected and the transfer function for the circuit in Fig. 1b is (4).

$$\left.\frac{V_o}{V_{bio}}\right|_{R_{b1},R_{b2}=R_n} = \frac{s}{s + \dfrac{2-G}{C_e R_b}} \tag{4}$$

By inspecting (4), an expression for the overall input resistance is reached (5).

$$R_{in} = \frac{R_b}{2-G} \tag{5}$$

When the VGA's gain (G) is 0, R_{in} is $R_b/2$ (the parallel of R_{b1} and R_{b2}), however, as G increases closer to 2, the input resistance tends to infinity. Increasing the gain further than 2 may lead to oscillation due to excessive positive feedback, which moves the closed-loop pole to the right-half plane. It is also necessary to know the transfer function from the bias voltage to the output (6).

$$\left.\frac{V_o}{V_{bias}}\right|_{s=0} = \frac{1}{2-G} \tag{6}$$

In dual supply circuits V_{bias} can be set to 0 V, though modern applications are trending to low-voltage single-supply circuits which presents constraints regarding the bias voltage range. Equation (6) shows that the gain applied to V_{bias} is proportional to the boosting factor applied to R_{in}. Moreover, any noise coming from the bias voltage is amplified.

B. Transistor-level design

A block diagram of the proposed CMOS circuit is shown in Fig. 2. It consists of a low input capacitance buffer and a VGA with common-mode control and low-pass filter negative feedback. The transistor-level schematic of the buffer is shown in Fig. 3 and the VGA with its auxiliary circuits is depicted in Fig. 4

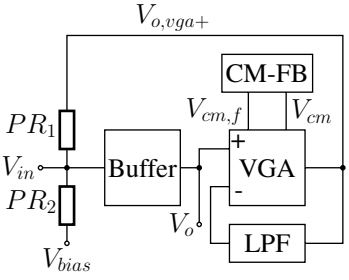


Fig. 2: Block diagram of the proposed CMOS circuit

The buffer used here was the one proposed by [12] and shown in Fig. 3. This topology reduces the gate stray capacitances, which leads to negligible voltage division between the electrode capacitance and the input capacitance. It consists of a telescopic cascode op-amp with unity gain feedback, whereas the output also drives the cascode devices ($M_{d,1c}$ and $M_{d,2c}$) and the bodies of all transistors in the differential pair are connected to the tail current source's output (drain of $M_{t,1c}$). Hence, the stray capacitance (C_{gd}, C_{gs} and C_{gb}) of M_{d1} are bootstrapped.

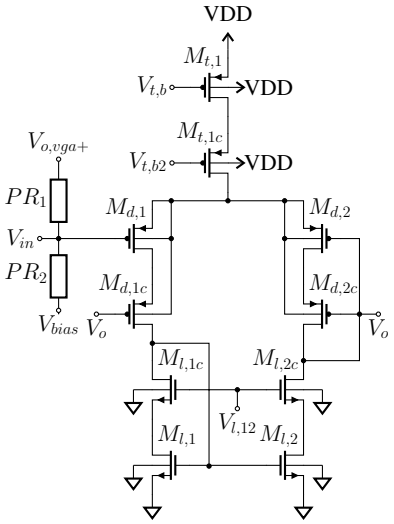


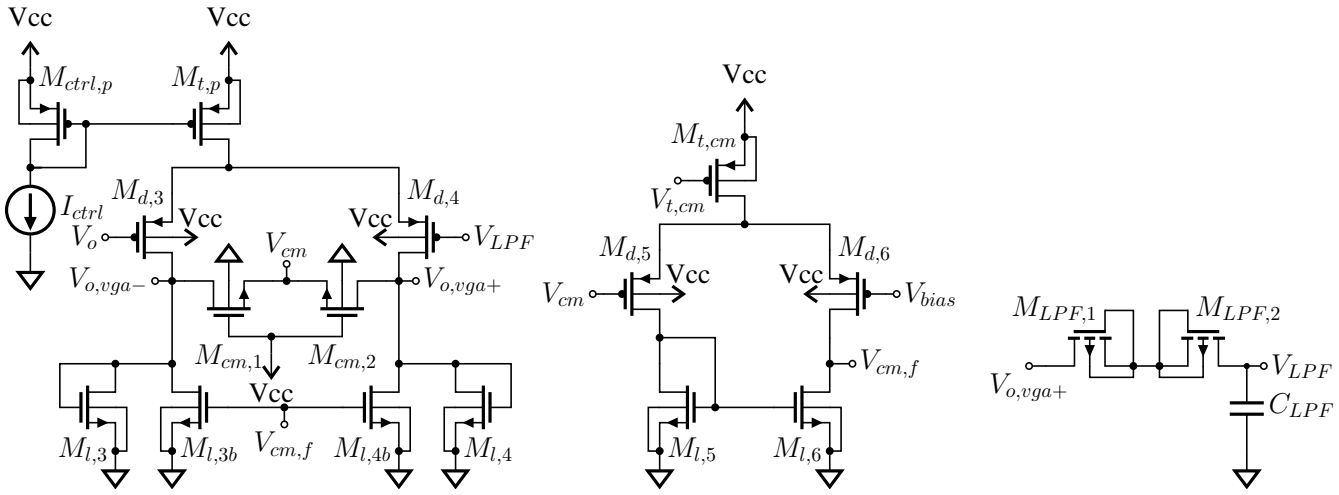
Fig. 3: Bootstrapped buffer

The bias resistors are implemented with pseudo-resistors such as the ones used in [17]. Pseudo-resistors attract the attention of the bio-amplifier community because they can be simply implemented with 1 or 2 transistors while providing very high resistance [18]. In recent years, the acceptance of pseudo-resistors has grown as researchers proposed improvements, such as enhancing their linearity and PVT sensitivity and making their resistance controllable [19].

The VGA's core is shown in Fig. 4a and consists of a PMOS differential pair, where the gain is controlled by the tail current. This control current is copied from an external current source by a current mirror, implemented with $M_{ctrl,p}$ and $M_{t,p}$. The differential pair's non-inverting input receives the input buffer's output (V_o). Two NMOS transistors, operating in the triode region, measure the common-mode signal (V_{cm}), which is amplified by a single-ended differential pair shown in Fig. 4b.

The load of the VGA comprises a diode-connected NMOS ($M_{l,3/4}$) in parallel with an active load that receives the common-mode feedback ($M_{l,3b/4b}$). Because the targeted gain is lower than 2, which is a relatively small gain, one can use diode-connected devices as the dominant load. That is, the diode-connected device presents an apparent resistance of $1/gm$, which is much smaller than the apparent resistance r_o of the current source loads.

The pseudo-resistors' (R_{b1} and R_{b2}) linearity range is small ($\approx 50\,\mathrm{mV}$), hence the DC component in the VGA's output ($V_{o,vga+}$) must be equal to V_{bias}. The common-mode feedback is essential to even out the voltage drop in both pseudo-resistors. The inverted and amplified common-mode signal ($V_{cm,f}$) controls the amount of current in the active loads ($M_{l,3b}$ and $M_{l,4b}$) and forces the current in the diode-connect loads ($M_{l,3}$ and $M_{l,4}$) to be constant. Moreover, if the amount of current in the dominating load is constant, so is the apparent resistance ($1/gm$). Consequently, changing the tail current



(a) Fully differential amplifier (b) Common-mode feedback (c) Feedback filter

Fig. 4: Positive feedback network circuitry with variable gain. a) Fully differential amplifier with controllable gain b) a differential pair to amplify and feedback the common-mode, controlling the DC level on the VGA's output c) a feedback filter used to control the VGA's frequency response

modifies the differential pair's gm but not the load resistance.

Because the VGA's input is a sensed signal, it can be contaminated with large low-frequency artifacts. Thus, to avoid differential amplification of these signals and unmatched DC bias, the low-pass filter network shown in Fig. 4c forms a negative feedback between $V_{o,vga+}$ and V_{LPF}. This filter defines the bandwidth of the VGA, and hence limits the bandwidth where R_{in} is boosted. The VGA's gain ($V_{o,vga+}/V_o$) without the feedback filter (open-loop) is named G'_{VGA}, while the gain with the feedback filter is G_{VGA}, and the equation that connects both is (7).

$$G_{VGA} = \frac{G'_{VGA}(1 + sC_{LPF}R_{LPF})}{G'_{VGA} + 1 + sC_{LPF}R_{LPF}} \tag{7}$$

Replacing G in (5) with (7), an equation for R_{in} with the frequency response is found:

$$R_{in} = \frac{R_b}{2 - G'_{VGA}} \times \frac{s + (G'_{VGA} + 1)\omega_{LPF}}{s + \frac{(G'_{VGA} + 2)\omega_{LPF}}{2 - G'_{VGA}}} \tag{8}$$

G'_{VGA} is expected to be between 1 and 2, thus the pole in (8) is at a higher frequency than the zero. As G'_{VGA} gets closer to 2, the pole frequency increases with a factor $1/(2-G'_{VGA})$. In low frequencies, R_{in} is approximately $R_b/2$ while in high frequencies it is $R_b/(2 - G'_{VGA})$. One should notice that contrary effects are taking place, as both the value of R_{in} in the pass-band and the pole frequency increase with $1/(2-G'_{VGA})$. This means that the design of the feedback filter should consider the largest boost factor ($1/(2 - G'_{VGA})$), to ensure that the desired R_{in} is achieved before the electrode's cut-off frequency (given by $1/2\pi C_e R_{in}$). Replacing the input resistance with the frequency behavior (8) in (4), the transfer function V_o/V_{bio} is updated to (9):

$$\frac{V_o}{V_{bio}} = \frac{s[s + (G'_{VGA} + 1)\omega_{LPF}]}{\left\{s^2 + s\left[\frac{2 - G'_{VGA}}{C_e R_b} + (G'_{VGA} + 1)\omega_{LPF}\right] + \frac{(G'_{VGA} + 2)\omega_{LPF}}{R_b C_e}\right\}} \tag{9}$$

The zero at the origin with two poles forces a high-pass filter behavior. However, as G'_{VGA} changes, the other zero and the two poles move. Thus, the frequency response can change from overdamped to maximally flat, underdamped or oscillatory behavior. The values of the poles are obtained from the denominator of (9). A condition for stability is reached by simplifying the poles' expressions and conditioning them to be at the left-half plane:

$$(G'_{VGA} + 1) > 2(G'_{VGA} - 2)\omega_{in}/\omega_{LPF}. \tag{10}$$

The feedback pole (ω_{LPF}) should be at a lower frequency than the input pole ($\omega_{in} = 1/R_b C_e$). Hence, if $\omega_{in} >> \omega_{LPF}$, G'_{VGA} should be smaller than 2 for stable operation.

The output noise spectra of capacitive electrodes are known to be dominated mostly by input current noise [3]. It can be modeled by adding a noise current source (i_n) to the input node, and hence the transfer function V_o/i_n is the parallel of C_e, R_{in} and C_{in}. The variable i_n is a combination of current noise from the bias resistances and from the buffer's input. In capacitive electrodes, $C_{in} << C_e$ to avoid voltage division of V_{bio}, thus C_{in} is negligible. Hence, the noise transfer function is $R_{in}||1/sC_e$, which can be obtained by dividing (9) by $1/sC_e$ and is shown below.

$$\frac{V_o}{i_n} = \frac{\frac{s + (G'_{VGA} + 1)\omega_{LPF}}{C_e}}{\left\{s^2 + s\left[\frac{2 - G'_{VGA}}{C_e R_b} + (G'_{VGA} + 1)\omega_{lpf}\right] + \frac{(G'_{VGA} + 2)\omega_{LPF}}{C_e R_b}\right\}} \tag{11}$$

For very-low frequencies, (11) tends to $(G'_{VGA}+1)R_b/(G'_{VGA}+2)$, thus smaller the R_b is, smaller the low-frequency noise contribution. For high frequencies, the noise transfer function tends to $1/sC_e$, thus larger electrode capacitance leads to smaller noise. The transition between these two states shows a second-order low-pass behavior, and it depends on the values of G'_{VGA}, ω_{LPF}, and C_eR_b.

C. Board-Level Design

In addition to the CMOS circuit, we also propose a board-level design for the conductance neutralization. The proposed analog front-end of Fig. 5 (called here ConN) comprises a buffer, guarding circuit to bootstrap the PCB's parasitic impedances, capacitance neutralization to attenuate the input capacitance, series capacitance to reduce the effect of changes in C_e, and conductance neutralization. To control the amount of positive feedback in the neutralization circuits, R_1 and R_3 are potentiometers. Because a low-resistance path to ground is necessary for the DC bias current of U1, a high-pass filter formed by C_1 and R_5 was added (equivalent functionality to the feedback filter of Fig. 4c). In this manner, the input resistance is only boosted for frequencies higher than $1/(2\pi R_5C_1)$. An improved diode-based bootstrapped bias circuit replaces the bias resistor (R_b) and provides quick discharging in the occurrence of large MAs.

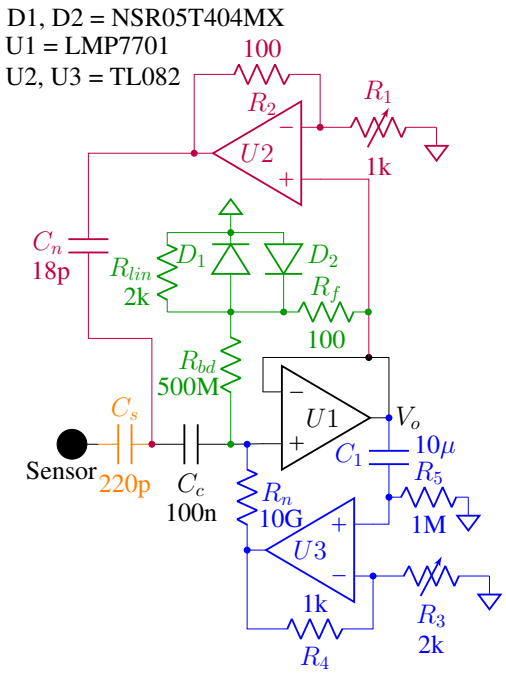


Fig. 5: Proposed AFE (ConN). It comprises the base circuit (black), capacitance neutralization (purple), conductance neutralization (blue), series capacitor C_s (orange), and a biasing circuit with diodes "D" (green)

The use of a bias resistor R_b is a simple technique to provide the necessary bias current to the op-amp's input. However, ultra-high resistors are inaccurate and require careful layout and mechanical assembly to avoid parallel leakage through the PCB's solder mask and any dust that can accumulate. To overcome these issues, bootstrapped bias circuits have been widely used [10], [12], [20]–[22], while the most recent developments use only resistors and varistors [23]. Here we introduce two modifications to this circuit as demonstrated in Fig. 5. First, the varistors are replaced by Schottky diodes. Then a resistor is placed in parallel with these antiparallel diodes. The equivalent input resistance is given by (12), where R_d is the parallel combination of the resistance of D_1 (R_{D1}), D_2 (R_{D2}) and R_{lin}.

$$R_{in,D} = \frac{R_dR_{bd}}{R_f} + R_d + R_{bd} \tag{12}$$

R_{bd} is the largest resistance, $R_{lin} > R_f$, and the on-resistance of the diodes ($R_{D1,2,on}$) is smaller than R_f. In normal operation, without voltage artifacts, the diodes are in an "off" state and present a very high resistance. Thus $R_d \approx R_{lin}$ and $R_{in,D}$ is R_{bd} boosted by a factor of R_{lin}/R_f. In the presence of a large voltage artifact, the diodes are "on" and R_d becomes $R_{D1,on}$ or $R_{D2,on}$, which are very small. Then, $R_{in,D}$ is approximately R_{bd}, providing a low-resistance path for discharging the input node.

The operating dynamics of the circuit used here are the same as the original one in [23]. However, the Schottky diodes present smaller forward voltage than varistors, meaning that they clip for lower artifacts. Moreover, if R_{lin} is not included, $R_{in,D}$ in normal operation is proportional to $R_{D1,2,off}$. These resistances change with small voltage artifacts, varying $R_{in,D}$. Hence, to force a constant $R_{in,D}$ when the diodes are "off", R_{lin} was included.

Note that both conductance neutralization and bootstrapped bias can boost the input resistance in discrete and integrated designs. However, the bootstrapped bias circuit cannot compensate for the discrete op-amps input resistance or gate leakage in integrated circuits.

Here we consider that C_e and V_{bio} are comprised within the "sensor" in Fig. 5 and that $C_{in} << C_e$ due to the capacitance neutralization. Then, conductance neutralization gain from V_o to the output of U3 is (13). Replacing this expression of G in (4) yields the transfer function for the complete circuit (14).

$$G = \left(1+\frac{R_4}{R_3}\right)\frac{s}{s+\dfrac{1}{C_1R_5}} \tag{13}$$

$$\frac{V_o}{V_{bio}} = \frac{s(s+\dfrac{1}{C_1R_5})}{s^2 + s\dfrac{C_eR_b+(1-R_4/R_3)C_1R_5}{C_eR_bC_1R_5} + \dfrac{2}{C_eR_bC_1R_5}} \tag{14}$$

From (14) it is observed that there are two zeros and two poles likewise (9). One zero is located at the origin while the other is defined by the high-pass R_5C_1 filter within the conductance neutralization circuit. On the other hand, the poles rely on C_eR_b, C_1R_5 and R_4/R_3; thus the poles are harder to predict as C_e is uncontrollable.

To comply with ambulatory ECG's bandwidth, f_c=0.5 Hz. For a range of C_e between 1 nF and 1 pF, the input resistance should range between 320 MΩ and 320 GΩ. Allowing up to

10% decrease in the midband gain due to voltage division between C_e and C_{in}, leads to the requirement of C_{in}<0.11 pF. This range of C_{in} is easily achievable with capacitance neutralization. The overall capacitance is the series combination of C_s and C_e, and hence C_s limits the maximum value. This aids in reducing the low cut-off frequency variations with changes in C_e. If C_{in} is neutralized, C_s does not affect the midband gain, however, it increases the noise level as shown in (11).

In practice, we implemented many variations of the discrete-level proposed circuit, and the one shown in Fig. 5 was the preferred one. Removing $D1$ and $D2$ allows increasing the input resistance even further, though the discharge time of MAs becomes too long without the clipping mechanism. Removing C_1 and R_5 eliminates the low-frequency peaks, however, it introduces DC a voltage to the output, which affects the diode's working range. Another alternative is to lower the resistance of R_n to the same value as R_{bd}, facilitating component selection and reducing monetary cost. In that case, a simple adjustment of the VGA's gain leads to similar values of low cut-off frequency, however, the noise becomes larger. The chosen topology is supplied with $\pm 5\,\mathrm{V}$ to allow a larger output swing compared to the $2.5\,\mathrm{V}$ single-supply alternative circuit.

III. Results and Discussion

A. CMOS Post-Layout Simulations

To explore the gate leakage compensation, the low-voltage MOSFETs of the TSMC 65nm technology were chosen because they have gate leakage models. Thicker oxide devices are available in this technology and would provide better input resistance and noise levels, however, the gate leakage is not modeled. The circuit was simulated in Cadence Virtuoso with Spectre. These post-layout simulations comprised C+CC extracted models. A parametric simulation on I_{ctrl} (see Fig. 4a), swept the current from $1\,\mu\mathrm{A}$ to $10\,\mu\mathrm{A}$. AC frequency response, noise, and transient simulations were the analyses performed, and the results are shown in Fig. 6.

Fig. 6a displays the G_{VGA} variation as a function of the control current (I_{ctrl}). The gain was obtained by measuring the ratio of $V_{o,vga+}$ and V_o in an AC sweep. The range of gains desired is achieved for I_{ctrl} of $2\,\mu\mathrm{A}$ and $6\,\mu\mathrm{A}$, where G_{VGA} is 0.97 V/V and 2.04 V/V respectively. The VGA's gain increases due to the rise in $gm_{d3,4}$ ($\approx \sqrt{2I_{ctrl}\mu_p C_{ox} W/L}$), while the VGA's load impedance is kept fairly constant by the common-mode feedback loop.

The input impedance was analyzed with the ratio between the voltage and the current flowing into the circuit's input. Fig. 6b shows the input impedance in the pass-band. When G_{VGA} is 1.6 V/V, 1.9 V/V and 2 V/V the input impedance is respectively $27\,\mathrm{M\Omega}$, $83\,\mathrm{M\Omega}$ and $260\,\mathrm{M\Omega}$. The peak value of Z_{in} is $3\,\mathrm{G\Omega}$ for a gain of 2.04 V/V. Knowing that Z_{in} is in the pass-band, one can fit the data from Fig. 6b in (5). Thus, $R_b/2$ is estimated to be approximately $11.4\,\mathrm{M\Omega}$.

The slope of the curve in Fig. 6b provides the sensitivity of Z_{in} to changes in G_{VGA}. Note that to achieve impedance boosting over 100 times, G_{VGA} must be extremely accurate. Moreover, it cannot be vulnerable to noise or unwanted variations. However, for small impedance boosts, such as 10, the sensitivity of Z_{in} with G_{VGA} is much smaller and easier to achieve in practice.

The value of the capacitance between the body and the electrode (C_e) has been reported between $1\,\mathrm{pF}$ and $1\,\mathrm{nF}$. To simulate the capacitive electrode's frequency response, V_o was assessed for a unitary input V_{bio} and a C_e of $1\,\mathrm{nF}$. The control current I_{ctrl} was swept as reported before, but only 5 curves are presented in Fig. 6c.

As expected from (9), the output demonstrates a high-pass filter behavior. The increase in I_{ctrl} (and G_{VGA}) decreases the cut-off frequency. Only the maximum simulated G_{VGA} led to a low-frequency peak (2.3 V/V). The cut-off frequencies for the displayed gains were $14.7\,\mathrm{Hz}$, $3.5\,\mathrm{Hz}$, $1.6\,\mathrm{Hz}$, $0.25\,\mathrm{Hz}$ and $0.085\,\mathrm{Hz}$. Taking as an example an electrocardiography, where the low cut-off frequency is $0.5\,\mathrm{Hz}$, the proposed circuit is necessary to achieve the desired low cut-off frequency.

From the 40 steps in the parametric simulation, I_{ctrl} equal to $5.23\,\mu\mathrm{A}$ is the one that leads to the largest bandwidth without peaking. As the current in the VGA increases beyond this I_{ctrl}, the transfer function behavior becomes underdamped. For $5.59\,\mu\mathrm{A}$ the cut-off was $75\,\mathrm{mHz}$ with a peak of $1.5\,\mathrm{V/V}$ at $0.33\,\mathrm{Hz}$. For the case with the highest I_{ctrl}, a peak of $2.5\,\mathrm{V/V}$ occurred.

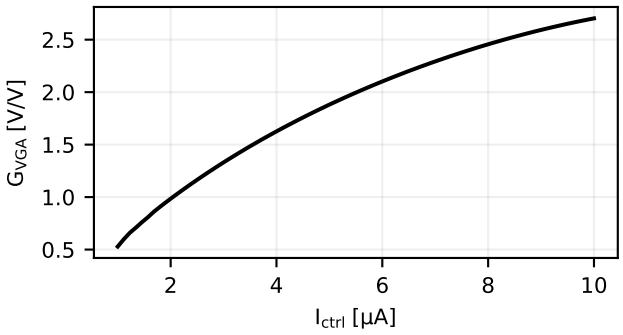
The relative noise, displayed in Fig. 6d as a function of G_{VGA}, is the proposed circuit's integrated input referred noise divided by the integrated input referred noise of the circuit without the input resistance boosting circuit. The integration limits are $0.5\,\mathrm{Hz}$ and $100\,\mathrm{Hz}$. For small G_{VGA}, the proposed circuit's R_{in} is smaller than R_b, tending to $R_b/2$ when G_{VGA} is zero. Thus the relative noise is smaller than 1. As G_{VGA} increases, the proposed circuit's input-referred noise rises and so does the relative noise. At the maximum R_{in} boosting, the noise is 7.5% higher compared to the circuit without boosting.

B. Board-Level Simulations and Measurements

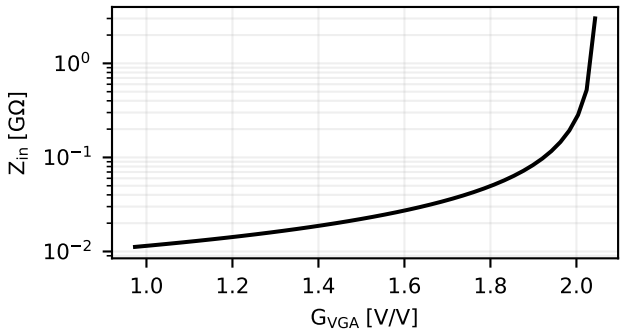
The proposed AFE's transfer function (14) was numerically simulated to evaluate the frequency response and the results are depicted in Fig. 7. One of the zeros relies on C_1R_5 while the poles depend on both C_1R_5 and R_bC_e. Hence, variations in C_e change the damping factor ζ of the second order denominator, so C_1R_5 has to be designed to provide an acceptable output for a range of C_e values.

For this analysis, C_e was assumed to be $1\,\mathrm{nF}$ and $1\,\mathrm{pF}$, R_b is $10\,\mathrm{G\Omega}$ and $R4/R3$ is 0.969 to set the equivalent input resistance to $320\,\mathrm{G\Omega}$ according to (5). C_1 was fixed at $10\,\mu\mathrm{F}$ while R_5 was $1\,\mathrm{M\Omega}$ or $10\,\mathrm{M\Omega}$ or $100\,\mathrm{M\Omega}$. Hence, the zero's frequency was $15.9\,\mathrm{mHz}$, $1.59\,\mathrm{mHz}$ and $0.159\,\mathrm{mHz}$ respectively. C_s was not included in this simulation to allow an understanding of the frequency behavior with conductance neutralization for different electrode capacitances.

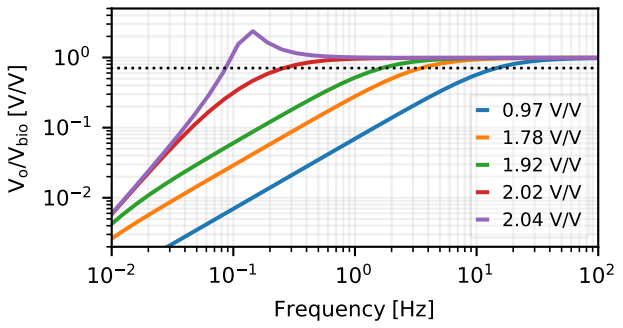
The results in Fig. 7a shows that for C_e=1 nF, all curves have similar under damped behavior with peaks of $10.8\,\mathrm{dB}$ at $2.3\,\mathrm{mHz}$, $10.9\,\mathrm{dB}$ at $7.2\,\mathrm{mHz}$ and $4.8\,\mathrm{dB}$ at $24.8\,\mathrm{mHz}$. On the other hand, when C_e=1 pF, the gain presents distinct behavior for each value of R_5. For $1\,\mathrm{M\Omega}$ the curve displays lower damping, with the zero's effect being visible at $15.9\,\mathrm{mHz}$



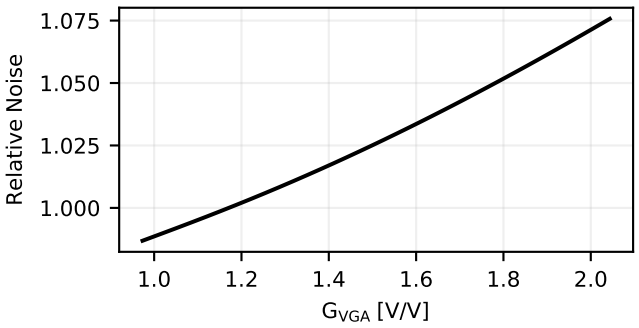
(a) G_{VGA} at 1 mHz as a function of I_{ctrl}



(b) Magnitude of Z_{in} as a function of G_{VGA} at 1 mHz



(c) Frequency response of V_o for different G_{VGA}, shown in the legend in V/V



(d) Relative integrated noise as a function of G_{VGA}

Fig. 6: Integrated CMOS design post-layout simulations

and the complex-conjugate poles cause a peak of 3.5 dB at 0.82 Hz. Setting R_5 to 10 MΩ moves the zero to 1.59 mHz while distancing the poles, which leads to a response closer to maximally flat. Last, R_5=100 MΩ reduces the zero's frequency to 0.159 mHz and separates the two poles, with their effects being visible around 10 mHz and 500 mHz. A root locus plot, not provided here, confirmed that when C_e is 1 pF and R_5 is either 10 MΩ or 100 MΩ, the poles were real. In all other simulated cases, they were complex-conjugate pairs.

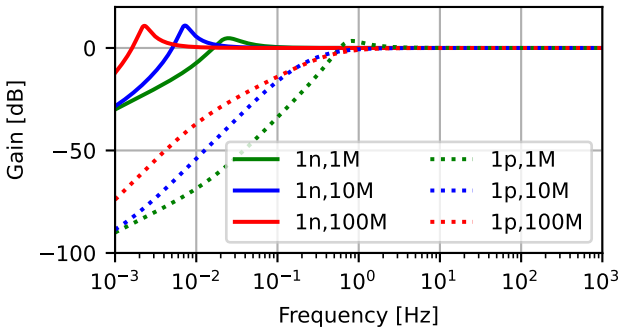
The effects described in the magnitude analysis are observed similarly in the phase delay analysis by inspection of Fig. 7b. Because of the zero at the origin in (14), the phase delay starts at 90°. By comparing the curves with the same color one can observe the effect of the other zero in the phase, which does not depend on C_e according to (14). Yet, the smaller damping factor of the complex poles when C_e is 1 nF compared to 1 pF is observed as a steep drop in phase. The aforementioned separation of poles is also present in the phase plot. For example, the blue curve peak is much wider when C_e is 1 pF.

The high-pass filter (C_1 and R_5) was added to the conductance neutralization loop, so the overall input resistance is not boosted in very low frequencies and a path for the flow of the input bias current is provided. Hence, it creates an impedance that increases with frequency, behaving as an inductor. This apparent inductance interacts with C_e and may cause peaks in the frequency response and also oscillation. On the other hand, if well-designed, the filter increases the order of the electrode's high-pass characteristic. The chosen value of R_5 was 1 MΩ to provide similar peaking for low and high C_e with a steeper slope to enhance attenuation of lower frequencies and discharge faster.

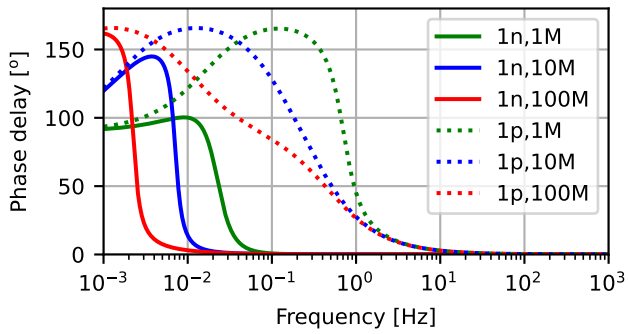
Fig. 8 shows the frequency response of the proposed AFE for different coupling capacitances over a copper board. By replacing C_s with a 0 Ω resistor, the condition with maximum coupling was assessed (C_e ≈1 nF). Then, a 1 pF capacitor was inserted into the place of C_s, simulating the worst-case scenario. The results shown in Fig. 8 are for a maximally boosted input resistance. That is, the calibration took place with a C_s of 1 pF, and the potentiometer was adjusted until the edge of oscillation.

The first thing we can observe in Fig. 8a is that the reference AFE displayed an f_c value of 71 mHz for full capacitance (Ref), while when C_s was 1 pF, f_c was 72 Hz (Ref 1p). For full C_e, the proposed AFE showed approximately 8 dB (ConN) of peaking, and its f_c was 33 mHz (ConN). When C_s was 1 pF, the peak was negligible and the cut-off frequency was 1.5 Hz (ConN 1p).

The measured phase delays in Fig. 8b are in agreement with the numerical simulations shown in Fig. 7b. The phase for the reference AFE starts at 90°, falling to 45° at the cut-off frequency and then reaching zero. The ConN peaks were of 130° at 30 mHz and of 141° at 0.66 Hz. Some traces in Fig. 8b are not plotted in the whole frequency range

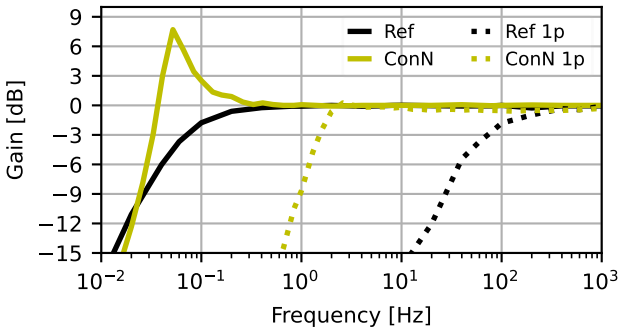


(a) Magnitude

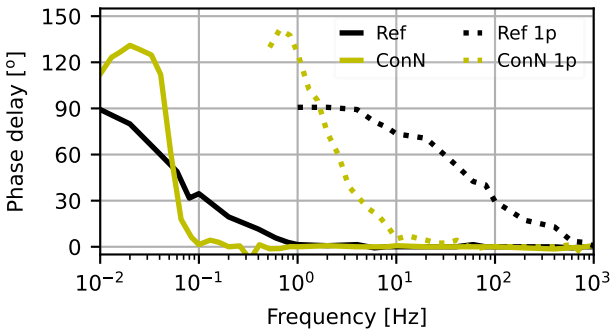


(b) Phase delay

Fig. 7: Numerical simulation of (14), where C_e and R_5 are varied. Legend is in the format "C_e [F], R_5 [Ω]". a) Magnitude of (14); b) Phase delay of (14)



(a) Magnitude



(b) Phase delay

Fig. 8: Measured bode plot comparing the proposed AFE with the reference AFE. Labels with "1p" stand for circuits where the coupling capacitance was limited by using C_s of 1 pF, while the absence of 1p means that the electrode had maximum electrode capacitance (≈1 nF)

because of the minimum scale of the measuring device. The injected signal's peak-to-peak amplitude was 40 mV, while the minimum resolution of the oscilloscope is 1 mV per division. Hence the output of the reference AFE for C_e equal to 1 pF was too small for frequencies below 1 Hz. Furthermore, the oscilloscope's noise floor was also in the amplitude of the minimum resolution, making measurements in this range of voltages impossible.

For the full C_e, the peak in the gain magnitude was high, and the increase in bandwidth compared to the reference AFE is small. This happens because the R_5C_1 limits the range of frequency where the input resistance is boosted. However, in this measurement, the conductance neutralization gain was maximized to lead to the lowest f_c when C_s =1 pF and was not optimized for high C_e operation. Hence, when C_s is forced to be 1 pF, one can clearly see the input resistance boost at work. Even though the ConND had an f_c 3 times larger than 0.5 Hz for the minimum capacitance, it performed much better than the reference AFE, which had f_c 144 times greater than the desired. This scaling in cut-off frequency is proportional to the increase of R_{in}.

With the measured low cut-off frequency and the electrode capacitance value, one can estimate the input resistance ($f_c = 1/2\pi R_{in}C_e$). By inspecting the curve from the reference AFE (Ref 1p) in Fig. 8 and knowing that C_e was 1 pF, the overall R_{in} is estimated to be 2.2 GΩ. The value of R_b is set to 10 GΩ, and the datasheet of LMP7701 does not provide a value for $R_{in,op}$. Thus we can calculate the value of $(R_{leak}||R_{in,op})$ as 2.82 GΩ. The proposed circuit with 1 pF capacitance had a cut-off frequency of 1.5 Hz, thus the apparent input resistance is 106 GΩ. This represents a boost of 48 times compared to the reference circuit's input resistance.

To display the clipping mechanism of the bootstrapped circuit with diodes, a triangular waveform was injected into the copper board where ConN and Ref electrodes were lying over. This input signal had a peak-to-peak amplitude of 1 V at a frequency of 0.5 Hz.

The data from Fig. 9 shows that the clipping region was as expected, and signal amplitudes above the Schottky diode forward voltage are blocked. The clipping values were −0.28 V and 0.3 V. During the discharge period (one of the diodes conducting), the resistance seen from the input node is 500 MΩ. The proposed circuit presented a slight phase shift compared to the input and the reference circuit. One can also see distortion on the reference circuit curve, which is caused by the high-pass characteristic.

To demonstrate the performance of the proposed electrodes under different coupling conditions, the common-mode rejection ratio (CMRR) of an unbalanced pair of electrodes was measured. That is, one of the electrodes had direct contact

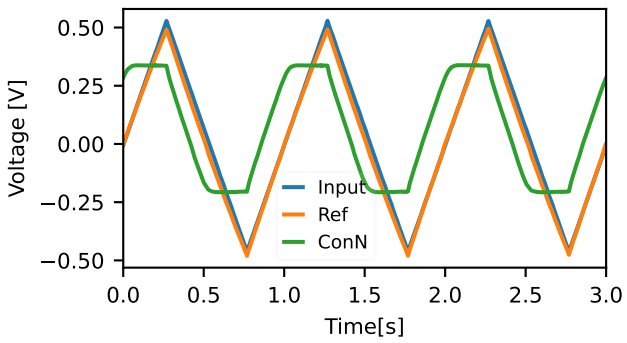


Fig. 9: Proposed AFE' response to a triangular input

with the skin and the other was connected through a cotton T-shirt. A reference signal from the signal generator was injected into the human body through a wet Ag/AgCl electrode connected to the right ankle, enabling the frequency response in realistic conditions to be obtained. A pair of identical capacitive electrodes were attached to the subject's lower back. An elastic band around the subject's waist held the electrodes in place. The tested topologies were the reference circuit and the proposed circuit with C_s (220 pF) and without it (shorting C_s). The bode plot is displayed in Fig. 10. The objective is to assess the improvement in the CMRR provided by C_s, which happens mainly around the low cut-off frequency. Thus, only the lower frequencies are displayed.

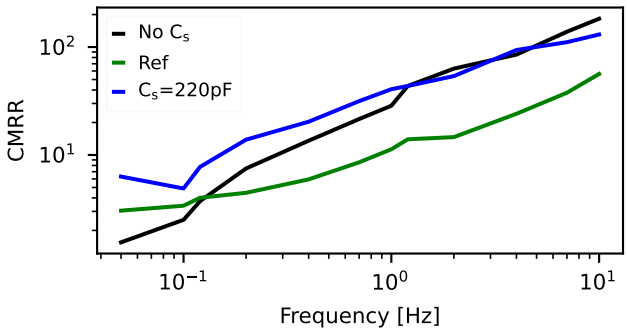


Fig. 10: CMRR of unbalanced electrodes. The reference circuit and proposed circuit with and without C_s are evaluated

Fig. 10 shows that for frequencies higher than the ambulatory ECG's low cut-off frequency (0.5 Hz), the proposed circuit presented higher CMRR than the reference electrode. In very low frequencies, the proposed circuit with C_s had the highest CMRR, while the proposed circuit without C_s had the worst CMRR. The explanation is the low-frequency peak created by the conductance neutralization when C_e is high. Because in this test one electrode has direct contact with the skin (high C_e) and the other has a smaller C_e, the peaks' amplitudes differ and create a CMRR issue. The proposed circuit with C_s has a smaller low-frequency peak, and the cut-off becomes less dependent on C_e. The reference circuit does not present low-frequency peaks but the cut-off frequency is inversely proportional to C_e. Thus, the added layer of clothing directly modifies the low-frequency response creating a mismatch and reducing the CMRR.

An ECG acquisition is demonstrated in Fig. 11. The waveforms displayed were obtained by using a pair of balanced similar electrodes. The reference circuit and the proposed circuit with and without a C_s of 220 pF were tested. The left column of Fig. 11 shows the ECG measured in direct contact with the skin and the right column shows the acquired signals measured through a T-shirt. The acquisition board possessed a band-pass filter with bandwidth between 50 mHz and 300 Hz, then a 2^{nd}-order digital band-pass with cut-off frequencies between 0.5 Hz and 100 Hz was applied in addition to a digital 4^{th}-order notch filter at 60 Hz. The subject was grounded with a wet Ag/AgCl electrode and the driven right leg circuit was not used.

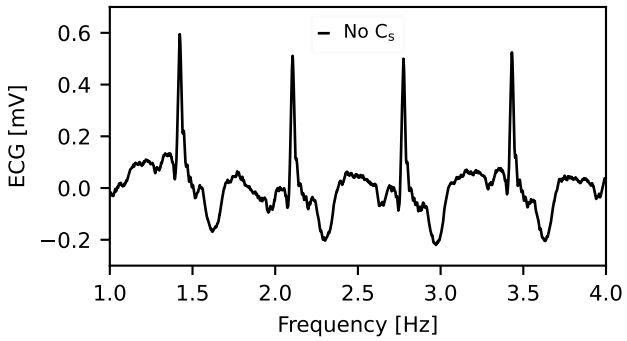
The measurements of ECG in direct contact with the skin (left column of Fig. 11) led to clean ECG waveforms for all three electrode topologies. The proposed circuit without C_s was the one with less 60 Hz interference, followed by the one with C_s. This was expected from Fig. 10 even though the CMRR at 60 Hz was not measured due to the mixing of noise and reference signal. Most of the breathing/motion artifact was removed by the digital band-pass filter in all cases. In the through-clothing acquisition, in both proposed circuits the QRS wave is still identifiable. However, the breathing artifact is significant, especially in the case without C_s where low-frequency CMRR is worse. Due to the smaller capacitance generated by C_s, noise is also visible in Fig. 11d. The reference circuit was not capable of proving a readable ECG through clothing. The proposed circuit's simulated RMS output noise, considering an electrode capacitance of 220 pF and integration limits of 0.5 Hz and 100 Hz, is 6.12 µV.

IV. Conclusions

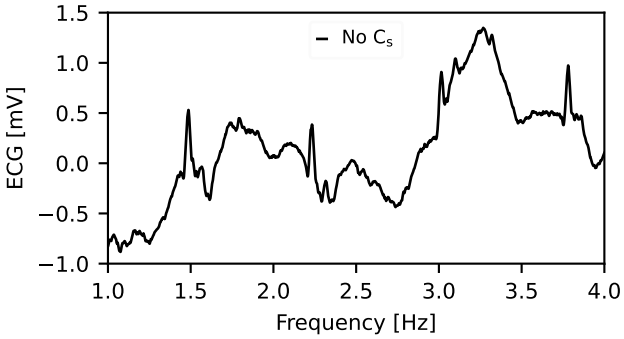
In this paper, we proposed a capacitive electrode topology based on a NIC circuit that boosts the input resistance and is not sensitive to gate leakage and the op-amp's input resistance. An integrated CMOS design was developed and simulated (post-layout). The results showed that with 40 steps of I_{ctrl}, the input resistance can be boosted by a factor of 100. Besides the power and area increase, the performance cost is a 7.5% increase in noise. These results were supported by measurements on a discrete design, where the input resistance increased by 48 times.

The boosted input resistance allowed the insertion of the small C_s in series with the electrode capacitance, reducing the variations of the f_c caused by the changes in the electrode capacitance and consequently improving the CMRR. Compared to the reference electrode, the proposed circuit was able to measure an ECG in direct contact with the skin and through clothing. The addition of C_s increases the amplifier's noise, however, it reduces the breathing artifact.

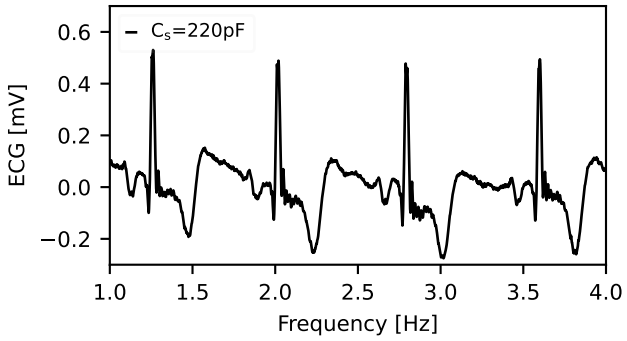
The results provided in this paper showed improvements in the overall performance of the AFE of a capacitive electrode for biomedical applications. Yet, some challenges must be addressed to achieve large-scale production. Here, both neutralization loops were tuned with a potentiometer, which



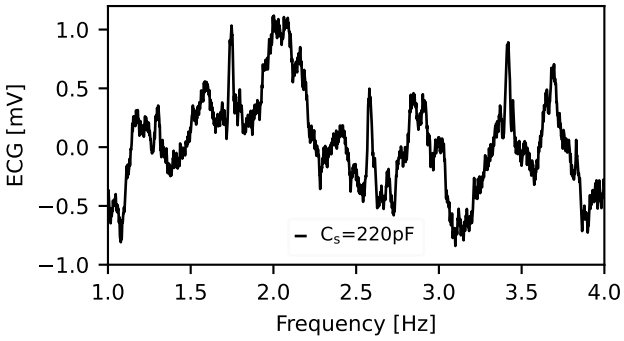
(a) ECG from proposed electrode without C_s in direct contact with the skin



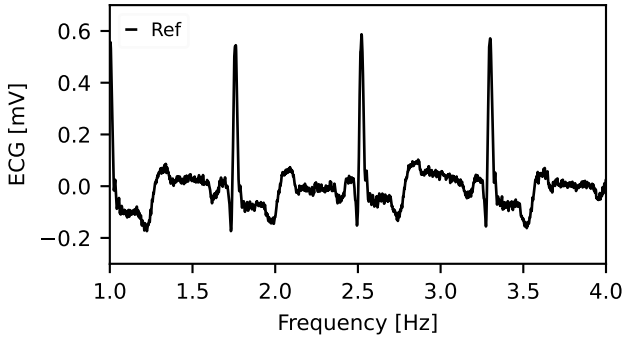
(b) ECG from proposed electrode without C_s through T-shirt



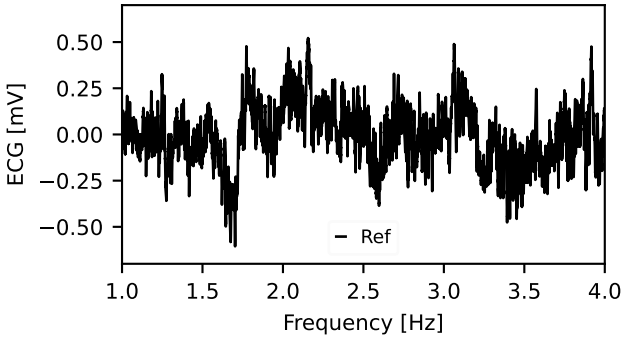
(c) ECG from proposed electrode with C_s=220 pF in direct contact with the skin



(d) ECG from proposed electrode with C_s=220 pF through T-shirt



(e) ECG from reference circuit in direct contact with the skin



(f) ECG from reference electrode through T-shirt

Fig. 11: Measured ECG with proposed and reference circuits in direct contact with the skin and through clothing. The proposed circuit was tested with and without C_s

requires manual trimming and are expensive. Fixed value resistors present inaccuracy that could lead to mismatched electrodes, and in the worst-case scenario, oscillation of the positive feedback.

The capacitance neutralization usually does not require very fine tuning as commercial op-amp's are already in the range of a few pF. Moreover, alternatives to the capacitance neutralization exist [12], [24] and it can also be automatically tuned [25]. Large input capacitances lead to voltage division and subsequent degradation of the midband CMRR.

The inaccuracy in the conductance neutralization loops affects R_{in}, and hence creates mismatches in the low cut-off frequencies. This is a critical issue if large input resistance boosting is targeted because accurate positive feedback gain is necessary. However, one should mind that even if C_s is used, significant mismatch in the low cut-off frequency is expected due to mismatched C_e.

Therefore, future works shall not only aim at boosting R_{in} but also controlling it for different values of C_e in each electrode, thus stabilizing the low cut-off frequencies. Moreover, the electrode's gain could be set by an automatic gain control. This should maximize the CMRR by compensating for mismatches created by different clothing, MA, PVT variation and drift of components.

ACKNOWLEDGMENT

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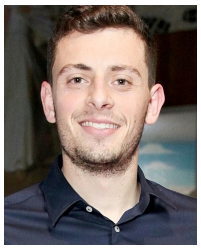

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