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Single-DC-Source Three-Phase Modified Packed U-Cell Inverter With Reduced Components and Active Capacitor Voltage Balancing

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ABSTRACT This article introduces a modified Packed U-Cell (PUC) inverter to establish a three-phase configuration using a single dc source to overcome the drawbacks of the multi-individual dc sources in the conventional three-phase PUC topology. The three-phase modified PUC is designed by the cascading connection of a flying capacitor and Hybrid Packed U-Cell (HPUC) in each phase, where the whole circuit design is fed by a single-dc-source voltage. The single-dc-source three-phase modified PUC inverter is also expandable by expanding the HPUC structure. The floating capacitors are actively balanced by integrating the abundant redundant switching states into the designed pulsewidth modulation technique through a voltage balancing algorithm. The performance of the three-phase nine-level modified PUC inverter and its floating capacitor voltage balancing is evaluated through theoretical and experimental analyses under all stand-alone and grid-connected operation conditions. The comparative study demonstrates that the three-phase modified PUC has fewer active and passive devices compared to other counterpart three-phase multilevel topologies.

INDEX TERMS Floating capacitor voltage balancing, hybrid packed U-cell (HPUC), reduced components counts, single-dc-source three-phase nine-level inverter, three-phase modified packed U-cell (PUC).

I. INTRODUCTION

Due to the voltage and current limitations of the semiconductor devices, the conventional single-phase H-Bridge is not suitable for high-power applications [1]. Therefore, the cascaded configuration of the H-Bridge configuration emerged as the solution to overcome this challenge, utilizing several dc sources to form a multilevel converter [2]. However, the cascaded H-Bridge and other multi-dc-source topologies are considered as the nonoptimized structure restricted to photovoltaic applications [3], [4], [5]. Subsequently, single-dc-source structures emerged as an optimized inverter topology [6]. To this end, the first generation of the multilevel inverter, including diode clamped, and the flying capacitor (FC) has even been adapted into single-dc-source configurations, as they continue to inspire new multilevel converter designs [7], [8].

In case of a single-dc-source structure, H-Bridge, Packed U-Cell (PUC), and Packed E-Cell (PEC) have emerged as successful single-phase compact multilevel inverters [9]. The PUC topology was introduced in [10] to reduce circuit devices and to multiply voltage levels. Due to the capacitor balancing problem in the extended PUC, the PEC was proposed as an optimal circuit, where component count is further reduced, and active capacitor balancing is achieved [11]. In [12], a compact switched-capacitor single-phase inverter was designed using a T-type cell. Nevertheless, it has extra devices and capacitor balancing issue for a full modulation index (MI) range. A single-phase single-dc-source

compact inverter was developed in [13] and [14] utilizing several bidirectional switches and capacitors to reach multilevel operation. However, it has the same defects of [12]. In [15] and [16], a single-phase single-dc-source step-up switched-capacitor multilevel inverter was introduced for boosting output voltage. However, it has drawbacks of notable active and passive component counts and capacitor balancing for a full MI range. Various innovative single-phase single-dc-source inverters were developed using H-bridge configurations; yet, they are not competitive with other topologies in terms of the number of devices [17], [18]. The main demerit of the aforementioned topologies is the necessity of three separated dc sources for a three-phase configuration, where the importance of single-dc-source topologies is greatly intensified.

The first generation of the single-dc-source three-phase inverter was the six-switch two-level topology [19]. In spite of simplicity, it requires a huge dc-link capacitor, while output voltage and current qualities are low. The three-phase two-level inverter is suitable for low-power applications as the voltage and current of switches are limited [20]. Despite this, it is used to make the single-dc-source three-phase structure for H-Bridge, where extra dc sources are replaced by the capacitors, but it is a nonoptimized in terms of number of devices and voltage levels [21], [22], [23]. Neutral point clamed (NPC) was the first single-dc-source three-phase multilevel inverter to operate at high voltage and current rating [24]. Although NPC improves power quality and dc-link voltage utilization, it has capacitor balancing and right diode selection challenges especially for its extended topology [25], [26]. To address NPC challenges due to the clamped diode loop, the three-phase FC was introduced using a clamped capacitor loop [27]. Although the FC is free of diode selection, it uses more capacitors, and voltage balancing problems appear especially in the extended structure [8]. Active neutral point clamped (ANPC) emerged as a single-dc-source five-level topology that operates in higher power rating and quality [28]. Extended ANPC confronts the same control complexity of NPC and FC extension versions [29]. In [30], the single-dc-source three-phase five-level inverter was developed using the H-Bridge and the floating capacitor inverter. Although the three-phase inverter of [30] has single-dc-source benefit and adequate switching states for capacitor balancing, it includes notable switches and capacitors particularly for the extended topology. In [31], the step-up-based single-phase single-dc-source multilevel inverter was presented, while it is also configurable as three-phase without extra dc sources. The multilevel inverter of [31] was built by chaining new bidirectional-switch-based cells to provide varied access to capacitors for redundant charging and discharging states. However, it contains noticeable semiconductor devices, while it confronts high-voltage stress as capacitor voltages are boosting.

This article focuses on modifying the conventional multi-dc-source three-phase PUC into a single-dc-source three-phase inverter topology, while more voltage levels are obtained, circuit devices are decreased, and floating capacitor voltages are actively balanced. The proposed three-phase PUC topology is a compromised between the cascaded connection of FC and hybrid packed U-cell (HPUC), where the whole circuit design is supplied by a single-dc-source voltage. The cascaded connection occurs in two stages per phase. First, the FC cell that has four switches and one floating capacitor is connected to a single dc source. Second, the HPUC has six switches and two capacitors to provide ac terminal. The proposed single-dc-source three-phase modified PUC inverter can also be expanded by expanding the HPUC stage, enabling higher voltage levels while maintaining an optimized component count. The floating capacitor voltages are actively regulated due to the effective and adequate redundant states, which are integrated into the designed pulsewidth modulation (PWM) technique through a voltage balancing algorithm without external and complicated voltage regulator controller, phase current direction, or/and operational condition. As a result of the active balancing for the floating capacitor voltages and single-dc-source structure, the three-phase modified PUC inverter is suitable for grid-connected operations as well as stand-alone ones. Accordingly, a current-based control framework is designed for the grid-connected operation of the three-phase modified PUC to synchronize the grid phase voltages and the inverter's output currents as to control the injected active and reactive power to the grid side. Therefore, the main contributions of this article are as follows.

1) This article develops the multi-dc-source three-phase PUC to create a single-dc-source three-phase modified PUC with reduced device counts.
2) It presents theoretical and mathematical analyses and discussion of the floating capacitor voltages behavior.
3) It designs the PWM algorithm for the floating capacitor voltage regulation using the integrated voltage balancing blockchain.
4) It designs a current-based controller for the grid-connected operation of the three-phase modified PUC inverter
5) It provides experimental validation of the three-phase modified PUC inverter under different stand-alone and grid-connected operations.

The rest of this article is organized as follows. Section II describes the circuit configuration and switching state possibilities of the nine-level operation of the three-phase modified PUC inverter. The mathematical and theoretical study is performed in Section III to analyze the behavior of the floating capacitor voltages to design a PWM method with the voltage balancing algorithm for active capacitor voltage regulation. Section III also includes the designed-current-based control framework for three-phase grid-connected operation. Section IV discusses the component count comparison analysis. The experimental results that are attained for different stand-alone and grid-connected operation conditions, including load and frequency changes, MI variations, start-up operation, and constant and dynamic grid current condition, are discussed in Section V. Finally, Section VI concludes this article.

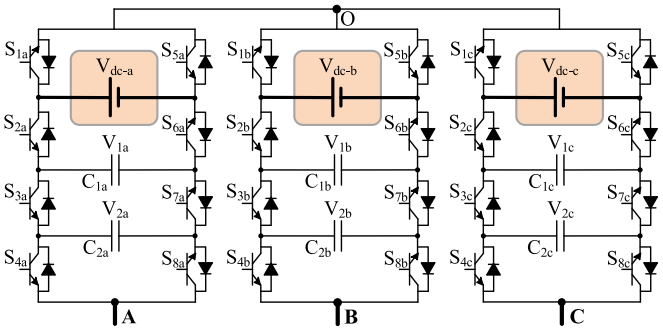

FIGURE 1. Conventional three-phase nine-level PUC with three isolated dc sources.

II. SINGLE-DC-SOURCE THREE-PHASE MODIFIED PUC INVERTER

A. CIRCUIT TOPOLOGY AND CONFIGURATION FOR NINE-LEVEL OPERATION

Although the PUC is a promising single-phase inverter, it needs three isolated dc sources for the three-phase configuration. Fig. 1 shows the three-phase nine-level PUC inverter using three dc sources. Indeed, this is the main drawback of the conventional packed inverters, as not only extra dc sources, voltage, and current sensors are required, but also a more complicated controller is needed.

Moreover, there will be circulating current among three phases, which makes an unbalanced power problem that directly affects capacitor voltage regulation ability. As a result, the switching and control techniques would be further complicated. To overcome this challenge, the packed multilevel inverters need to be developed to a single dc source for a three-phase configuration. Taking the benefit of the FC cell and reconfiguring the PUC with two capacitors as an HPUC, a single-dc-source three-phase packed inverter is created. Fig. 2 illustrates the single-dc-source three-phase nine-level inverter cascading the FC cell and the HPUC. According to the circuit, each phase contains a single FC cell as the first stage connected to a single dc source and an HPUC as the second stage that makes ac output. The FC cell includes four switches and one capacitor, and the HPUC contains six switches and two capacitors. Therefore, ten switches and three capacitors are needed for nine-level generation. FC cell capacitor voltage is adjusted to half of dc input voltage ($V_{dc}/2$). The second and third capacitors placed in the HPUC are regulated to quarter and one-eighth of dc input voltage ($V_{dc}/4$ and $V_{dc}/8$), respectively. Accordingly, the voltage stress across switches is distributed based on their location in the proposed modified PUC inverter. S_1, S_2, S_6, and S_7 in the FC cell experience up to $V_{dc}/2$, S_3, and S_8 handle $V_{dc}/4$, and S_4, S_5, S_9, and S_{10} are limited to $V_{dc}/8$. This means that no switch is exposed to V_{dc}, which simplifies device selection, improves reliability, and supports scalable design with manageable voltage stress across all components. The nine-level voltage appears between output terminal of each phase (A, B, and C) and inverter neutral point (O): V_{AO}, V_{BO}, and V_{CO}, employing the positive voltage levels as 0, $V_{dc}/8$, $2V_{dc}/8$, $3V_{dc}/8$, $4V_{dc}/8$, $5V_{dc}/8$, $6V_{dc}/8$, $7V_{dc}/8$, and $8V_{dc}/8$. Phase voltages V_{An}, V_{Bn}, and V_{Cn} (n is the neutral point of three-phase loads) and line voltages V_{AB}, V_{BC}, and V_{AC} are 17-level voltages between $+V_{dc}$ and $-V_{dc}$ with the step of $V_{dc}/8$.

TABLE 1. All Possible Switching States For Positive Voltage Levels in a Single-Phase Nine-Level Modified PUC Inverter

State	S_1	S_2	S_3	S_4	S_5	Output Voltage
1	0	0	0	0	0	$V_{out} = 0$
2	0	0	1	1	1	$V_{out} = 0$
3	0	0	0	0	1	$V_{out} = +V_{dc}/8$
4	0	0	0	1	0	$V_{out} = +V_{dc}/8$
5	0	0	0	1	1	$V_{out} = +2V_{dc}/8$
6	0	1	1	0	0	$V_{out} = +2V_{dc}/8$
7	1	0	1	0	0	$V_{out} = +2V_{dc}/8$
8	0	1	1	0	1	$V_{out} = +3V_{dc}/8$
9	0	1	1	1	0	$V_{out} = +3V_{dc}/8$
10	1	0	1	0	1	$V_{out} = +3V_{dc}/8$
11	1	0	1	1	0	$V_{out} = +3V_{dc}/8$
12	0	1	0	0	0	$V_{out} = +4V_{dc}/8$
13	0	1	1	1	1	$V_{out} = +4V_{dc}/8$
14	1	0	0	0	0	$V_{out} = +4V_{dc}/8$
15	1	0	1	1	1	$V_{out} = +4V_{dc}/8$
16	0	1	0	0	1	$V_{out} = +5V_{dc}/8$
17	0	1	0	1	0	$V_{out} = +5V_{dc}/8$
18	1	0	0	0	1	$V_{out} = +5V_{dc}/8$
19	1	0	0	1	0	$V_{out} = +5V_{dc}/8$
20	0	1	0	1	1	$V_{out} = +6V_{dc}/8$
21	1	0	0	1	1	$V_{out} = +6V_{dc}/8$
22	1	1	1	0	0	$V_{out} = +6V_{dc}/8$
23	1	1	1	0	1	$V_{out} = +7V_{dc}/8$
24	1	1	1	1	0	$V_{out} = +7V_{dc}/8$
25	1	1	0	0	0	$V_{out} = +8V_{dc}/8$
26	1	1	1	1	1	$V_{out} = +8V_{dc}/8$

B. SWITCHING STATE SEQUENCE AND OPERATION

To specify the switching sequence, it is only required to do it for a single-phase configuration, as the switching intervals of two other phases are accordingly achieved by phase shifting. Fig. 3 shows a single phase of the nine-level modified PUC inverter. Considering complementary operation for the switches: (S_1, S_6), (S_2, S_7), (S_3, S_8), (S_4, S_9), and (S_5, S_{10}), there are 32 states. Some states are also not usable as they are generating negative voltage levels. Indeed, only 26 states can be effectively utilized for nine-level voltage and six states that generate levels; $-V_{dc}/8$, $-9V_{dc}/8$, and $-10V_{dc}/8$ are not assumed. A total of 26 effective switching states with positive voltage levels (between 0 and V_{dc} with a step of $V_{dc}/8$) are listed in Table 1.

C. CHARGING AND DISCHARGING STATES OF FLOATING CAPACITORS

As shown in Table 1, there are plenty of redundant states for each level, where they can be used for capacitor voltage balancing.

Table 2 shows redundant charging and discharging states of the floating capacitors that are used to regulate their voltages to the desired dc values. The floating capacitors are involved in voltage levels $V_{dc}/8$, $2V_{dc}/8$, $3V_{dc}/8$, $4V_{dc}/8$, $5V_{dc}/8$, $6V_{dc}/8$, and $7V_{dc}/8$, while there is no effect for voltage levels 0 and $8V_{dc}/8$. Redundant states must be integrated with the

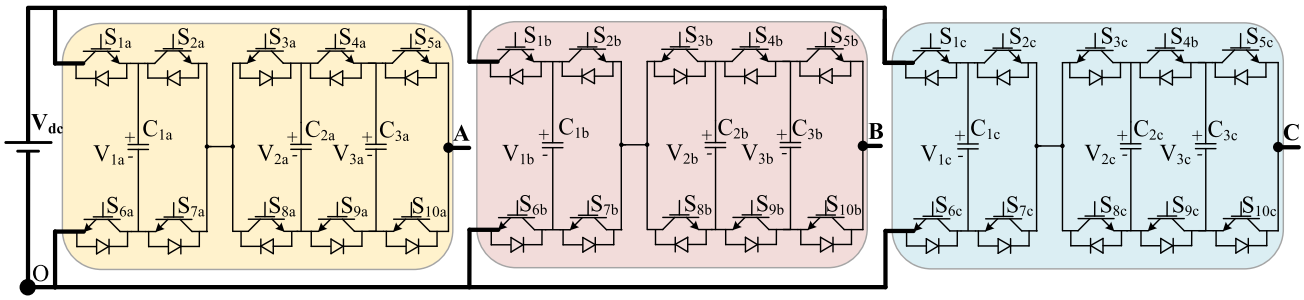

FIGURE 2. Schematic of the single-dc-source three-phase 17-level (line to line) modified PUC inverter.

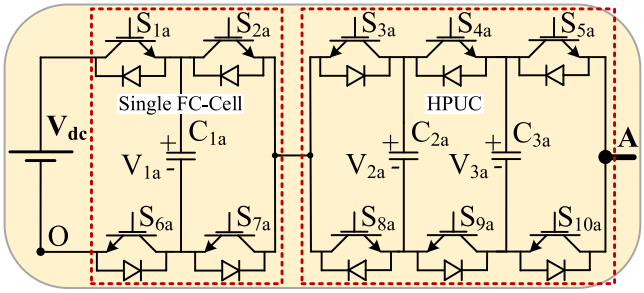

FIGURE 3. Single-phase schematic of the single-dc-source nine-level inverter.

TABLE 2. Floating Capacitor States (Nothing: –, Charging: ↑, and Discharging: ↓) of a Single-Phase Nine-Level Modified PUC Inverter Related to Table 1

State	S_1	S_2	S_3	S_4	S_5	C_1	C_2	C_3
1	*0*	*0*	*0*	*0*	*0*	-	-	-
2	*0*	*0*	*1*	*1*	*1*	-	-	-
3	*0*	*0*	*0*	*0*	*1*	-	-	↓
4	*0*	*0*	*0*	*1*	*0*	-	↓	↑
5	*0*	*0*	*0*	*1*	*1*	-	↓	-
6	*0*	*1*	*1*	*0*	*0*	↓	↑	-
7	*1*	*0*	*1*	*0*	*0*	↑	↑	-
8	*0*	*1*	*1*	*0*	*1*	↓	↑	↓
9	*0*	*1*	*1*	*1*	*0*	↓	-	↑
10	*1*	*0*	*1*	*0*	*1*	↑	↑	↓
11	*1*	*0*	*1*	*1*	*0*	↑	-	↑
12	*0*	*1*	*0*	*0*	*0*	↓	-	-
13	*0*	*1*	*1*	*1*	*1*	↓	-	-
14	*1*	*0*	*0*	*0*	*0*	↑	-	-
15	*1*	*0*	*1*	*1*	*1*	↑	-	-
16	*0*	*1*	*0*	*0*	*1*	↓	-	↓
17	*0*	*1*	*0*	*1*	*0*	↓	↓	↑
18	*1*	*0*	*0*	*0*	*1*	↑	-	↓
19	*1*	*0*	*0*	*1*	*0*	↑	↓	↑
20	*0*	*1*	*0*	*1*	*1*	↓	↓	-
21	*1*	*0*	*0*	*1*	*1*	↑	↓	-
22	*1*	*1*	*1*	*0*	*0*	-	↑	-
23	*1*	*1*	*1*	*0*	*1*	-	↑	↓
24	*1*	*1*	*1*	*1*	*0*	-	-	↑
25	*1*	*1*	*0*	*0*	*0*	-	-	-
26	*1*	*1*	*1*	*1*	*1*	-	-	-

PWM algorithm to balance the capacitor voltages with right switching state selection. Fig. 4 shows all conduction paths of different states regarding the voltage level $+2V_{dc}/8$ that indicates the involved floating capacitors.

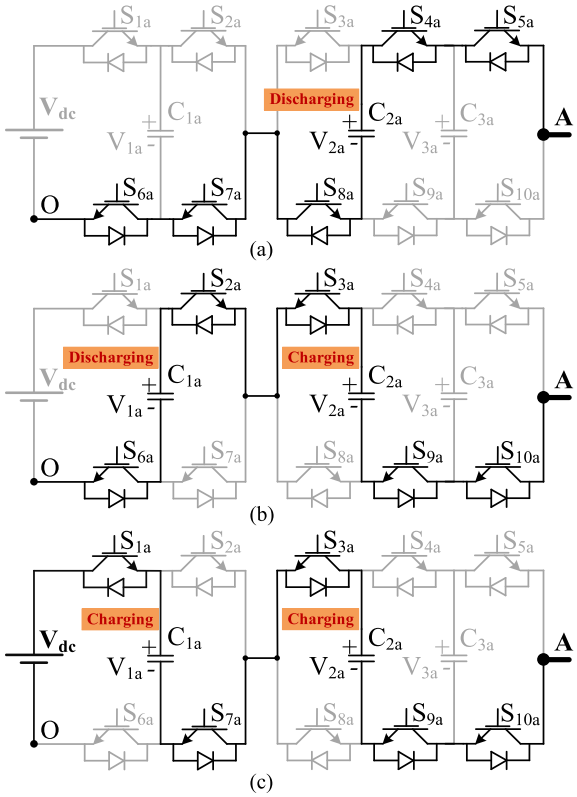

FIGURE 4. All conduction paths for different switching states of the voltage level; $+2V_{dc}/8$, and floating capacitor condition with respect to Tables 1 and 2. (a) State 5, (b) state 6, (c) state 7.

D. EXTENDING OF THE THREE-PHASE MODIFIED PUC INVERTER TOPOLOGY

The proposed three-phase packed multilevel inverter is extensible by the extension of the HPUC through adding more U-Cells. Fig. 5 shows a generalized structure of the single-dc-source three-phase modified PUC inverter for the m voltage level generation. For instance, 17 voltage levels are acquired by adding one extra U-Cell to the HPUC, which means that only two switches and one floating capacitor are added to the basic topology of Fig. 2. Therefore, the designed three-phase inverter has an optimized topology since a great number of voltage levels are generated, while few active and passive devices are included.

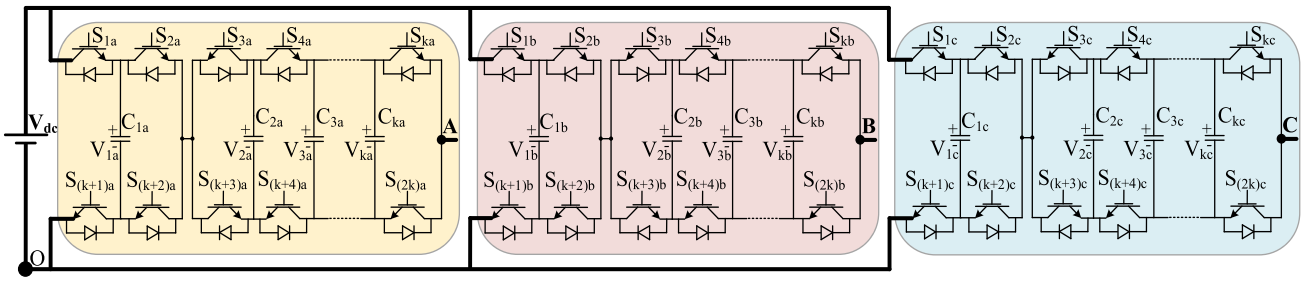

FIGURE 5. Extended circuit structure of the single-dc-source three-phase modified PUC inverter.

III. ACTIVE CAPACITOR VOLTAGE BALANCING ALGORITHM FOR STAND-ALONE AND GRID-CONNECTED OPERATIONS

A. FLOATING CAPACITOR VOLTAGE AMPLITUDE CALCULATIONS

As mentioned previously, first, second, and third capacitor voltages of each phase of Fig. 2 should be half, one-fourth, and one-eighth of main dc source, respectively. Indeed, their voltages are reducing by half with even coefficients, as V_1, V_2, and V_3 are (half, one-fourth, and one-eighth) of V_{dc}. Although this is a general procedure in multilevel inverters with the vertical capacitors' extension, there is no mathematical proof that their voltages are regulated in this way. In this article, the capacitor voltage amplitude calculation of the proposed three-phase inverter is done, but it can also be generalized for the other multilevel topologies. Since the three-phase dc–ac modified PUC is acting as a buck converter (like the other structures such as NPC, H-Bridge, PUC, PEC, etc.), the following equation is assumed valid:

$$V_{dc} > V_1 > V_2 > V_3. \tag{1}$$

The nine-level voltage can be written based on V_{dc}, V_1, V_2, and V_3 with respect to the switching states as (2). Then, it must be clarified that which V_{out} relationship of (2) belongs to which voltage level to calculate the capacitor voltage amplitudes. The highest, middle, and lowest voltage levels ($V_{dc}/8$, $4V_{dc}/8$, and $7V_{dc}/8$) are considered. 0 and $8V_{dc}/8$ are not assumed, as no capacitor is involved

$$\begin{cases} V_{out} = V_3 \\ V_{out} = V_2 - V_3 \\ V_{out} = V_2 \\ V_{out} = V_1 - V_2 \\ V_{out} = V_{dc} - V_1 - V_2 \\ V_{out} = V_1 - V_2 + V_3 \\ V_{out} = V_1 - V_3 \end{cases} \quad \begin{cases} V_{out} = V_{dc} - V_1 - V_2 + V_3 \\ V_{out} = V_{dc} - V_1 - V_3 \\ V_{out} = V_1 \\ V_{out} = V_1 \\ V_{out} = V_{dc} - V_1 \\ V_{out} = V_{dc} - V_1 \\ V_{out} = V_1 + V_3 \end{cases}$$

$$\times \begin{cases} V_{out} = V_1 + V_2 - V_3 \\ V_{out} = V_{dc} - V_1 + V_3 \\ V_{out} = V_{dc} - V_1 + V_2 - V_3 \\ V_{out} = V_1 + V_2 \\ V_{out} = V_{dc} - V_1 + V_2 \\ V_{out} = V_{dc} - V_2 \\ V_{out} = V_{dc} - V_2 + V_3 \\ V_{out} = V_{dc} - V_3. \end{cases} \tag{2}$$

By comparing V_{out} in (2), it will be found that

$$\begin{cases} V_{out} = V_1 + V_3 \\ V_{out} = V_1 + V_2 - V_3 \\ V_{out} = V_{dc} - V_1 + V_3 \\ V_{out} = V_{dc} - V_1 + V_2 - V_3 \\ V_{out} = V_1 + V_2 \\ V_{out} = V_{dc} - V_1 + V_2 \\ V_{out} = V_{dc} - V_2 \\ V_{out} = V_{dc} - V_2 + V_3 \\ V_{out} = V_{dc} - V_3 \end{cases} > \begin{cases} V_{out} = V_1 \\ V_{out} = V_{dc} - V_1 \end{cases}$$

$$> \begin{cases} V_{out} = V_3 \\ V_{out} = V_2 - V_3 \\ V_{out} = V_2 \\ V_{out} = V_1 - V_2 \\ V_{out} = V_{dc} - V_1 - V_2 \\ V_{out} = V_1 - V_2 + V_3 \\ V_{out} = V_1 - V_3 \\ V_{out} = V_{dc} - V_1 - V_2 + V_3 \\ V_{out} = V_{dc} - V_1 - V_3. \end{cases} \tag{3}$$

Here, it can be concluded that these two states of V_{out} ($V_{out} = V_1$ and $V_{out} = V_{dc} - V_1$) represent the middle voltage level ($4V_{dc}/8$). Consequently, equating ($V_1 = V_{dc} - V_1$), V_1 is obtained as $V_1 = V_{dc}/2$.

V_{out} for the highest voltage level ($7V_{dc}/8$) is as (4). By setting ($V_2 = (V_1 - V_2) = (V_{dc} - V_1 - V_2) = 7V_{dc}/8$), V_2 is $V_2 = V_1/2 = V_{dc}/4$

$$\begin{cases} V_{out} = V_3 \\ V_{out} = V_2 - V_3 \end{cases} < \begin{cases} V_{out} = V_2 \\ V_{out} = V_1 - V_2 \\ V_{out} = V_{dc} - V_1 - V_2 \end{cases}$$

$$> \begin{cases} V_{out} = V_1 - V_2 + V_3 \\ V_{out} = V_1 - V_3 \\ V_{out} = V_{dc} - V_1 - V_2 + V_3 \\ V_{out} = V_{dc} - V_1 - V_3 \\ V_{out} = V_1 \\ V_{out} = V_{dc} - V_1 \\ V_{out} = V_1 + V_3 \\ V_{out} = V_1 + V_2 - V_3 \end{cases} \text{ and}$$

$$\begin{cases} V_{\text{out}} = V_{\text{dc}} - V_1 + V_3 \\ V_{\text{out}} = V_{\text{dc}} - V_1 + V_2 - V_3 \\ V_{\text{out}} = V_1 + V_2 \\ V_{\text{out}} = V_{\text{dc}} - V_1 + V_2 \\ V_{\text{out}} = V_{\text{dc}} - V_2 \\ V_{\text{out}} = V_{\text{dc}} - V_2 + V_3 \\ V_{\text{out}} = V_{\text{dc}} - V_3 \end{cases}. \tag{4}$$

Also, the following equation is valid for the lowest voltage level ($V_{\text{dc}}/8$), where V_3 is also achieved: $V_3 = V_2/2 = V_{\text{dc}}/8$ by equating $(V_3 = V_2 - V_3) = V_{\text{dc}}/8$:

$$\begin{cases} V_{\text{out}} = V_3 \\ V_{\text{out}} = V_2 - V_3 \end{cases} < \left(\begin{cases} V_{\text{out}} = V_2 \\ V_{\text{out}} = V_1 - V_2 \\ V_{\text{out}} = V_{\text{dc}} - V_1 - V_2 \\ V_{\text{out}} = V_1 - V_2 + V_3 \\ V_{\text{out}} = V_1 - V_3 \\ V_{\text{out}} = V_{\text{dc}} - V_1 - V_2 + V_3 \\ V_{\text{out}} = V_{\text{dc}} - V_1 - V_3 \\ V_{\text{out}} = V_1 \\ V_{\text{out}} = V_{\text{dc}} - V_1 \end{cases} \right) \text{and}$$

$$\begin{cases} V_{\text{out}} = V_1 + V_3 \\ V_{\text{out}} = V_1 + V_2 - V_3 \\ V_{\text{out}} = V_{\text{dc}} - V_1 + V_3 \\ V_{\text{out}} = V_{\text{dc}} - V_1 + V_2 - V_3 \\ V_{\text{out}} = V_1 + V_2 \\ V_{\text{out}} = V_{\text{dc}} - V_1 + V_2 \\ V_{\text{out}} = V_{\text{dc}} - V_2 \\ V_{\text{out}} = V_{\text{dc}} - V_2 + V_3 \\ V_{\text{out}} = V_{\text{dc}} - V_3 \end{cases}. \tag{5}$$

B. FLOATING CAPACITOR VOLTAGE BALANCING ANALYSIS

In order to explain the necessity of engaging the switching state into PWM for capacitor voltage balancing, some mathematical analyses are done for the voltage level, $4V_{\text{dc}}/8$. The following equation expresses two states of $4V_{\text{dc}}/8$, where first capacitor voltage (V_1) is involved:

$$\begin{cases} V_{\text{out}} = V_1 = 4V_{\text{dc}}/8 \\ V_{\text{out}} = V_{\text{dc}} - V_1 = 4V_{\text{dc}}/8 \end{cases}. \tag{6}$$

Although V_1 should be equal to $V_{\text{dc}}/2$, it has some voltage ripple in practice as $V_1 = V_{\text{dc}}/2 + V_{\text{ripple}}$ that has to be controlled to well regulate V_1 to its dc amplitude. It can be shown that engaging redundant states with the PWM algorithm can accurately control V_{ripple} and balance the floating capacitor voltage. To this end, a predefined nine-level voltage waveform is assumed as Fig. 6 to perform the theoretical analysis on V_1. Applying Fourier series on the nine-level voltage of Fig. 6, V_{out} can be written as

$$V_{\text{out}} = a_0 + \sum_{n=1}^{\infty} a_n \cos(nt) + \sum_{n=1}^{\infty} b_n \sin(nt) \tag{7}$$

where a_0, a_n, and b_n ($n = 1,3\ 5,\ 7,\ 9, \ldots$) are calculated as follows:

$$a_0 = \frac{V_{\text{dc}}}{2},\ a_n = 0, b_n = \frac{V_{\text{dc}}}{2n\pi} \begin{bmatrix} \cos(n\alpha_1) + \cos(n\alpha_2) \\ + \cos(n\alpha_3) + \cos(n\alpha_4) \end{bmatrix}. \tag{8}$$

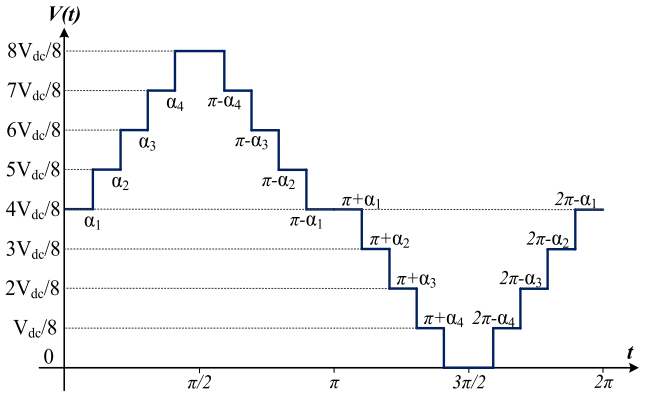

FIGURE 6. Predefined fundamental frequency nine-level voltage waveform.

Therefore, V_{out} of Fig. 6 can be written as

$$V_{\text{out}} = \sum_{n=1}^{\infty} \left[\frac{V_{\text{dc}}[\cos(n\alpha_1) + \cos(n\alpha_2) + \cos(n\alpha_3) + \cos(n\alpha_4)]}{2n\pi} \right] \sin(nt). \tag{9}$$

Considering Fig. 6, $V_{\text{out}} = 4V_{\text{dc}}/8$ is in the following time interval:

$$\begin{cases} V_{\text{out}} = 4V_{\text{dc}}/8 \\ 0 < t < (\alpha_1/2\pi f) \\ ((\pi - \alpha_1)/2\pi f) < t < ((\pi + \alpha_1)/2\pi f) \\ ((2\pi - \alpha_1)/2\pi f) < t < (2\pi/2\pi f) \end{cases} \tag{10}$$

where f is the output voltage's fundamental frequency. To determine V_1, it is first required to obtain the relationship between first capacitor current (I_1) and output current (I_{out}) for the redundant states of $4V_{\text{dc}}/8$. The relationship between I_1 and I_{out} is as follows:

$$\begin{cases} V_{\text{out}} = V_1 \Rightarrow I_1 = -I_{\text{out}} \\ V_{\text{out}} = V_{\text{dc}} - V_1 \Rightarrow I_1 = +I_{\text{out}}. \end{cases} \tag{11}$$

Substituting $I_{\text{out}} = V_{\text{out}}/Z$ (Z is the impedance of output load, and $I_1 = C_1 dV_1/dt$), (11) will be as follows:

$$C_1 \frac{dV_1}{dt} = \pm \frac{V_{\text{out}}}{Z} \tag{12}$$

where $\pm$ represents the current direction; hence, V_1 voltage ripple is acquired using the following equations:

$$V_1 = \pm \int_0^t \frac{V_{\text{out}}}{ZC_1} dt \tag{13}$$

where t is the time interval of (10). Considering negative and positive current direction ($I_1 = -I_{\text{out}}$ and $I_1 = +I_{\text{out}}$), V_1 is

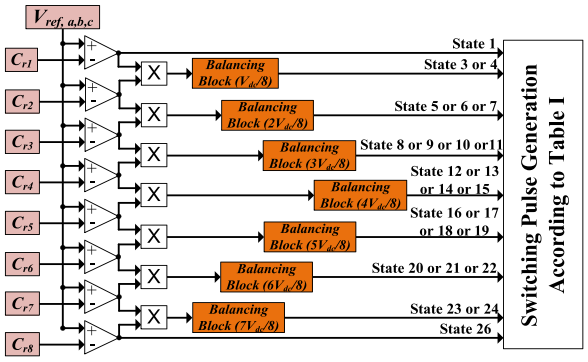

FIGURE 7. Diagram of the level-shift PWM technique integrated into the floating capacitor voltage balancing blocks for the nine-level three-phase modified PUC inverter.

obtained as (14) for each time interval of (10)

$$\begin{cases} V_1 = \frac{V_{dc}}{2} \underbrace{\mp \dfrac{\left[\frac{V_{dc}}{2}\alpha_1 - 1 + \sum_{n=1}^{\infty}\frac{b_n}{n}\cos(n\alpha_1)\right]}{C_1 Z}}_{V_{ripple}}, & 0 < t < \alpha_1 \\ V_1 = \frac{V_{dc}}{2} \underbrace{\mp \dfrac{[V_{dc}\alpha_1]}{C_1 Z}}_{V_{ripple}}, & \pi - \alpha_1 < t < \pi + \alpha_1 \\ V_1 = \frac{V_{dc}}{2} \underbrace{\mp \dfrac{\left[\frac{V_{dc}}{2}\alpha_1 + \sum_{n=1}^{\infty}\frac{b_n}{n} - \sum_{n=1}^{\infty}\frac{b_n}{n}\cos(n\alpha_1)\right]}{C_1 Z}}_{V_{ripple}}, & \\ 2\pi - \alpha_1 < t < 2\pi. & \end{cases} \tag{14}$$

It is clear that V_{ripple} of the first capacitor has a positive value for each time interval when current is positive that means V_1 exceeds $V_{dc}/2$. On the contrary, V_{ripple} has a negative value for each time interval when current is negative that means V_1 drops below $V_{dc}/2$. Indeed, V_{ripple} shows charging/discharging conditions of the first capacitor, so both states must be integrated into the PWM technique to balance C_1 energy and to regulate V_1 to $V_{dc}/2$.

C. DESIGNED PWM ALGORITHM FOR ACTIVE FLOATING CAPACITOR VOLTAGE BALANCING

Fig. 7 shows a diagram of the designed level-shift PWM method integrated with the capacitor voltage balancing mechanism for the three-phase nine-level modified PUC. C_{r1}–C_{r8} are the triangle waveforms as the carrier signal, which are level-shifted between –1 and 1, and V_{ref} is the sinusoidal waveform as the reference signal. The floating capacitor voltages are regulated by balancing blocks. Each balancing block contains redundant switching states for an output voltage level, including $V_{dc}/8$, $2V_{dc}/8$, $3V_{dc}/8$, $4V_{dc}/8$, $5V_{dc}/8$, $6V_{dc}/8$, and $7V_{dc}/8$, to regulate the floating capacitor voltages. For instance, Fig. 8 illustrates an example of an algorithm diagram for the redundant switching state selection mechanism in the balancing block regarding to the output voltage level $3V_{dc}/8$. Thanks to the balancing block, the redundant switching states related to the output voltage level $3V_{dc}/8$ are selected as to adjust the charging and discharging of the involved capacitors and, therefore, to regulate their voltages. If the capacitor voltage is increasing, the redundant switching states for discharging condition are chosen and vice versa, so that the capacitor voltages are adjusted to their right dc values with an appropriate voltage ripple. The remaining balancing blocks for other output voltage levels follow a similar approach to establish the switching state selection mechanism using Tables 1 and 2 and, therefore, to regulate all floating capacitor voltages to their desired dc values. It is important to clarify that voltage balancing refers to the regulation of each capacitor to its dc voltage ($V_{dc}/2$, $V_{dc}/4$, and $V_{dc}/8$), forming a proportional or hierarchical voltage distribution. The balancing mechanism ensures that each capacitor remains within an acceptable ripple range of its set point, rather than enforcing identical voltages.

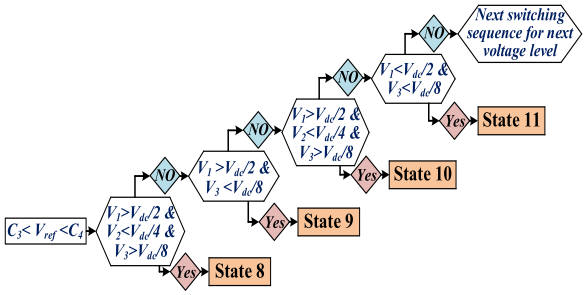

FIGURE 8. Example of the redundant switching state selection mechanism for capacitor voltage regulation in the balancing block of the designed PWM technique of Fig. 7.

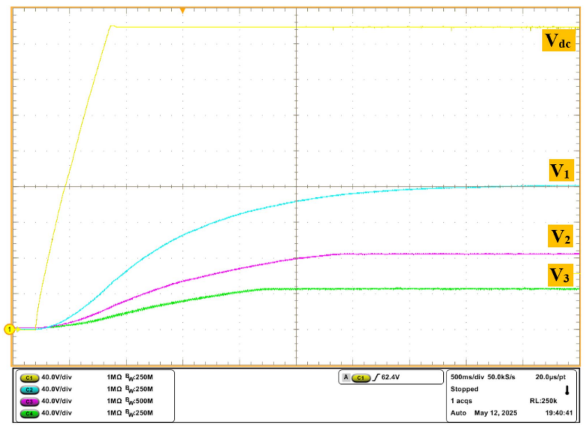

FIGURE 9. Experimental results of main dc source (V_{dc}) and dc capacitor voltages (V_1, V_2, and V_3) of Fig. 3 under start-up operation while switching frequency is 5 kHz, (CH1: V_{dc}; CH2: V_1; CH3: V_2; CH4: V_3, all 40 V/Div).

Fig. 9 shows the experimental results of the dc source (V_{dc}) and capacitor voltages (V_1, V_2, and V_3) of single-phase modified PUC under start-up condition. As a result of the balancing blocks integrated into the designed PWM method, when V_{dc} suddenly rises from 0 to 340 V as a start-up operation, V_1, V_2,

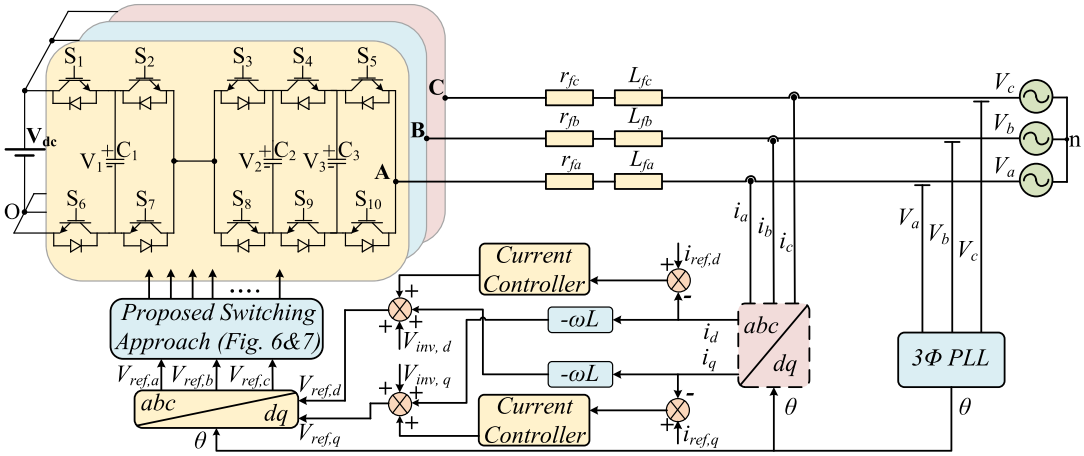

FIGURE 10. Current control strategy diagram for the grid-connected operation of the single-dc-source three-phase modified PUC inverter.

and V_3 start to charge up to their dc values 170, 85, and 42.5 V, respectively.

D. PROPOSED CURRENT CONTROL FRAMEWORK FOR THE THREE-PHASE GRID-CONNECTED MODE OF OPERATION

Fig. 10 depicts the designed control strategy diagram including current control and grid synchronization for the single-dc-source three-phase grid-connected modified PUC inverter. (i_a, i_b, and i_c) are the three-phase currents that are injected by the inverter to the grid. (r_{fa}, r_{fb}, and r_{fc}) and (L_{fa}, L_{fb}, and L_{fc}) are also resistance and inductance parts of the grid filter respectively. As the three-phase currents of the inverter must be synchronized with the three-phase voltages of the grid to ensure the pure active power delivery, a phase-locked loop (PLL) is employed to extract the phase angle (θ) of the grid voltage. Therefore, the three-phase current references are established using the phase angles of the grid voltage to control the reactive power while injecting pure active power. According to the designed three-phase grid-connected proportional–integral (PI)-based controller of Fig. 10, the three-phase measured currents (i_a, i_b, and i_c) are transformed into the synchronous reference (dq) frame. Applying the obtained phase angle of the grid voltage and using ($abc \rightarrow qd$) transformation, the three-phase measured and desired currents are converted from ac into dc components as follows:

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos(\theta) & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ -\sin(\theta) & -\sin(\theta - \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}. \tag{15}$$

Using Kirchhoff's Voltage Law, the dynamics model of the grid-connected system in the dq frame is also presented as follows:

$$\begin{aligned} L\frac{di_d}{dt} &= -Ri_d + \omega L i_q - V_{\text{ref},d} + V_{\text{inv},d} \\ L\frac{di_q}{dt} &= -Ri_q - \omega L i_d - V_{\text{ref},q} + V_{\text{inv},q} \end{aligned} \tag{16}$$

where ω is the grid frequency and ($V_{\text{ref},d}$ and $V_{\text{ref},\,q}$) are the dq components of the demanded reference voltages, which must be desirably generated. ($V_{\text{inv},d}$ and $V_{\text{inv},\,q}$) are also the dq components of the three-phase voltages of the inverter, which is achieved from (V_{An}, V_{Bn}, and V_{Cn}). Afterward, the errors between the desired currents components ($i_{\text{ref},q}$ and $i_{\text{ref},d}$) and the actual current components (i_q and i_d) are compensated by the current controller blocks using two PI control systems. Hence, the designed current control structure in the dq frame is given as follows:

$$\begin{aligned} V_{\text{ref},d} &= \omega L i_q + V_{\text{inv},d} + K_p e_d + K_I \int e_d(\tau) d\tau \\ V_{\text{ref},q} &= -\omega L i_d + V_{\text{inv},q} + K_p e_q + K_I \int e_q(\tau) d\tau \end{aligned} \tag{17}$$

where $K_P$is the proportional gain, $K_I$is the integral gain, $e_d = i_{\text{ref},d} - i_d$, and $e_q = i_{\text{ref},q} - i_q$. By compensating the obtained error between i_q and its reference $i_{\text{ref},q}$, the reactive power is controlled so that the unity power factor is ensured. The amount of the active power is also controlled by compensating the error between i_d and its reference $i_{\text{ref},d}$ so that the desired amount of the active power is delivered to the grid. The controlled signals are then retransformed into three-phase control signals using an inverse Park transformation ($dq \rightarrow abc$) to obtain the three-phase reference signals ($V_{\text{ref},\,a}$, $V_{\text{ref},\,b}$, and $V_{\text{ref},\,c}$). The three-phase reference signals are

$$\begin{bmatrix} V_{\text{ref},a} \\ V_{\text{ref},b} \\ V_{\text{ref},c} \end{bmatrix} = \begin{bmatrix} \cos(\theta) & -\sin(\theta) & 1 \\ \cos\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta - \frac{2\pi}{3}\right) & 1 \\ \cos\left(\theta + \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) & 1 \end{bmatrix} \begin{bmatrix} V_{\text{ref},d} \\ V_{\text{ref},q} \\ V_{\text{ref},0} \end{bmatrix}. \tag{18}$$

These generated three-phase sinewaves ($V_{\text{ref},\,a}$, $V_{\text{ref},\,b}$, and $V_{\text{ref},\,c}$) will be added to the proposed PWM switching method as the reference signals to be compared with carrier signals (C_{r1}–C_{r8}), as illustrated in Fig. 7, to generate the firing pulses for the three-phase inverter's switches. The active

TABLE 3. Circuit Device Analysis Between Single-DC-Source Three-Phase Nine-Level Modified PUC Inverter and Other Similar Nine-Level Topologies

Type of Inverter	*Power Switch*	*Auxiliary Capacitor*	*Power Diode*	*Control Complexity*
NPC	*8*	*4*	*6*	*Very High*
FC	*16*	*8*	*0*	*Very High*
ANPC	*12*	*5*	*0*	*High*
MMC-Half Bridge	*16*	*8*	*0*	*Very High*
MMC-Full Bridge	*32*	*8*	*0*	*Very High*
Hybrid FC and HB in [30]	*12*	*3*	*0*	*High*
Hybrid six-switch and HB in [23]	*14*	*3*	*0*	*Very High*
Modified PUC	*10*	*3*	*0*	*Very Low*

floating capacitor voltage balancing is still achieved through the balancing blocks using the redundant switching states.

IV. COMPARATIVE ANALYSIS OF THE THREE-PHASE MODIFIED PUC

The single-dc-source three-phase nine-level modified PUC inverter has reduced total devices, while it generates more output stepped voltage. Moreover, it could solve the main problem of the conventional three-phase PUC inverter, which was the multi-dc-source structure. In order to further investigate that the proposed three-phase inverter has an optimized circuit, it is analytically compared to other single-dc-source three-phase multilevel inverter topologies such as NPC, FC, ANPC, and Modular Multilevel Converter (MMC) based on both half- and full-bridge submodules. Table 3 lists total active and passive components for the three-phase nine-level modified PUC inverter and similar three-phase nine-level topologies. According to the comparative analysis, the nine-level modified PUC inverter has a notably lower number of circuit devices in comparison to the other single-dc-source three-phase nine-level inverters. A reduced number of active semiconductor devices generally result in lower switching losses. Although a detailed switching loss analysis is not the focus of this work, the reduced number of switches (as presented in Table 3), combined with lower voltage stress on the devices and strategic switching state selection, indicates that the proposed modified PUC inverter likely offers lower switching losses compared to other three-phase multilevel inverter counterparts. Despite this, its prominent advantage lies in the active capacitor voltage balancing achieved through redundant switching state selection, which classifies it as a three-phase power converter with a very low complexity level for the designed control technique. Thanks to the active capacitor voltage balancing capability as well as high voltage gain and multilevel voltage output features, the proposed single-dc-source three-phase modified PUC inverter is also a strong candidate for solid-state transformer (SST) front-/back-end stages. Its compact structure, reduced component count, and compatibility with medium-frequency transformers make it well suited for efficient and flexible SST architectures operating in both stand-alone and grid-connected modes of operations.

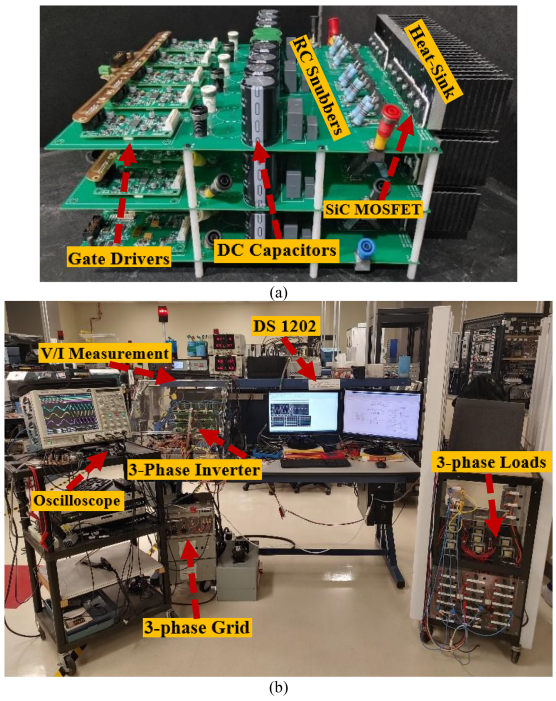

FIGURE 11. Laboratory prototype and experimental setup of the three-phase nine-level modified PUC inverter used for experimental validation for both stand-alone and grid-connected operations. (a) Laboratory prototype. (b) Experimental setup.

V. EXPERIMENTAL VALIDATION AND DISCUSSION OF THE SINGLE-DC-SOURCE THREE-PHASE NINE-LEVEL MODIFIED PUC INVERTER

The single-dc-source three-phase packed multilevel inverter is experimentally verified for stand-alone and grid-connected operations. The experimental tests include three-phase linear-balanced loads, the output load change, the amplitude MI variation, fundamental frequency change, and variable and steady grid current operation. These tests are done to validate the excellent regulation of the floating capacitor voltages regardless of the operation condition. Fig. 11(a) depicts the prototype of the three-phase nine-level modified PUC. Fig. 11(b) also shows the experimental setup of the modified PUC inverter for both stand-alone and grid-connected operations. The three-phase inverter's power switches are chosen as SiC MOSFET, C3M0120090D, and are controlled through the implementation of the proposed three-phase level-shift PWM method of Fig. 7 and the designed three-phase grid-connected control technique of Fig. 10 in a MicroLab Box 1202 setup. The OPAL-RT high-voltage/-current measurement is also utilized to measure single-dc-source and dc capacitor voltages as well as grid voltage and current. Moreover, the parameters of the experimental tests for the stand-alone and grid-connected operations are listed in Table 4.

A. THREE-PHASE LINEAR AND BALANCED LOAD

As the first step, the presented modified PUC inverter is tested with the three-phase linear-balanced *RL* loads (under

TABLE 4. Experimental Test Parameters of the Three-Phase Modified PUC Inverter

Input DC Voltage	$340V_{dc}$
Grid AC Voltage	$120V_{rms}$
DC Capacitors Capacitance	*2040uF*
Linear R-L load (for each phase)	*80Ω & 5mH*
Fundamental and Switching Frequency	*60Hz & 5kHz*
Amplitude Modulation Index	*0.9*

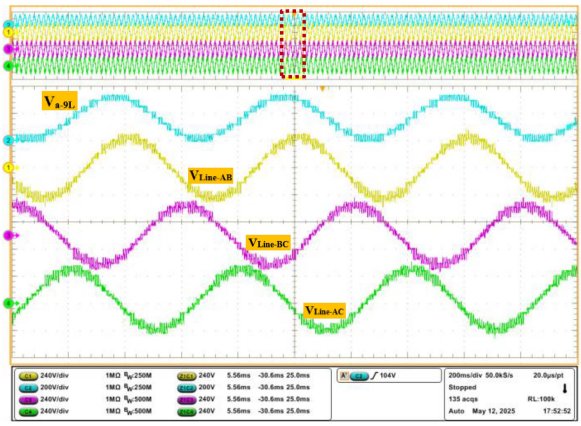

FIGURE 12. Nine-level and three-phase line voltage waveforms of the stand-alone three-phase modified PUC inverter under linear and symmetrical load condition, (CH1: nine-level voltage, 100 V/Div; CH2, 3, and 4: three-phase line voltages, 110 V/Div).

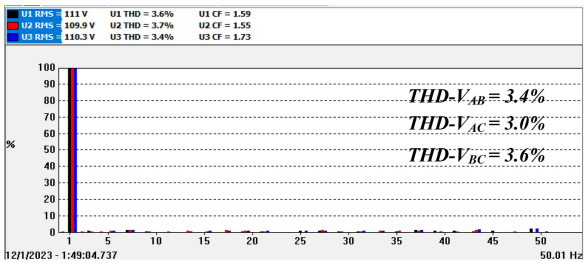

FIGURE 13. Harmonic content of three-phase line voltage waveforms of Fig. 12.

same test parameter of Table 4). Fig. 12 shows a nine-level voltage of phase A (V_{AO}) and three-phase line voltages (V_{AB}, V_{BC}, and V_{CA}). As it can be perceived from the obtained results of Fig. 12, the nine-level voltage waveform is perfectly generated according to the switching sequence of Table 1 that leads to an appropriate 17-level line voltage waveform as well. Considering the line voltage waveforms, it can be concluded that all dc capacitor voltages are properly regulated to their dc values. Fig. 13 displays the harmonic content (up to 49th) of three-phase line voltage waveforms of Fig. 12. The obtained total harmonic distortion (THD) is as low as (approximately) ~ 4%, which means that ac output filter is not required.

B. OUTPUT LOAD CHANGE OPERATION

For the first dynamical stand-alone operation, the floating capacitor voltage balancing of the designed three-phase inverter is tested under output load change. To this end, the resistive part of one phase load (phase A) is changed from

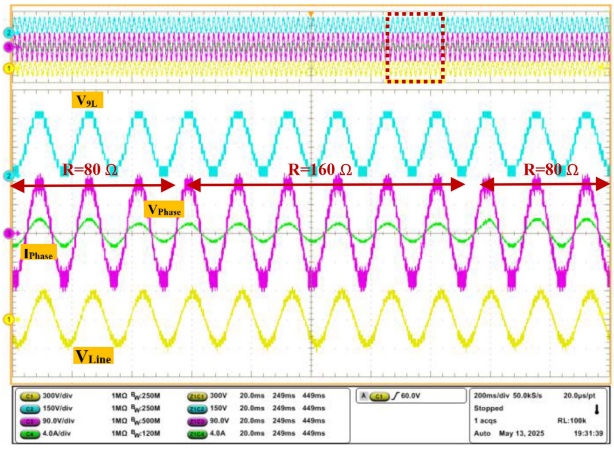

FIGURE 14. Output variables of the stand-alone three-phase modified PUC inverter, (nine-level, phase, line voltages, and phase current) under output load change operation, (CH1: nine-level voltage, 120 V/Div; CH2: line voltages, 120 V/Div; CH3: phase voltage, 45 V/Div; CH4: phase current, 1.5 A/Div).

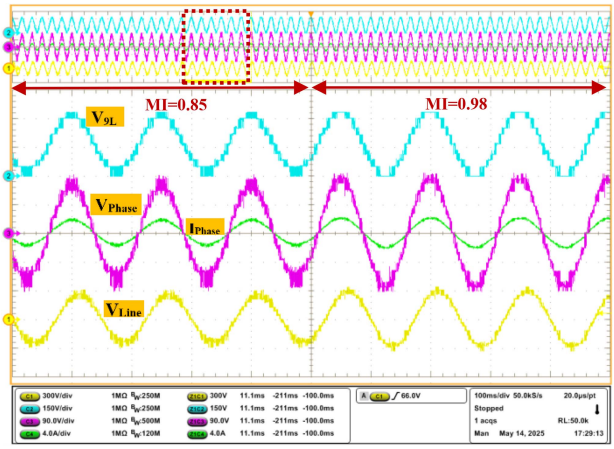

FIGURE 15. Output variables of the stand-alone three-phase modified PUC inverter, (nine-level, phase, line voltages, and phase current) under MI change, (CH1: nine-level voltage, 120 V/Div; CH2: line voltages, 120 V/Div; CH3: phase voltage, 45 V/Div; CH4: phase current, 1.5 A/Div).

80 to 160 Ω and again to 80 Ω. Fig. 14 shows the nine-level, phase, line voltage, and load current waveforms under dynamical load conditions. The load current responds to the load change, while all dc capacitor voltages remained balanced at their dc amplitude as can be seen from proper generation of output stepped voltages. Therefore, the performance of the three-phase modified PUC inverter is robust against the uncertainties of the load changes. In other words, the floating capacitor voltage regulation is independent of the current direction or current changes.

C. AMPLITUDE MI VARIATION

The proposed single-dc-source three-phase nine-level inverter is also tested under amplitude MI changes for stand-alone operation. Fig. 15 indicates the nine-level, phase, line voltage, and phase current waveforms when the MI varies from 0.85 to 0.98. As can be seen, pulsewidth and the number of voltage

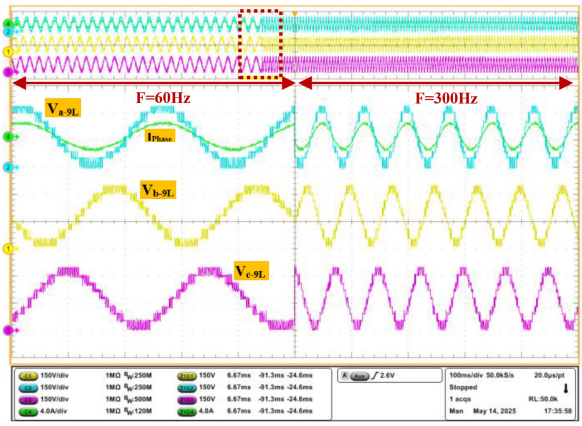

FIGURE 16. Output variables of the stand-alone three-phase modified PUC inverter, (nine-level, phase, line voltages, and phase current) under fundamental frequency change, (CH1, 2, and 3: three-phase nine-level voltages, 80 V/Div; CH4: phase current, 2 A/Div).

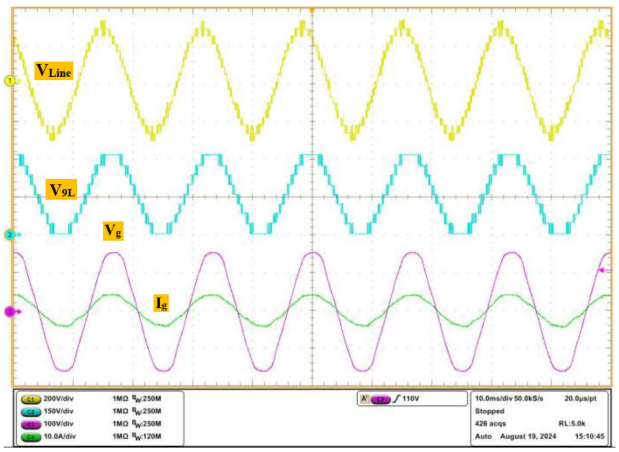

FIGURE 17. Output variables of the three-phase grid-connected modified PUC inverter (line and nine-level voltages and grid voltage/current) under normal grid-connected operation, (CH1: line voltage 200 V/Div; CH2: nine-level voltages, 150 V/Div; CH3 and CH4: grid voltage/current, 100 V/Div and 10 A/Div).

levels vary because of MI variations. However, the floating capacitor voltages are kept balanced regardless of the MI changes.

D. SYSTEM FUNDAMENTAL FREQUENCY CHANGES

Since multilevel inverters must be operational for different system fundamental frequency, the three-phase modified PUC inverter is tested under fundamental frequency changes to verify its performance for a more electric aircraft application. Fig. 16 demonstrates the three-phase nine-level voltages and output phase current waveforms when the fundamental frequency changes from 60 to 300 Hz. The output load is a three-phase linear and symmetrical (*RL*) with values listed in Table 4. As shown in Fig. 16, the output voltage and current variables have a stable performance under fundamental frequency changes as the dc capacitor voltages remained regulated at their dc values.

E. GRID-CONNECTED OPERATION OF THE THREE-PHASE SYSTEM

As the last performance validation analysis, the modified PUC inverter has been experimentally tested for three-phase grid-connected operation, which is controlled based on the designed current controller of Section III-A. The dc-source voltage has been adjusted to 340 V, and the grid voltage is $120V_{\text{rms}}$. Fig. 17 displays the output variables of the three-phase grid-connected modified PUC inverter including the line and nine-level voltages as well as the grid voltage/current, where the current reference has been set constant to 4 A. As can be seen from Fig. 17, the capacitor voltages are balanced as the output stepped voltages are perfectly generated, while the three-phase grid connectivity requirements are met as the grid voltage/current waveforms are in phase.

Fig. 18 also demonstrates the experimental results of the three-phase grid-connected modified PUC inverter including line and nine-level voltages along with grid voltage/current under dynamic grid current operation. To this end,

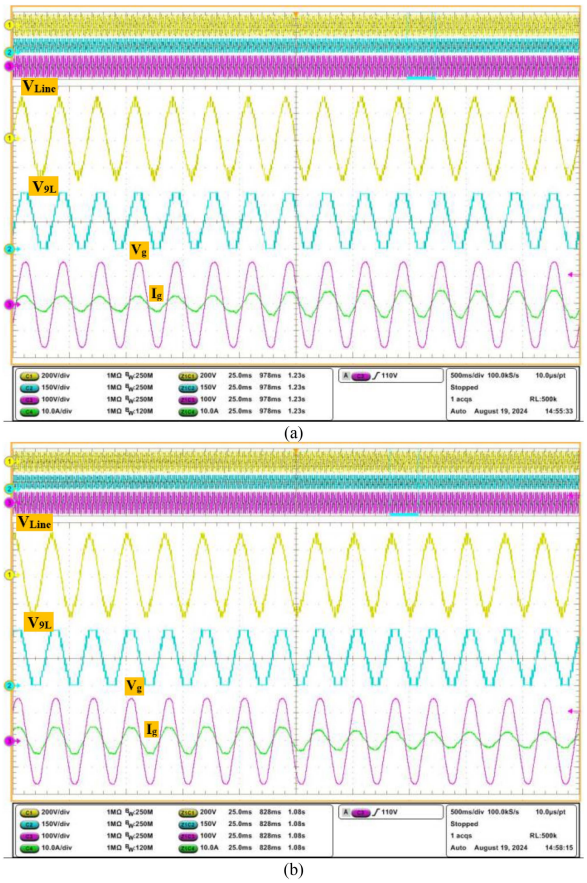

FIGURE 18. Output variables of the three-phase grid-connected modified PUC inverter (line and nine-level voltages and grid voltage/current) under dynamical grid-connected operation. (a) Increasing the current reference (4 to 6 A). (b) Decreasing the current reference (6 to 4 A), (CH1: line voltage 200 V/Div; CH2: nine-level voltages, 150 V/Div; CH3 and CH4: grid voltage/current, 100 V/Div and 10 A/Div).

Fig. 18(a) indicates the experimental results related to the grid-connected operation condition when the current reference increases from 4 to 6 A, and Fig. 18(b) demonstrates the experimental results when the current reference decreases from 6 to 4 A. Considering that the output stepped voltage waveforms of Fig. 18 are well formed, the capacitor voltages are kept balanced under dynamical grid-connected operation, while the grid connectivity requirements are fulfilled for the three-phase inverter even though the current reference changes.

VI. CONCLUSION

In this article, a novel modified PUC topology has been introduced by cascading the FC cell and the HPUC to establish a single-dc-source three-phase packed multilevel inverter and, therefore, to overcome the drawbacks of the multi-dc-source structure in their conventional three-phase configuration. According to the designed three-phase modified PUC inverter, the single FC cell is connected to the HPUC unit in each phase where the three-phase configuration is fed by a single dc source. Thanks to the cascaded connection of FC and HPUC units, there are abundant redundant switching states, where floating capacitor voltages are actively balanced within acceptable voltage ripple with no need of the external voltage regulator. To this end, the voltage ripple of V_1 was measured to be within $\pm 2.3\%$ of $V_{dc}/2$, while the voltage ripple of V_2 and V_3 are remained within $\pm 5\%$ of $V_{dc}/4$ and of $V_{dc}/8$, respectively, under all tested load and operating conditions, including load steps, MI variation, and frequency change, confirming effective regulation of capacitor voltage using the proposed balancing blocks. Indeed, the designed voltage balancing mechanism, based on redundant switching state selection within the PWM framework, offers inherent robustness even under such nonidealities. The HPUC unit is also extendable by adding more U-Cells to generalize the circuit structure of the proposed single-dc-source three-phase packed multilevel inverter. Comparative study shows that the single-dc-source three-phase modified PUC inverter has an optimized structure as it has fewer active and passive components compared to other similar single-dc-source three-phase multilevel inverter topologies. The theoretical analyses along with experimental validations prove excellent performance of the three-phase modified PUC inverter in dealing with different stand-alone and grid-connected operation conditions, as capacitor voltages are actively balanced to their determined dc voltage amplitudes.

REFERENCES

[1] E. S. Asl, E. Babaei, M. Sabahi, M. H. B. Nozadian, and C. Cecati, "New half-bridge and full-bridge topologies for a switched-boost inverter with continuous input current," *IEEE Trans. Ind. Electron.*, vol. 65, no. 4, pp. 3188–3197, Apr. 2018.

[2] P. K. Jain and S. B. Dewan, "A performance comparison of full- and half-bridge series resonant inverters in high-frequency high-power applications," *IEEE Trans. Ind. Appl.*, vol. 26, no. 2, pp. 317–323, Mar./Apr. 1990.

[3] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Pérez, "A survey on cascaded multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2197–2206, Jul. 2010.

[4] J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738,Aug. 2002.

[5] G.-J. Su, "Multilevel DC-link inverter," *IEEE Trans. Ind. Appl.*, vol. 41, no. 3, pp. 848–854, May/Jun. 2005.

[6] M. Trabelsi, H. Vahedi, and H. Abu-Rub, "Review on single-DC-source multilevel inverters: Topologies, challenges, industrial applications, and recommendations," *IEEE Open J. Ind. Electron. Soc.*, vol. 2, pp. 112–127, 2021.

[7] J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama, "A survey on neutral-point-clamped inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2219–2230, Jul. 2010.

[8] J. Huang and K. A. Corzine, "Extended operation of flying capacitor multilevel inverters," *IEEE Trans. Power Electron.*, vol. 21, no. 1, pp. 140–147, Jan. 2006.

[9] M. Mehrasa, M. Babaie, A. Zafari, and K. Al-Haddad, "Passivity ANFIS-based control for an intelligent compact multilevel converter," *IEEE Trans. Ind. Informat.*, vol. 17, no. 8, pp. 5141–5151, Aug. 2021.

[10] Y. Ounejjar, K. Al-Haddad, and L. Gregoire, "Packed U cells multilevel converter topology: Theoretical study and experimental validation," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1294–1306, Apr. 2011.

[11] M. Sharifzadeh and K. Al-Haddad, "Packed E-cell (PEC) converter topology operation and experimental validation," *IEEE Access*, vol. 7, pp. 93049–93061, 2019.

[12] J. S. M. Ali and V. Krishnasamy, "Compact switched capacitor multilevel inverter (CSCMLI) with self-voltage balancing and boosting ability," *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4009–4013, May 2019.

[13] A. N. Babadi, O. Salari, M. J. Mojibian, and M. T. Bina, "Modified multilevel inverters with reduced structures based on packed U-cell," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 6, no. 2, pp. 874–887, Jun. 2018.

[14] K.-M. Kim, J.-K. Han, and G.-W. Moon, "A high step-up switched-capacitor 13-level inverter with reduced number of switches," *IEEE Trans. Power Electron.*, vol. 36, no. 3, pp. 2505–2509, Mar. 2021.

[15] A. Taghvaie, J. Adabi, and M. Rezanejad, "A self-balanced step-up multilevel inverter based on switched-capacitor structure," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 199–209, Jan. 2018.

[16] R. Barzegarkhoo, H. M. Kojabadi, E. Zamiry, N. Vosoughi, and L. Chang, "Generalized structure for a single phase switched-capacitor multilevel inverter using a new multiple DC link producer with reduced number of switches," *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5604–5617, Aug. 2016.

[17] J. Salmon, A. M. Knight, and J. Ewanchuk, "Single-phase multilevel PWM inverter topologies using coupled inductors," *IEEE Trans. Power Electron.*, vol. 24, no. 5, pp. 1259–1266, May 2009.

[18] S. S. Lee, "A single-phase single-source 7-level inverter with triple voltage boosting gain," *IEEE Access*, vol. 6, pp. 30005–30011, 2018.

[19] D. G. Holmes and B. P. McGrath, "Opportunities for harmonic cancellation with carrier-based PWM for a two-level and multilevel cascaded inverters," *IEEE Trans. Ind. Appl.*, vol. 37, no. 2, pp. 574–582, Mar./Apr. 2001.

[20] O. Ojo, "The generalized discontinuous PWM scheme for three-phase voltage source inverters," *IEEE Trans. Ind. Electron.*, vol. 51, no. 6, pp. 1280–1289, Dec. 2004.

[21] S. G. Song, F. S. Kang, and S. Park, "Cascaded multilevel inverter employing three-phase transformers and single DC input," *IEEE Trans. Ind. Electron.*, vol. 56, no. 6, pp. 2005–2014, Jun. 2009.

[22] T. Qanbari and B. Tousi, "Single-source three-phase multilevel inverter assembled by three-phase two-level inverter and two single-phase cascaded H-bridge inverters," *IEEE Trans. Power Electron.*, vol. 36, no. 5, pp. 5204–5212, May 2021.

[23] K.-M. Tsang and W.-L. Chan, "Single DC source three-phase multilevel inverter using reduced number of switches," *IET Power Electron.*, vol. 7, no. 4, pp. 775–783, 2013.

[24] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Appl.*, vol. IA-17, no. 5, pp. 518–523, Sep. 1981.

[25] N. Hatti, Y. Kondo, and H. Akagi, "Five-level diode-clamped PWM converters connected back-to-back for motor drives," *IEEE Trans. Ind. Appl.*, vol. 44, no. 4, pp. 1268–1276, Jul./Aug. 2008.

[26] B. Vafakhah, J. Ewanchuk, and J. Salmon, "Multicarrier interleaved PWM strategies for a five-level NPC inverter using a three-phase coupled inductor," *IEEE Trans. Ind. Appl.*, vol. 47, no. 6, pp. 2549–2558, Nov./Dec. 2011.
[27] Y. Liang and C. O. Nwankpa, "A power-line conditioner based on flying-capacitor multilevel voltage-source converter with phase-shift SPWM," *IEEE Trans. Ind. Appl.*, vol. 36, no. 4, pp. 965–971, Jul./Aug. 2000.
[28] S. R. Pulikanti and V. G. Agelidis, "Hybrid flying-capacitor-based active-neutral-point-clamped five-level converter operated with SHE-PWM," *IEEE Trans. Ind. Electron.*, vol. 58, no. 10, pp. 4643–4653, Oct. 2011.
[29] J. Li, S. Bhattacharya, and A. Q. Huang, "A new nine-level active NPC (ANPC) converter for grid connection of large wind turbines for distributed generation," *IEEE Trans. Power Electron.*, vol. 26, no. 3, pp. 961–972, Mar. 2011.
[30] P. Roshankumar, P. P. Rajeevan, K. Mathew, K. Gopakumar, J. I. Leon, and L. G. Franquelo, "A five-level inverter topology with single-DC supply by cascading a flying capacitor inverter and an H-bridge," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3505–3512, Aug. 2012.
[31] A. Taghvaie, J. Adabi, and M. Rezanejad, "Circuit topology and operation of a step-up multilevel inverter with a single DC source," *IEEE Trans. Ind. Electron.*, vol. 63, no. 11, pp. 6643–6652, Nov. 2016.

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