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MPC Design and Comparative Analysis of Single-Phase 7-Level PUC and 9-Level CSC Inverters for Grid Integration of PV Panels

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Abstract

In this study, a novel comparison between single phase 7-Level Packed U—Cell (PUC) inverter and single phase 9-Level Cross Switches Cell (CSC) inverter with Model Predictive Controller (MPC) for solar grid-tied applications is presented. Our innovation introduces a unique approach by integrating PV solar panels in PUC and CSC inverters in their two DC links rather than just one which increases power density of the system. Another key benefit for the proposed models lies in their simplified design, offering improved power quality and reduced complexity relative to traditional configurations. Moreover, both models feature streamlined control architectures that eliminate the need for additional controllers such as PI controllers for grid reference current extraction. Furthermore, the implementation of Maximum Power Point Tracking (MPPT) technology directly optimizes power output from the PV panels, negating the necessity for a DC-DC booster converter during integration. To validate the proposed concept's performance for both inverters, extensive simulations were conducted using MATLAB/Simulink, assessing both inverters under steady-state conditions as well as various disturbances to evaluate its robustness and dynamic response. Both inverters exhibit robustness against variations in grid voltage, phase shift, and irradiation. By comparing both inverters, results demonstrate that the CSC inverter exhibits superior performance due to its booster feature which relies on generating voltage level greater than the DC input source. This primary advantage makes CSC a booster inverter.

Keywords: multilevel converters; PUC inverter; CSC inverter; MPC; MPPT; grid connected PV applications; booster inverter

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1. Introduction

As world's energy demand keeps growing tremendously due to fossil fuels finite nature and their harmful emissions, the transition to clean energy won't be just a decision or choice, but also a must and a necessity for building a sustainable energy future with a robust, resilient and equitable global ecosystem. Shifting to clean energy sources means integrating Renewable Energy sources such as solar and wind. Using Renewable Energy sources over all carbon emission sources contributes to climate changes mitigation, greenhouse emissions reduction, and finite natural resources conservation. This transition will absolutely resolve one of the most pressing issues facing the world.

Solar energy has become the fastest-growing renewable energy source globally due to its low maintenance requirements and lack of noise emissions, among other benefits. Worldwide, the annual demand for photovoltaic (PV) systems, solar energy system, is on the rise, with approximately 522 GW of new PV installations anticipated between 2019 and 2022 [1]. However, connecting PV systems to power grids presents several challenges, including choosing the appropriate grid node voltage level based on the capacity of the PV system, ensuring power quality management, and developing effective control systems [1,2].

Due to the urgent need for energy alternative transition and since inverters are tasked with converting the DC power generated by Renewable Energy systems into AC power that can be fed into the grid, researchers are focusing more on efficient power electronics inverters for energy conversion for high power applications. Therefore, improvement of power electronics inverters will facilitate renewable energy sources to integrate into the grid, and consequently helping in supplying high power loads to wide range of consumers.

Inverters can be categorized into two main families: 2-Level Inverters and Multilevel Inverters (MLIs). 2-Level inverters are characterized by their high switching frequency and low voltage amplitude accompanied with high harmonic contents which calls for big inductance for filtering it out [3]. These characteristics limit the use of 2-Level Inverters in medium-voltage-high-power applications [4]. To overcome these obstacles, MLIs are introduced to be integrated in power conversion stage. MLIs were first introduced by Baker and Lawrence in 1975 [5]. MLI minimizes voltage distortion leading to better power quality, decreases harmonic distortion allowing for a smaller filter size, decreases stress on switching devices, lowers detrimental effects, decreases switching losses, lowers electromagnetic interference and supports higher power ratings (increases voltage amplitude) [6].

MLIs are made up of advanced power semiconductors and DC voltage source(s) which generate an alternating output of distinct voltage levels from lower DC voltage levels. The output step voltage level is produced by the inverter between its output terminal and neutral reference node. The number of these output step voltage levels defines the inverter's level number; for example if the inverter generates three distinct voltage levels then it is called three-level inverter and if it generates five distinct voltage levels then it is called five-level inverter. Thus, at least three voltage levels should be generated by the inverter, in each phase, in order to be classified as MLI. Although, higher number of voltage levels improves the output waveform's voltage and current quality (resulting in more sinusoidal, smoother waveforms with reduced total harmonic distortion), it also results in more complex and expensive system. Consequently, indicating the suitable number of an inverter's voltage levels relies on cost, size, and its intended use [7]. As a result, MLIs continue to outperform conventional 2-level inverters by overcoming their shortcomings and drawbacks [8–10].

MLIs represent an appealing advancement for medium to high voltage and high-power applications, including high-power AC motor drives, active power filters, aerospace applications [11] ventilation applications [12], hybrid electric vehicles [13], and the integration of renewable energy sources into the grid [14].

Contemporary research on voltage source MLIs mainly categorizes them into three conventional types. Cascaded H-Bridge (CHB) was introduced in 1975 by grouping single-phase inverters in series [5,15], followed by the Neutral Point Diode Clamped (NPC) inverter which was introduced in 1981 [16], and the Flying Capacitor Inverter (FCI) [8]. With advancements in power electronics, several MLIs have been introduced and developed, including the Active Front-End Rectifier (AFE Rectifier), Matrix Converters, Packed U-Cell (PUC) [17,18], and Packed E-Cell (PEC) [19].

The CHB inverter, which requires multiple separate DC sources, is utilized in high-power applications, while the NPC inverter, using a single separate DC source, like the FCI, is suitable for medium and high-power applications. CHB and NPC are primarily utilized in motor drives. The FCI is particularly proposed for medium voltage applications. AFE rectifiers are employed in AC-DC power conversion, offering advantages over diode rectifiers in terms of sinusoidal input currents, bidirectional power flow capability, and controllable power factor. The Matrix Converter serves as an alternative to back-to-back configurations and is preferred in applications where size and volume are critical considerations.

In comparison to the aforementioned MLI topologies, PUC produces more voltage levels with superior power quality while utilizing fewer DC sources, utilizing just a single DC source, and fewer passive and active components [20–27]. Thus, PUC inverter can generate up to seven output voltage levels using six switches, one DC source, and one DC capacitor. However, NPC and FCI require a significant number of clamping diodes and flying capacitors respectively to achieve a higher number of output voltage levels [28,29]. Besides, in NPC inverter, other factors, like load power factor, can cause imbalances in the DC capacitor voltages [30]. Modified CHB topologies have been also proposed to enhance output voltage quality and decrease circuit components' number [31]. However, these modifications necessitate different values for the DC sources. Consequently, PUC inverter is regarded as the most reliable and dependable among the above-mentioned MLI that is more compact and cost-effective.

Recently, a Cross Switches Cell (CSC) inverter, which is a modified version of PUC topology, was introduced in [32]. By incorporating two crossover bidirectional switches into the PUC design, it can generate 9 voltage levels. Thus, its maximum output voltage level exceeds the DC source voltage letting CSC of having boost capability. As a result, the CSC inverter produces 9 voltage levels while requiring fewer DC sources, capacitors, and switches compared to the CHB (symmetric/asymmetric), FCI, NPC, PEC, and PUC MLIs [32–35]. This reduction in components and sources lowers manufacturing costs, making the CSC ideal for applications where minimizing the number of DC sources and components is essential.

Given that MLIs are composed of multiple internal power semiconductors, various well-established modulation techniques have been developed and proposed for their control over the past few decades. The most commonly suggested and used techniques include Pulse Width Modulation (PWM) [36,37] and Space Vector Modulation (SVM) [38]. Other modulation techniques such as Space Vector Control (SVC) and Selective Harmonic Elimination (SHE) have been also reported [39–41]. Moreover, several control methods have been presented in literature to control MLIs' switches such as Hysteresis Control, Model Predictive Control (MPC),and Artificial Intelligence-Based Methods [42–44].

The MPC method has been successfully utilized across various MLI topologies discussed in the literature, including 3-level NPC, 4-level FCI, CHB MLIs, 7-level PUC, and matrix converters [45,46]. The FCS-MPC directly implements control actions on the inverter without needing a modulation process [45]. Additionally, FCS-MPC is a multi-objective control strategy that optimizes a specified cost function based on the application's requirements.

This paper presents a comparison between a single phase 7L-PUC grid-tied inverter and single phase 9L-CSC grid tied inverter, in which the contribution of this paper is demonstrated by replacing both the input battery source and DC link capacitor with solar panels (PV panels) in the two proposed inverters to increase the power density of the system, as illustrated in Figures 1a and 2a. Both proposed inverters undergo the same control topology in which both inverters utilize a Finite Set Model Predictive Controller (MPC), incorporating a Maximum Power Point Tracking (MPPT) technique to ensure maximum power output from the PV panels. The control topology proposed for both

inverters is characterized by reduced complexity. The paper discusses the PUC converter in Section 2, followed by an elaboration on CSC inverter in Section 3. Section 4 provides an introduction to the MPC configuration for the grid-connected 7L-PUC inverter and 9L-CSC inverter. Then, Section 5 presents simulation results for PUC inverter while Section 6 presents simulation results for CSC inverter using MATLAB/Simulink for both inverters. Finally, Section 7 concludes the work through comparing both proposed topologies.

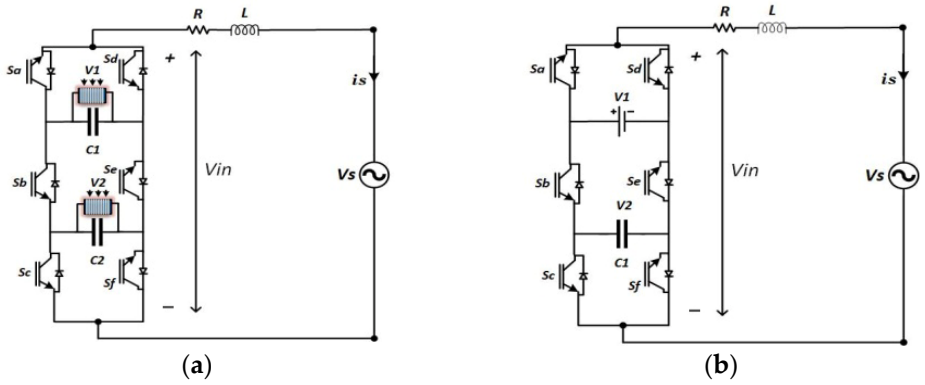

Figure 1. (**a**) Proposed and (**b**) conventional PUC converter.

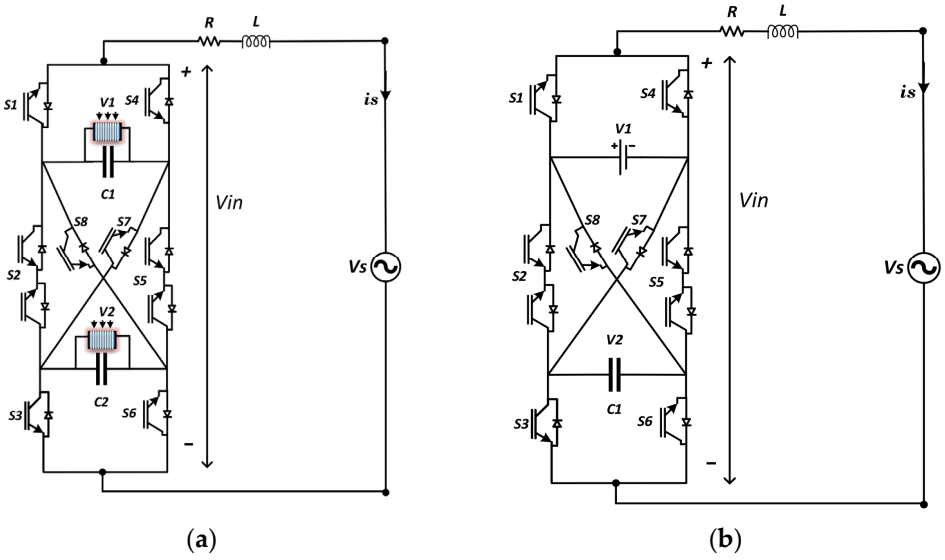

Figure 2. (**a**) Proposed and (**b**) conventional CSC converter.

2. Packed U-Cell Converter Topology

The PUC converter was developed and introduced by Ounejjar and Al-Haddad [17,18]. It is an adapted version of the CHB, notable for having fewer switches while achieving a high number of output voltage levels. The PUC converter features six active switches and two DC links, as depicted in Figure 1b. Operating in inverter mode, it utilizes an isolated DC source as the primary DC link and a capacitor as a secondary, auxiliary DC link. The voltage of the capacitor is regulated based on the DC source voltage. The switches are considered ideal, operating in only two states: ON or OFF. They function in complementary pairs, with S_a paired with S_d, S_b with S_e, and S_c with S_f. As illustrated in Figure 1b, each complementary pair connects to a DC link, forming a U-cell configuration. The PUC setup generates eight switching states, as detailed in Table 1, with each state creating a specific current path through the circuit, involving the DC sources and the load. The number of output voltage levels varies based on the voltage ratio between the DC links.

Table 1. PUC Inverter all Possible Switching States.

States	S_a	S_b	S_c	V_{in} (Output Voltage)
1	1	0	0	V_1
2	1	0	1	$V_1 - V_2$
3	1	1	0	V_2
4	1	1	1	0
5	0	0	0	0
6	0	0	1	$-V_2$
7	0	1	0	$V_2 - V_1$
8	0	1	1	$-V_1$

PUC inverter achieves its maximum output of seven voltage levels when $V_1 = 3V_2$, as illustrated in Table 2. When $V_1 = 2V_2$, PUC inverter generates five voltage levels, as shown in Table 3. Additionally, when $V_1 = V_2$, PUC inverter generates three voltage levels, as indicated in Table 4.

Table 2. Voltage Levels Values Produced by 7-Level PUC Inverter. ($V_2 = E$ & $V_1 = 3V_2 = 3E$).

States	S_a	S_b	S_c	V_{in} (Output Voltage)	V_{in} (Output Voltage Value)
1	1	0	0	V_1	+3E
2	1	0	1	$V_1 - V_2$	$3E - E = +2E$
3	1	1	0	V_2	+E
4	1	1	1	0	0
5	0	0	0	0	0
6	0	0	1	$-V_2$	−E
7	0	1	0	$V_2 - V_1$	$E - 3E = -2E$
8	0	1	1	$-V_1$	−3E

Table 3. Voltage Levels Values Produced by 5-Level PUC Inverter. ($V_2 = E$ & $V_1 = 2V_2 = 2E$).

States	S_a	S_b	S_c	V_{in} (Output Voltage)	V_{in} (Output Voltage Value)
1	1	0	0	V_1	+2E
2	1	0	1	$V_1 - V_2$	$2E - E = +E$
3	1	1	0	V_2	+E
4	1	1	1	0	0
5	0	0	0	0	0
6	0	0	1	$-V_2$	−E
7	0	1	0	$V_2 - V_1$	$E - 2E = -E$
8	0	1	1	$-V_1$	−2E

Table 4. Voltage Levels Values Produced by 3-Level PUC Inverter. ($V_1 = V_2 = E$).

States	S_a	S_b	S_c	V_{in} (Output Voltage)	V_{in} (Output Voltage Value)
1	1	0	0	V_1	+E
2	1	0	1	$V_1 - V_2$	$E - E = 0$
3	1	1	0	V_2	+E
4	1	1	1	0	0
5	0	0	0	0	0
6	0	0	1	$-V_2$	−E
7	0	1	0	$V_2 - V_1$	$E - E = 0$
8	0	1	1	$-V_1$	−E

It is important to mention that the novelty here is to modify the PUC topology by replacing both the input battery source and DC link capacitor with PV panels as shown in Figure 1a. Therefore, the considered circuit for our study in this section is the one illustrated in Figure 1a.

3. Crossover Switches Cell Converter Topology

Single phase 9-level grid tied CSC inverter is depicted in Figure 2b. This CSC system includes one DC source and one capacitor, with their voltage levels designated as V_1 and V_2, respectively. The system comprises eight switches, labeled S_1 to S_8, among which S_2 and S_5 only function as bidirectional switches. The switches S_1 and S_4, as well as S_3 and S_6, are operated in a complementary manner, while one switch only from the group (S_2, S_5, S_7, S_8) is activated ON at any given time. The CSC setup generates sixteen switching states, as detailed in Table 5.

Table 5. Voltage Levels Values Produced by 9-Level CSC Inverter (V2 = E & V1 = 3V2 = 3E).

States	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	V_{in} (Output Voltage)	V_{in} (Output Voltage Value)	Capacitor Charging State
1	1	0	0	0	0	1	1	0	$V_1 + V_2$	3E + E = 4E	Charged
2	1	0	0	0	1	1	0	0	V_1	3E	By passed
3	1	0	1	0	0	0	1	0	V_1	3E	By passed
4	1	0	1	0	1	0	0	0	$V_1 - V_2$	3E − E = 2E	Discharged
5	0	0	0	1	0	1	1	0	V_2	E	Charged
6	1	1	0	0	0	1	0	0	V_2	E	Charged
7	0	0	1	1	0	0	1	0	0	0	By passed
8	1	1	1	0	0	0	0	0	0	0	By passed
9	0	0	0	1	1	1	0	0	0	0	By passed
10	1	0	0	0	0	1	0	1	0	0	By passed
11	0	0	1	1	1	0	0	0	$-V_2$	−E	Discharged
12	1	0	1	0	0	0	0	1	$-V_2$	−E	Discharged
13	0	1	0	1	0	1	0	0	$-V_1 + V_2$	−3E + E = −2E	Charged
14	0	0	0	1	0	1	0	1	$-V_1$	−3E	By passed
15	0	1	1	1	0	0	0	0	$-V_1$	−3E	By passed
16	0	0	1	1	0	0	0	1	$-V_1 - V_2$	−3E − E = −4E	Discharged

Adding two crossover switches (S_7 and S_8) between DC link and capacitor to the PUC inverter results in two extra output voltage levels of $\pm(V_1 + V_2)$. This adjustment also enhances the stability of the DC voltage by creating additional paths for the charging and discharging of the capacitor [32,47]. Thus, to achieve a 9-level output voltage, the capacitor voltage V_2 must be regulated to $V_{1/3}$.

It is important to mention that the novelty here is also to modify the CSC topology by replacing both the input battery source and DC link capacitor with PV panels as shown in Figure 2a. Thus, PV solar panels are connected in parallel with a capacitor replacing the DC battery input and also PV solar panels are connected in parallel with a capacitor in the second DC link as well. Therefore, the considered circuit for our study in this section is the one illustrated in Figure 2a.

4. Model Predictive Control Design

This paper employs MPC to manage PUC and CSC inverters, utilizing its ability to forecast the future behavior of variables [48,49]. MPC controller is distinguished from traditional controllers due to its flexibility in managing and controlling various variables with constraints. This approach eliminates the need for a cascaded control structure for controlling system's parameters. Thus, MPC features two loops in its control architecture:

a fast inner loop and a slower outer loop. In each switching state, the MPC assesses the controlled variable $x(k)$ and predicts its future value $x(k+1)$ using the predictive control. It then evaluates a cost function, in which the minimum cost function is selected by MPC. The switching state that corresponds to the selected cost function is regarded as the optimal switching state, which is consequently applied to the inverter through switching pulses.

4.1. Model Predictive Control Design for PUC

In [50,51], both load current and capacitor voltage V_2 are controlled by the MPC. However, in this study, we focus on controlling load current, the output voltage of the PV in the primary DC link and the output voltage of the PV in the secondary auxiliary DC link. To simplify calculations, we introduce two new variables, S_1 and S_2, which are derived from S_a, S_b, and S_c, as indicated in Equations (1) and (2).

$$S_1 = S_a - S_b \tag{1}$$

$$S_2 = S_b - S_c \tag{2}$$

By inserting (1) and (2) into the switching states of Table 1, we derive the simplified switching states presented in Table 6.

Table 6. Simplified Switching States.

States	S_1	S_2	V_{in} (Output Voltage)
1	1	0	V_1
2	1	−1	$V_1 - V_2$
3	0	1	V_2
4	0	0	0
5	0	0	0
6	0	−1	$-V_2$
7	−1	1	$V_2 - V_1$
8	−1	0	$-V_1$

PUC inverter produces voltage vector V_{in} that is generated using (3).

$$V_{in} = S_1 V_1 + S_2 V_2 \tag{3}$$

Load current dynamics is represented in (4) using vector differential equation:

$$V_{in} = v_s + R i_s + L\frac{di_s}{dt} \tag{4}$$

Using Euler Forward Approximation, Load current can be expressed as shown in Equation (5).

$$\frac{di_s}{dt} = \frac{i_s(k+1) - i_s(k)}{T_s} \tag{5}$$

Replace (5) in (4) to derive (6).

$$i_s(k+1) = \left(1 - \frac{RT_s}{L}\right) i_s(k) + \frac{T_s}{L}(V_{in}(k) - v_s) \tag{6}$$

Once the predicted load current is obtained, the cost function g is formulated as shown in Equation (7).

$$g(k) = L(i_s(k+1) - i_s{}^*)^2 + D_1(V_1 - V_{PV1})^2 + D_2(V_2 - V_{PV2})^2 \tag{7}$$

As previously mentioned, the cost function g is calculated for each switching state, and the MPC selects the minimum cost function. Consequently, S_1 and S_2 are determined based on this minimum cost function, which then identifies the corresponding switching state number using Table 6. The switching states for S_a, S_b, and S_c are then selected from Table 1 to be implemented on the PUC inverter switches.

At instant *k*, the load current or grid current is measured, and based on these readings, $i_s(k+1)$ is generated and predicted using Equation (6). The cost function is then calculated at instant *k* using Equation (7). i_s^* in the cost function represents the grid reference current where V_1 represents the V_{mppt} of the PV in the primary DC link, V_{PV1} represents output voltage of the PV in the primary DC link, V_2 represents V_{mppt} of the PV in the secondary auxiliary DC link, and V_{PV2} represents the output voltage of the PV in the secondary auxiliary DC link.

Grid reference current depends on grid voltage, for which a PLL block is utilized to extract the phase angle, ensuring that the grid reference current is in phase with the grid voltage. To adjust the power factor between the grid voltage and the grid reference current, a phase shift is applied to the angle generated by the PLL block. If the phase shift is set to zero, the grid voltage and grid reference current are in phase, achieving unity power factor operation. Otherwise, reactive power will be exchanged with the grid.

Regarding the amplitude of the grid reference current, if PUC operates in its standard configuration, as shown in Figure 1b, the amplitude is chosen arbitrarily to match the required power to be injected into the grid. In this study, however, PUC topology is modified as depicted in Figure 1a, with PV solar panels connected in parallel with a capacitor replacing the DC battery input. Additionally, solar panels are connected in parallel with a capacitor in the second DC link. This modification necessitates deriving the amplitude of the grid reference current from the PV solar power or using a PI controller to minimize the voltage differences between the reference and actual DC link [52]. In our proposed control strategy, the grid reference current amplitude is generated from the PV solar power, calculated by dividing the PV solar power by V_s.

It is essential to highlight that the cost function in Equation (7) should ideally include weighting factors if there are more than one variable parameter to control. Weighting factors are typically used to mitigate coupling effects between multiple controlled variables in the cost function. Accordingly, weighting factors in this study are chosen as follows; L = 10, D_1 = 5 and D_2 = 5.

Figure 3 illustrates the flow chart of the proposed MPC topology applied to the single phase 7-level PUC inverter. As noted, MPC consists of two loops: an inner loop and an outer loop. The outer loop measures the grid current at instant *k*, $i_s(k)$, at each sampling time. Meanwhile, for each possible state, the inner loop calculates the predictive grid current value $i_s(k+1)$ and generates the corresponding cost function to store the optimal values. The inner loop is executed eight times to account for the eight possible switching states in the PUC. After completing the executions for eight possible states, the minimum cost function value is selected, and its related switching state is applied to the PUC's six switches.

To incorporate PV solar applications in our work, an MPPT algorithm is necessary to enhance PV efficiency, achieve accurate and rapid tracking performance, and reduce oscillations around the MPP. MPPT methods can be categorized as on-line or off-line. The on-line method regulates the PV voltage at the MPP voltage, while the off-line method is based on models techniques. Perturbation and Observation (P&O) is a common on-line method and is widely used among MPPT techniques due to its simplicity. P&O technique is implemented in our work, and its detailed operational method is described in [51]. The P&O technique directly manages and controls the power output, in which the need for a DC-DC boost converter will be eliminated when integrating PV solar panels with the PUC inverter.

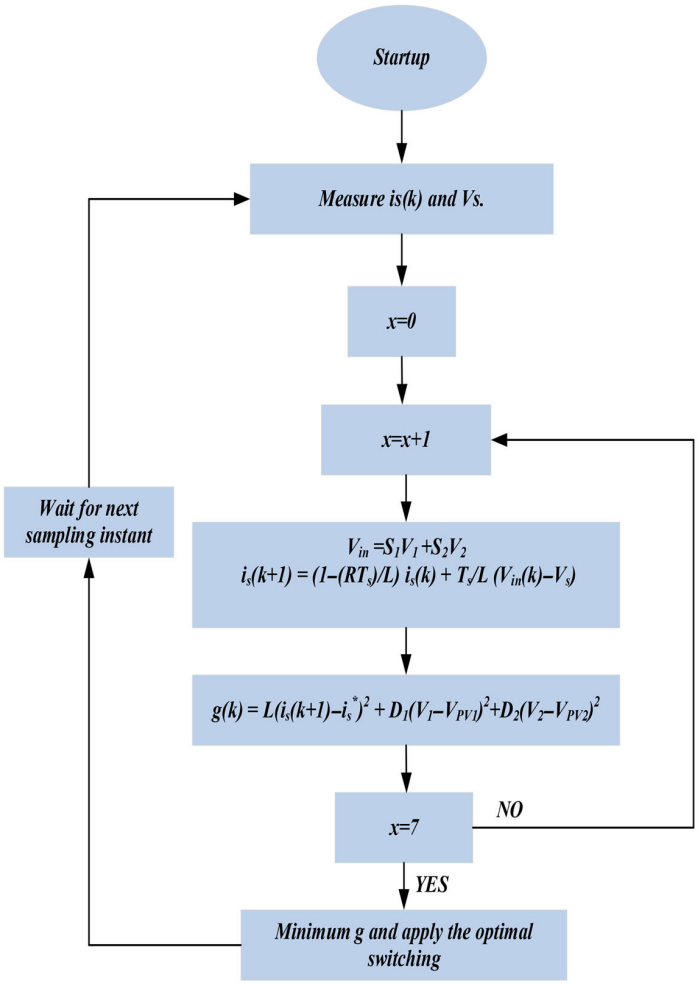

Figure 3. MPC algorithm flowchart applied on 7L-PUC inverter.

The complete system model demonstrating MPC applied on the single-phase 7L-PUC inverter is illustrated in Figure 4.

4.2. Model Predictive Control Design for CSC

By applying Kirchhoff's laws, DC source voltage $V_1(t)$, capacitor voltage $V_2(t)$, grid current $i_s(t)$, grid voltage $V_s(t)$, output voltage $V_{in}(t)$, and the eight switches S_i {I = 1… 8} can be formulated as follows:

Capacitor voltage is represented in (8).

$$\frac{dV_2}{dt} = \frac{(S_3 - S_2 - S_7)i_s}{C} \tag{8}$$

Using Euler Forward Approximation, Voltage capacitor can be expressed as shown in Equation (9).

$$\frac{dV_2}{dt} = \frac{V_2(k+1) - V_2(k)}{T_s} \tag{9}$$

Compare (8) and (9) to derive (10).

$$V_2(k+1) = V_2(k) + \frac{T_s(S_3 - S_2 - S_7)i_s(k)}{C} \tag{10}$$

CSC inverter produces voltage vector V_{in} that is generated using (11).

$$V_{in} = (S_1 - S_2 - S_8)V_1 + (S_2 - S_3 + S_7)V_2 \tag{11}$$

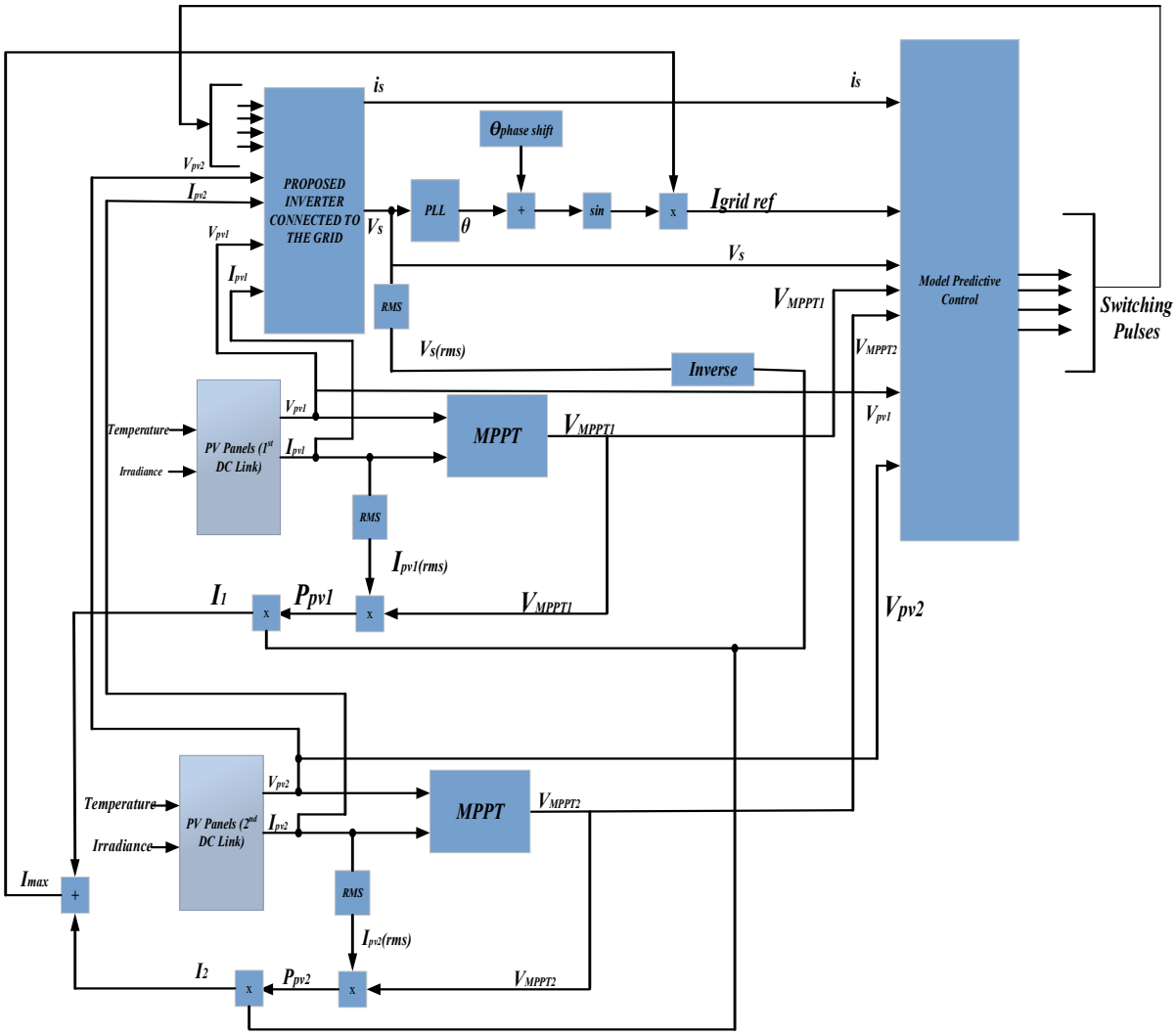

Figure 4. Schematic control model applied on the proposed inverters.

Load current dynamics is represented in (12) using vector differential equation:

$$V_{in} = v_s + Ri_s + L\frac{di_s}{dt} \tag{12}$$

Using Euler Forward Approximation, Load current can be expressed as shown in Equation (13).

$$\frac{di_s}{dt} = \frac{i_s(k+1) - i_s(k)}{T_s} \tag{13}$$

Replace (13) in (12) to derive (14).

$$i_s(k+1) = \left(1 - \frac{RT_s}{L}\right)i_s(k) + \frac{T_s}{L}(V_{in}(k) - v_s) \tag{14}$$

Once the predicted load current is obtained, the cost function g is formulated as shown in Equation (15).

$$g(k) = L(i_s(k+1) - {i_s}^*)^2 + D_1(V_1 - V_{PV1})^2 \tag{15}$$

As previously mentioned, the cost function g is calculated for each switching state and the MPC selects the minimum cost function. Consequently, S_1, S_2, S_3, S_4, S_5, S_6, S_7, and S_8 are determined based on this minimum cost function.

The same control strategy that is applied for PUC inverter is also applied for CSC inverter in which at instant k, the load current or grid current is measured, and based on these readings, $i_s(k+1)$ is generated and predicted using Equation (14). Cost function is then calculated at instant k using Equation (15). i_s^* in (15) represents the grid reference current where V_1 represents the V_{mppt} of the PV in the primary DC link, V_{PV1} represents output voltage of the PV in the primary DC link, V_2 represents V_{mppt} of the PV in the secondary auxiliary DC link, and V_{PV2} represents the output voltage of the PV in the secondary auxiliary DC link.

As for Grid Reference Current, a PLL block is utilized to extract the phase angle from the grid voltage, ensuring that the grid reference current is in phase with the grid voltage. To adjust the power factor between the grid voltage and the grid reference current, a phase shift is applied to the angle generated by the PLL block.

Regarding the amplitude of the grid reference current, it is derived from the PV solar power, calculated by dividing the PV solar power by V_s.

As for the weighting factors, they are also chosen as follows; L = 10, D_1 = 5 and D_2 = 5.

Figure 5 illustrates the flow chart of the proposed MPC topology applied to the single phase 9-level CSC inverter. As mentioned previously, MPC consists of two loops: an inner loop and an outer loop. The outer loop measures the grid current at instant k, $i_s(k)$, at each sampling time. Meanwhile, for each possible state, the inner loop calculates the predictive grid current value $i_s(k+1)$ and generates the corresponding cost function to store the optimal values. The inner loop is executed sixteen times to account for the sixteen possible switching states in the CSC. After completing the executions for sixteen possible states, the minimum cost function value is selected, and its related switching state is applied to the CSC's eight switches.

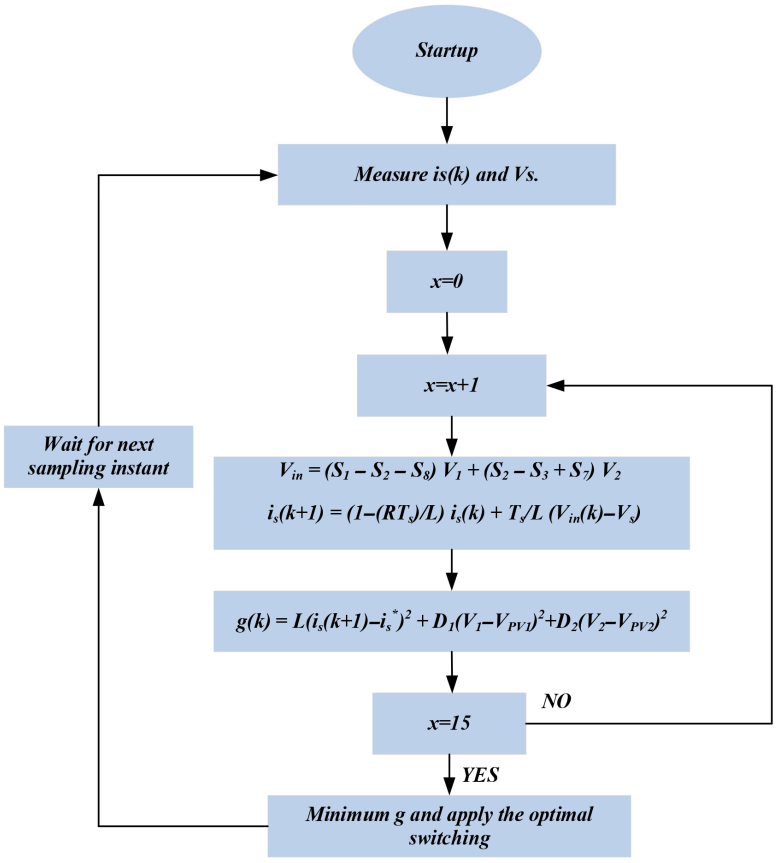

Figure 5. MPC algorithm Flowchart applied on 9L-CSC inverter.

MPPT algorithm is necessary to be applied in the control strategy due to the PV solar incorporation in our work. P&O technique is also implemented here. P&O technique directly manages and controls the power output, in which the need for a DC-DC boost converter will be eliminated when integrating PV solar panels with the PUC inverter.

The complete system model demonstrating MPC applied on the single-phase 9L-CSC inverter is illustrated in Figure 4.

5. Simulation Results and Analysis for PUC

To assess the effectiveness and reliability of our proposed approach, we conducted simulations of the entire system using MATLAB/Simulink. The sampling time was configured to Ts = 20 µs. Irradiance and temperature were set at 1000 W/m^2 and 25 °C, respectively. Table 7 displays the parameters of the system utilized in the simulations.

Table 7. System's Parameters for PUC Inverter.

Sampling Time	**20 µs**
DC bus voltage (PV panels)	300–315 V (9 panels in series)
DC link voltage (PV panels)	99–105 V (3 panels in series)
DC capacitor C	1000 µF
Line inductor L	2.5 mH
Parasitic Resistor (r)	0.1 Ω
AC grid voltage (V_{rms})	300 V
Frequency	60 Hz

Figures 6–8 display the results during steady-state operation. Figure 6 shows the inverter's 7-level output voltage (V_{in}). Figure 7 confirms that the inverter's output current (i_s) and grid voltage (V_s) remain in phase during steady-state operation. Also, it illustrates that the current (i_s) consistently tracks the grid reference current (i_s^*). Additionally, a harmonic distortion level (THD) of about 2.8% has been achieved, as show in Figure 8, demonstrating that the injected current aligns well with grid connectivity standards and requirements, which specify a limit of less than 5%.

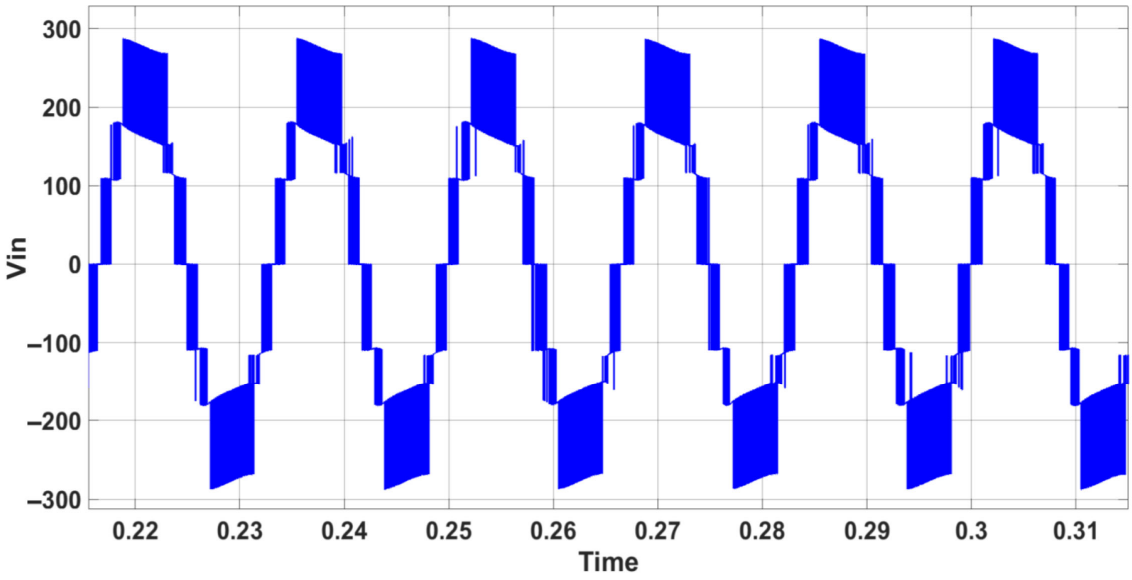

Figure 6. Inverter 7-level output voltage in steady state operation—PUC inverter.

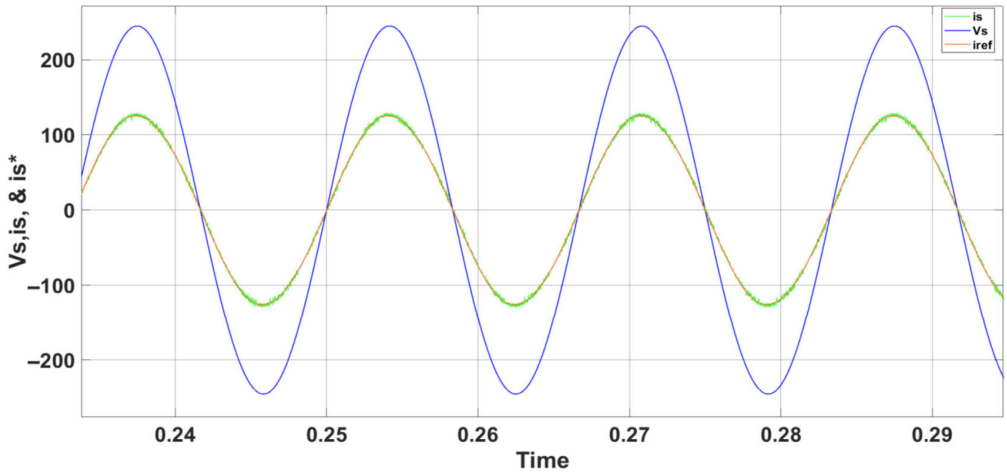

Figure 7. AC waveforms i_s (A) (multiplied by 10), i_s* (A) (multiplied by 10), and V_s (V) in steady state operation—PUC inverter.

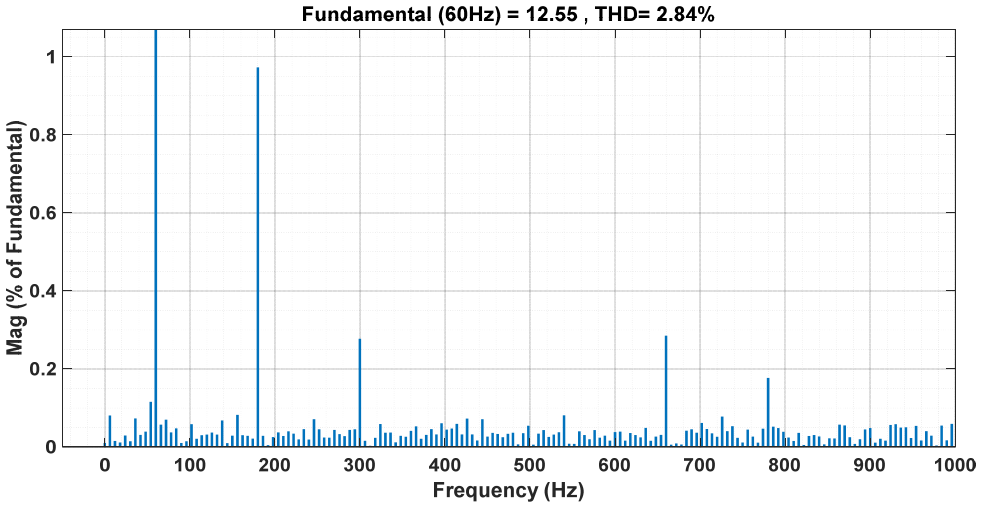

Figure 8. AC Grid current harmonic spectrum in steady state operation—PUC inverter.

Figures 9 and 10 present the voltage and current waveforms during changes in grid voltage. Grid voltage was modified from 300 V to 270 V (phase-to-phase V_{rms}) to 270 V (phase-to-phase V_{rms}), reflecting a 10% change in grid voltage. It is clear from Figure 9 that these changes do not affect the inverter's voltage. Figure 10 indicates that the grid current continues to meet the desired values, even though the grid voltage experiences a slight drop. It also demonstrates that the current (i_s) continues to track the grid reference current (i_s^*) despite disturbances caused by variations in grid voltage. Furthermore, a harmonic distortion level of roughly 2.6% has been obtained, confirming that the injected current adheres to the grid connectivity standards and requirements.

To further evaluate the system's robustness, an additional test was conducted aimed at exchanging reactive power with the grid. This resulted in a sudden shift in the phase angle between the grid voltage and current from 0° to 30°, altering the power factor (PF) from 1 to 0.85. Figures 11 and 12 illustrate the simulation results of this change. As shown in Figure 11, the inverter's voltage remains unaffected. Figure 12 demonstrates that the grid voltage and current are initially in phase but later exhibit a phase shift of $\pi/6$ when the delay is adjusted, indicating the generation of reactive power. It also reveals that the current (i_s) continues to track the grid reference current (i_s^*) during the reactive power variation disturbance. It has also been confirmed that the injected current satisfies the grid connectivity norms and regulations, with a THD level of around 2.6%.

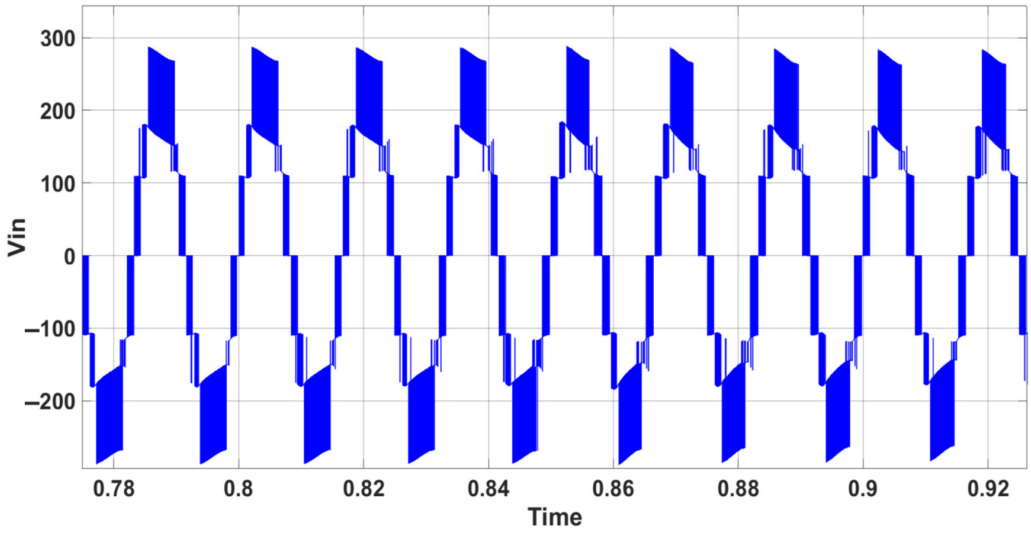

Figure 9. Inverter 7-level output voltage during 10% grid voltage variation—PUC inverter.

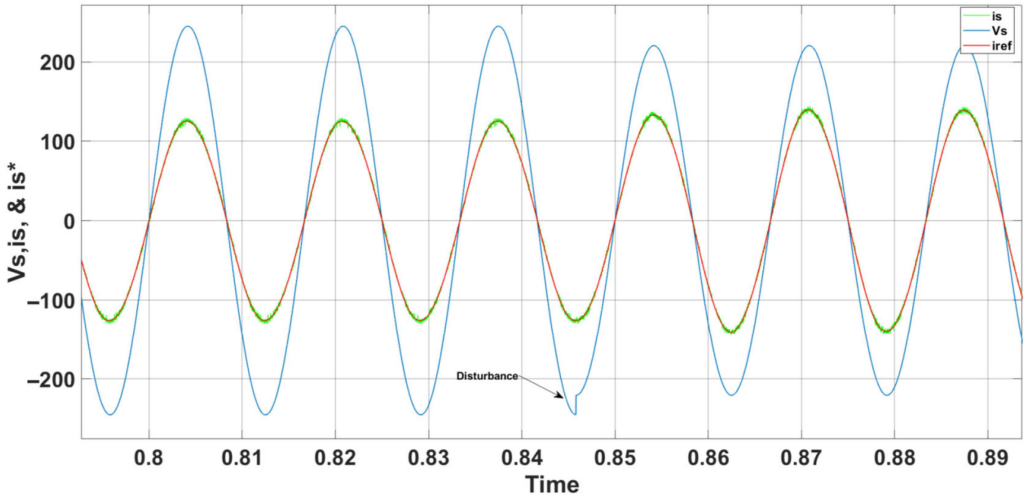

Figure 10. AC waveforms i_s (A) (multiplied by 10), i_s* (A) (multiplied by 10), and V_s (V) during 10% grid voltage variation—PUC inverter.

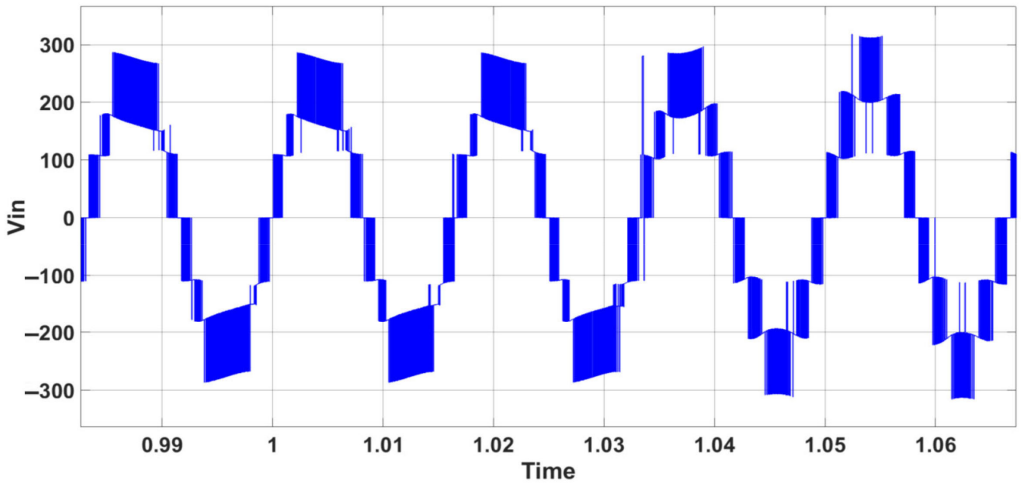

Figure 11. Inverter 7-level output voltage during reactive power variation—PUC inverter.

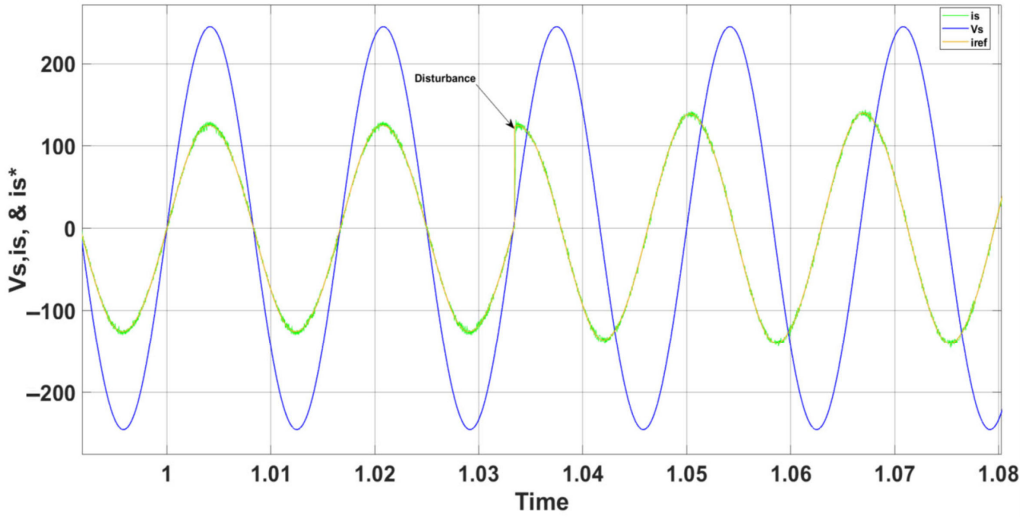

Figure 12. AC waveforms i_s (A) (multiplied by 10), i_s* (A) (multiplied by 10), and V_s (V) during reactive power variation—PUC inverter.

A test on irradiation variation was also conducted on the proposed system. This involved a sudden change in irradiation levels, ranging from 500 W/m^2 to 1000 W/m^2. Figures 13–17 illustrate the simulation results of this operation. As shown in Figure 13, the inverter's voltage remains unaffected during the irradiation variation. Figure 14 indicates that while the grid current values fluctuate slightly, the grid voltage remains constant. It also demonstrates that the current (i_s) continues to track the grid reference current (i_s^*) during the disturbance caused by the irradiation variation. Figure 15 confirms the increase in power output from the PV solar panels as irradiation levels rise. Figure 16 demonstrates the well tracking voltages of V_{DC1} and $V_{mppt(DC1)}$ during irradiation variation. Whereas, Figure 17 illustrates the well balanced and tracked voltages of V_{DC2} and $V_{mppt(DC2)}$ Moreover, THD level varies from 5.3% to 3.4%.

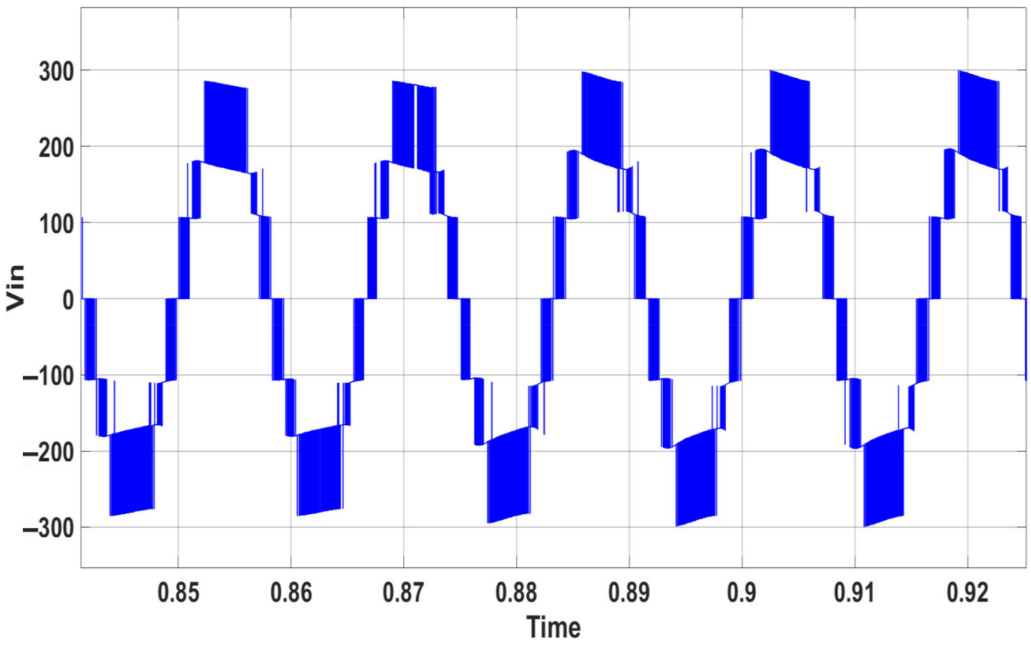

Figure 13. Inverter 7-level output voltage during irradiation variation—PUC inverter.

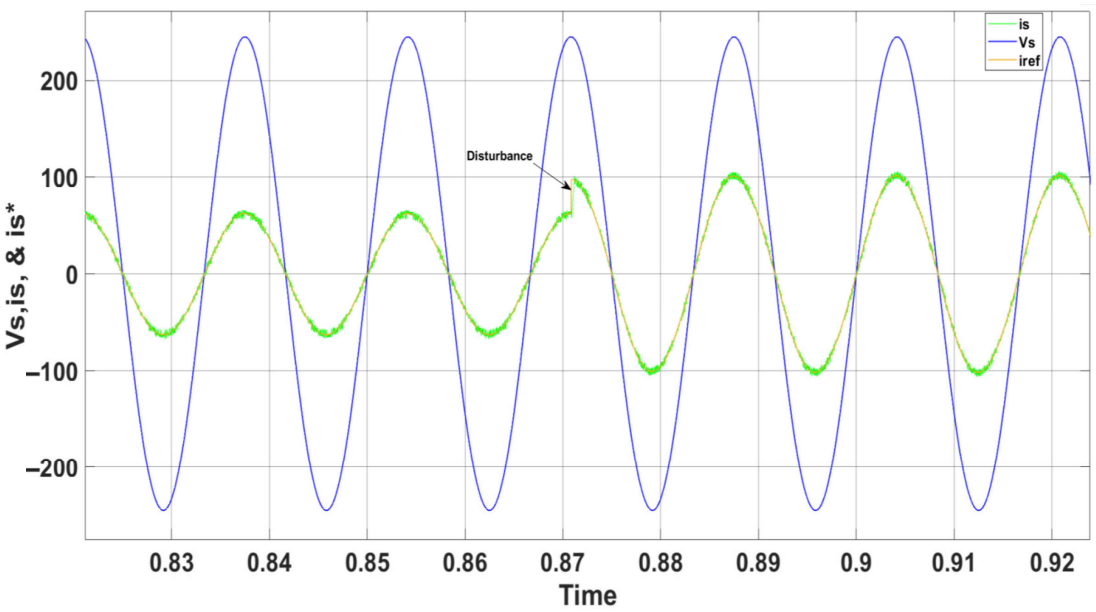

Figure 14. AC waveforms i_s (A) (multiplied by 10), i_s* (A) (multiplied by 10), and V_s (V) during irradiation variation—PUC inverter.

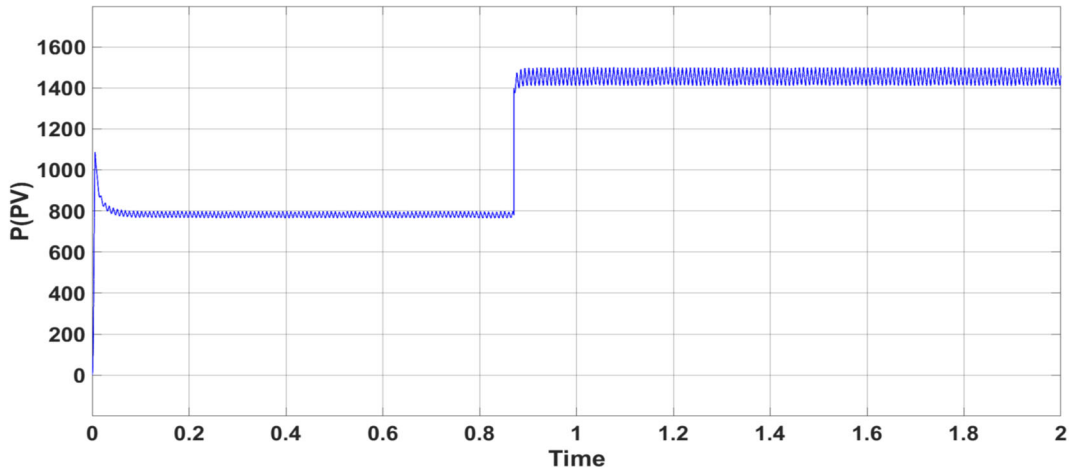

Figure 15. PV power during irradiation variation—PUC inverter.

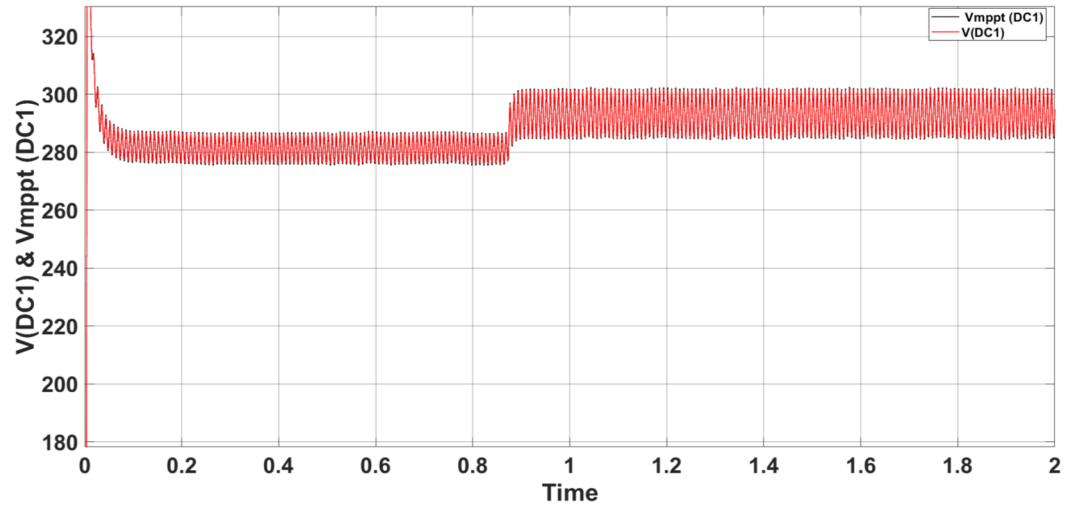

Figure 16. V_{DC1} and $V_{mppt(DC1)}$ during irradiation variation—PUC inverter.

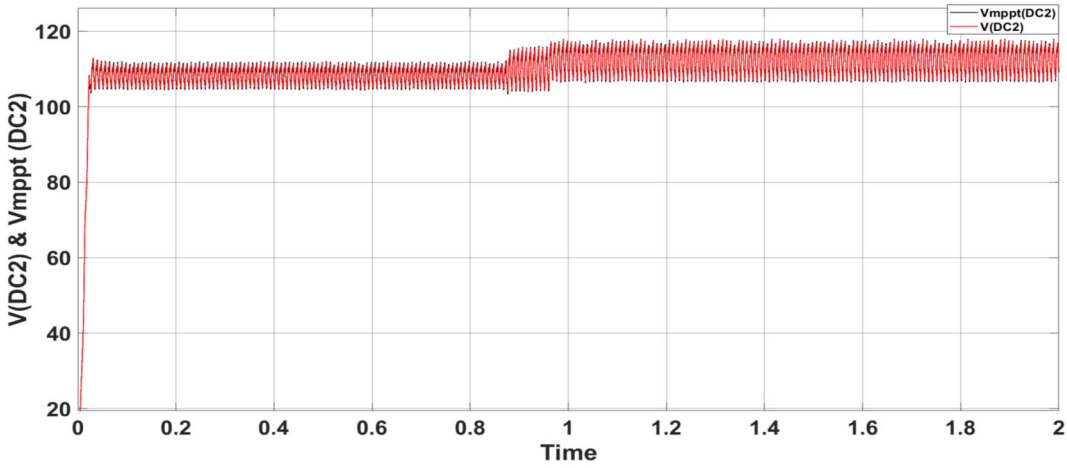

Figure 17. V_{DC2} and $V_{mppt(DC2)}$ during irradiation variation—PUC inverter.

6. Simulation Results and Analysis for CSC

To evaluate the effectiveness and reliability of our proposed method, we did for the CSC topology the same procedure as we did for PUC topology, thus we performed simulations of the entire system using MATLAB/Simulink, with a sampling time set to Ts = 20 µs. Irradiance and temperature were set at 1000 W/m^2 and 25 °C, respectively. The parameters used in the simulations are shown in Table 8.

Table 8. System's Parameters for CSC Inverter.

Sampling Time	20 µs
DC bus voltage (PV panels)	200–210 V (6 panels in series)
DC link voltage (PV panels)	66–70 V (2 panels in series)
DC capacitor C	1000 µF
Line inductor L	2.5 mH
Parasitic Resistor (r)	0.1 Ω
AC grid voltage (V_{rms})	300 V
Frequency	60 Hz

Figures 18–20 present the results observed during steady-state operation of the CSC inverter. Figure 18 illustrates the inverter's 9-level output voltage (V_{in}). Figure 19 confirms that the inverter's output current (i_s) and grid voltage (V_s) remain in phase during steady-state conditions. It also shows that the current (i_s) consistently follows the grid reference current (i_s^*). It is important to mention that a harmonic distortion level of about 3.12% has been achieved, as shown in Figure 20, indicating that the injected current satisfies the grid connectivity criteria and standards, which call for a threshold of less than 5%.

Figures 21 and 22 display the voltage and current waveforms during variations in grid voltage. The grid voltage was adjusted from 300 V (phase-to-phase V_{rms}) to 270 V (phase-to-phase V_{rms}), representing a 10% change. As seen in Figure 21, these adjustments do not impact the inverter's 9-level output voltage. Figure 22 shows that the grid current continues to meet the target values, even though the grid voltage experiences a slight decrease. It also indicates that the current (i_s) remains aligned with the grid reference current (i_s^*) despite the disturbances caused by changes in grid voltage. Furthermore, THD level of approximately 2.7% has been reached.

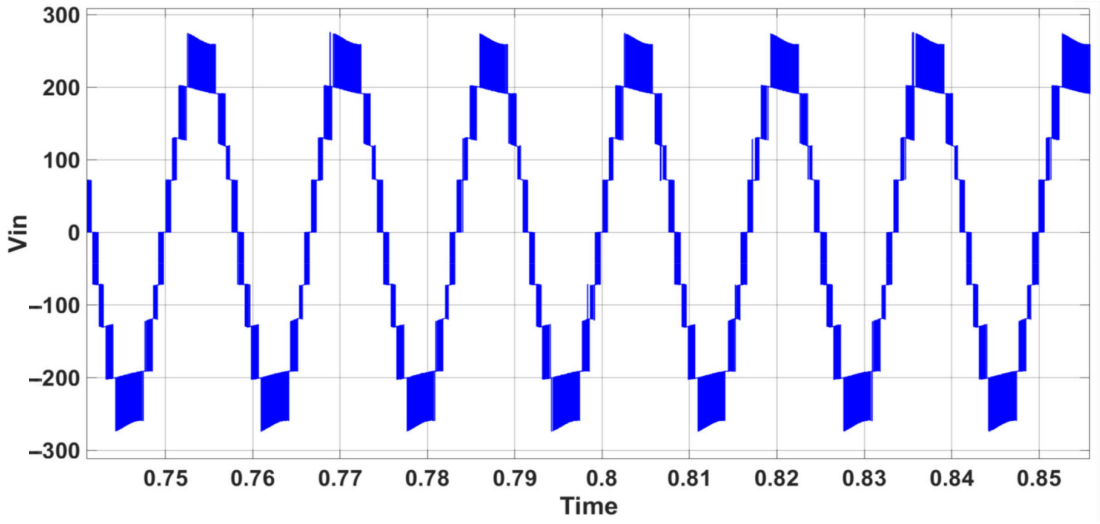

Figure 18. Inverter 7-level output voltage in steady state operation—CSC inverter.

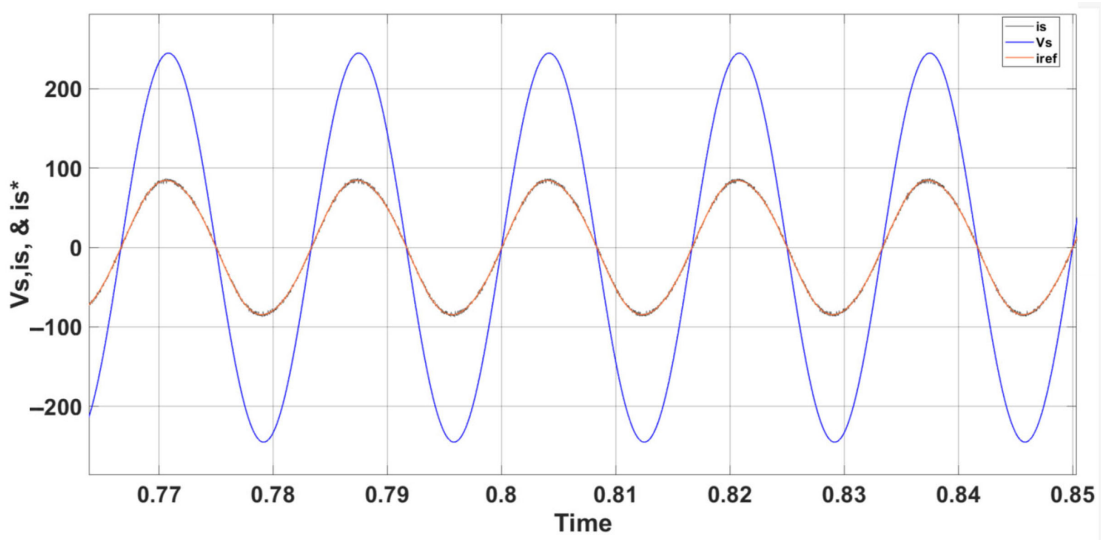

Figure 19. AC waveforms i_s (A) (multiplied by 10), i_s* (A) (multiplied by 10), and V_s (V) in steady state operation—CSC inverter.

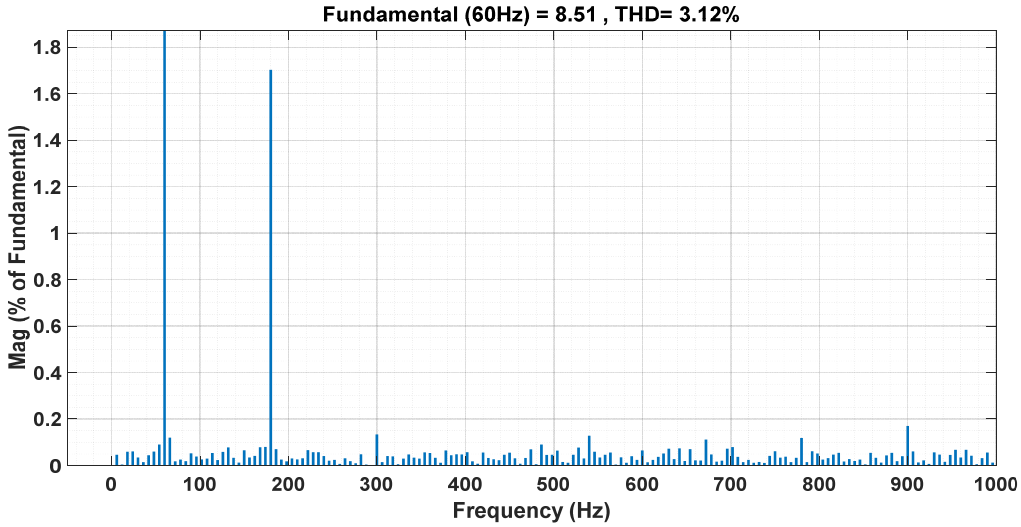

Figure 20. Grid current harmonic spectrum in steady state operation—CSC inverter.

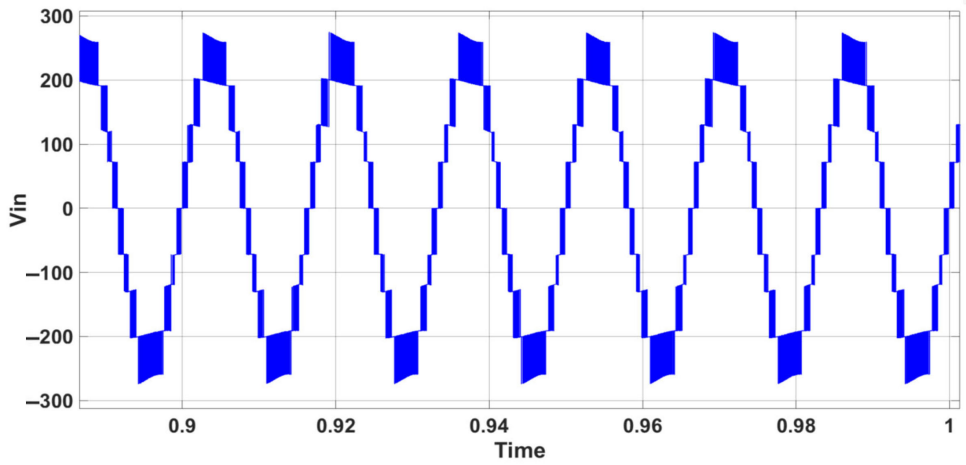

Figure 21. Inverter 7-level output voltage during 10% grid voltage variation—CSC inverter.

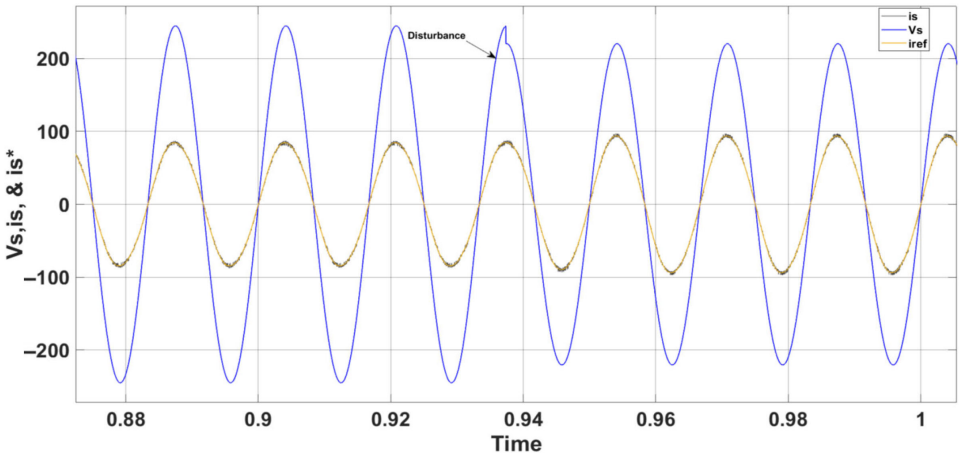

Figure 22. AC waveforms i_s (A) (multiplied by 10), i_s* (A) (multiplied by 10), and V_s (V) during 10% grid voltage variation—CSC inverter.

To further assess the system's robustness, an additional test was performed to facilitate the exchange of reactive power with the grid. This led to a sudden change in the phase angle between the grid voltage and current from 0° to 30°, which modified the power factor (PF) from 1 to 0.85. Figures 23 and 24 depict the simulation results of this adjustment. As indicated in Figure 23, the inverter's voltage remains stable. Figure 24 shows that while the grid voltage and current start off in phase, they later display a phase shift of $\pi/6$ when the delay is modified, signifying the generation of reactive power. It also demonstrates that the current (i_s) continues to follow the grid reference current (i_s^*) during the disturbance caused by the variation in reactive power. Additionally, a THD level of about 2.94% has been attained.

A test was also performed on the proposed system to assess irradiation variation, which involved a sudden change in irradiation levels from 500 W/m^2 to 1000 W/m^2. Figures 25–29 present the simulation results of this experiment. As depicted in Figure 25, the inverter's voltage remains unchanged during the irradiation variation. Figure 26 shows that while the grid current values experience slight fluctuations, the grid voltage stays constant. It also illustrates that the current (i_s) continues to follow the grid reference current (i_s^*) despite the disturbances caused by the changes in irradiation. Figure 27 assures an increase in power output from the PV solar panels corresponding to the rise in irradiation levels. Figure 28 demonstrates the well tracking voltages of V_{DC1} and $V_{mppt(DC1)}$ during irradiation variation. Whereas, Figure 29 illustrates the well balanced and tracked voltages of V_{DC2} and $V_{mppt(DC2)}$ Moreover, THD level varies from 5.2% to 3.7%.

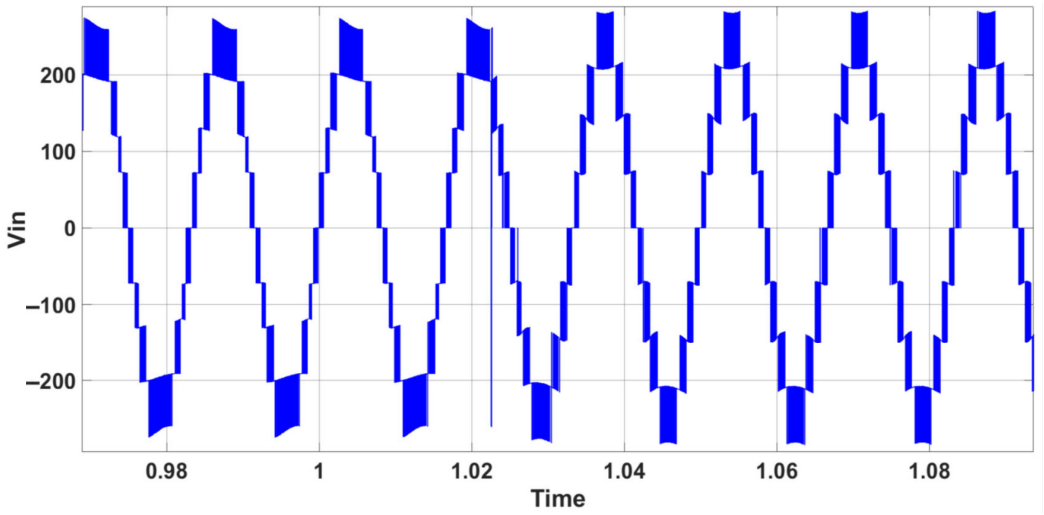

Figure 23. Inverter 7-level output voltage during reactive power variation—CSC inverter.

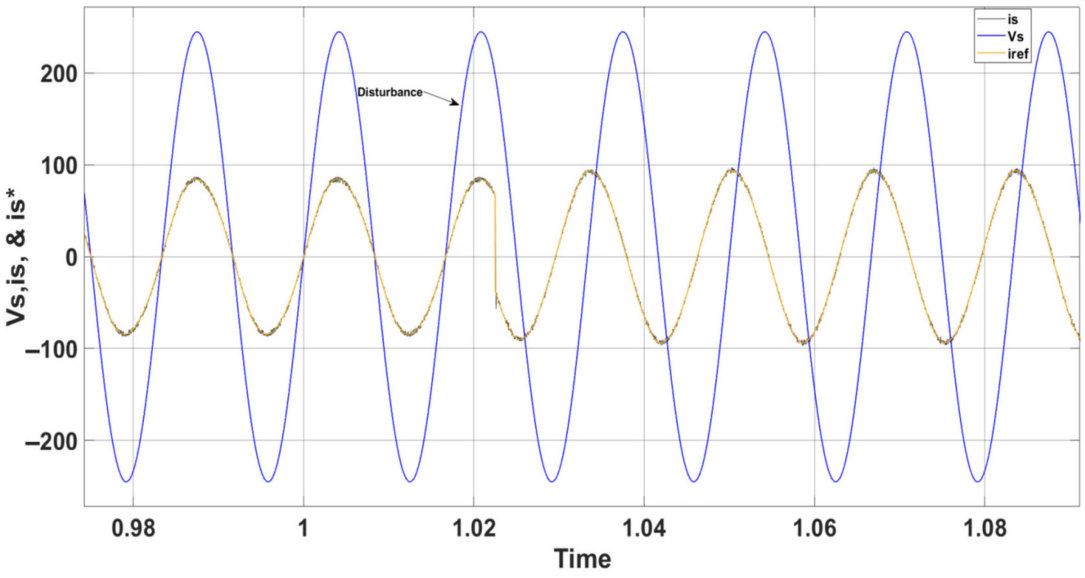

Figure 24. AC waveforms i_s (A) (multiplied by 10), i_s* (A) (multiplied by 10), and V_s (V) during reactive power variation—CSC inverter.

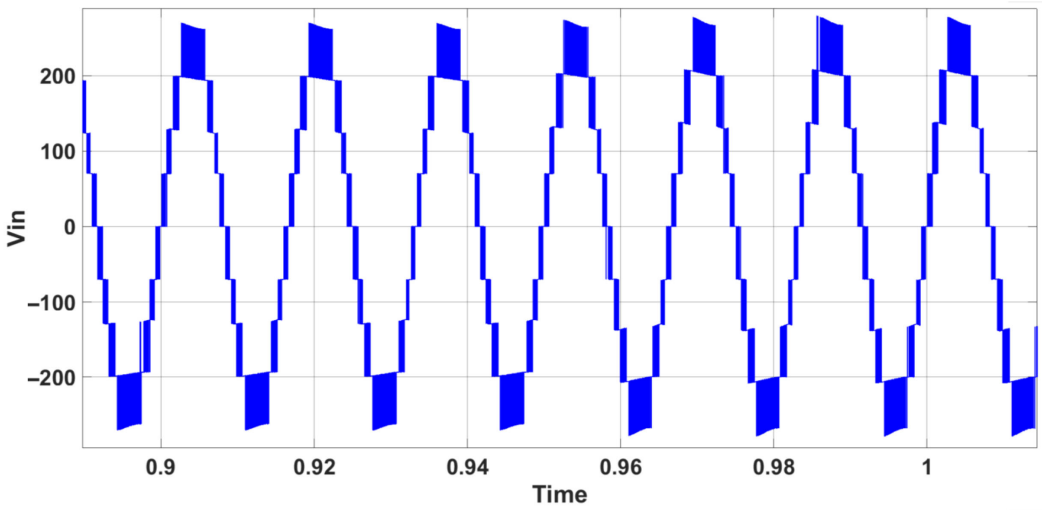

Figure 25. Inverter 7-level output voltage during irradiation variation—CSC inverter.

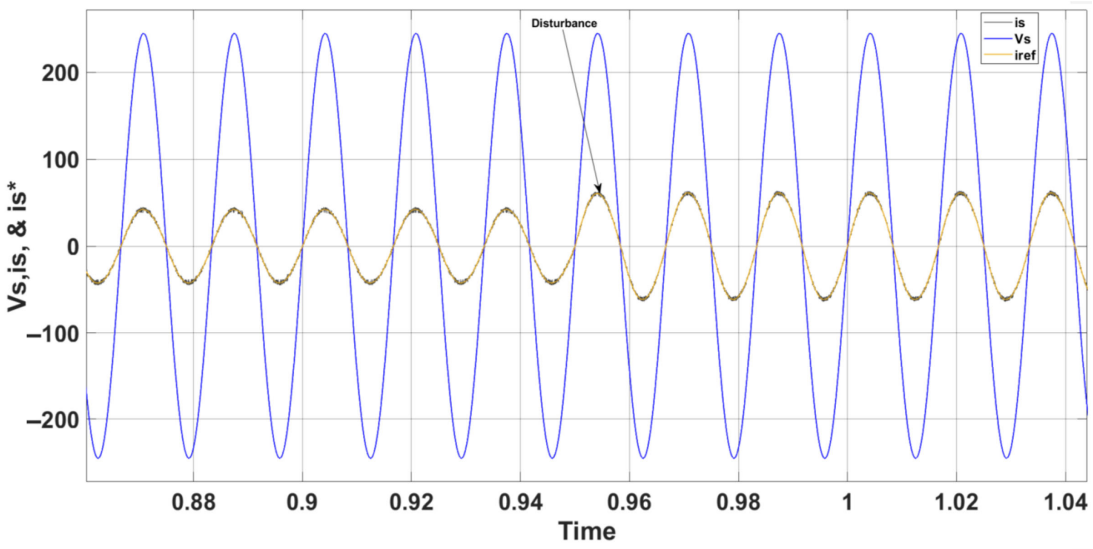

Figure 26. AC waveforms i_s (A) (multiplied by 10), i_s* (A) (multiplied by 10), and V_s (V) during irradiation variation—CSC inverter.

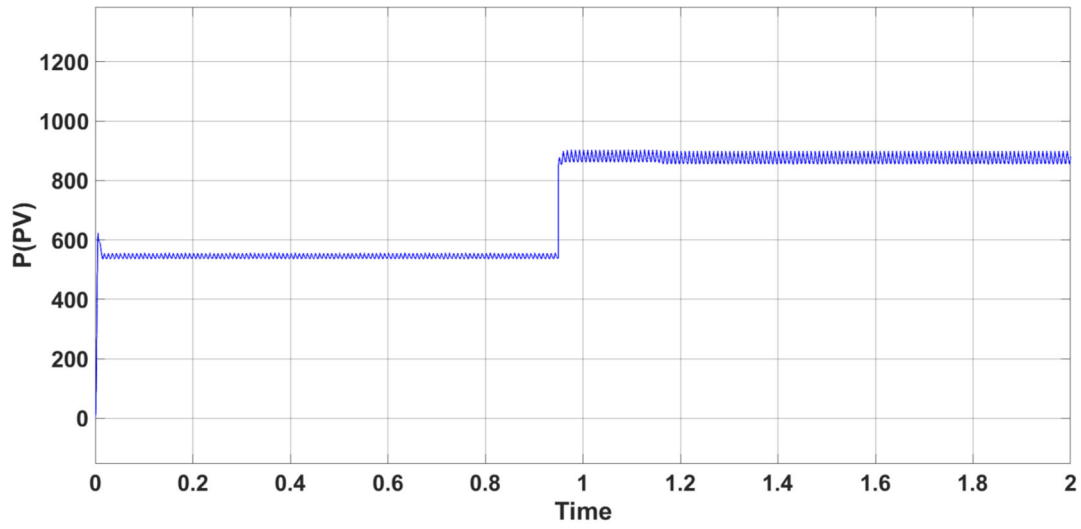

Figure 27. PV power during irradiation variation—CSC inverter.

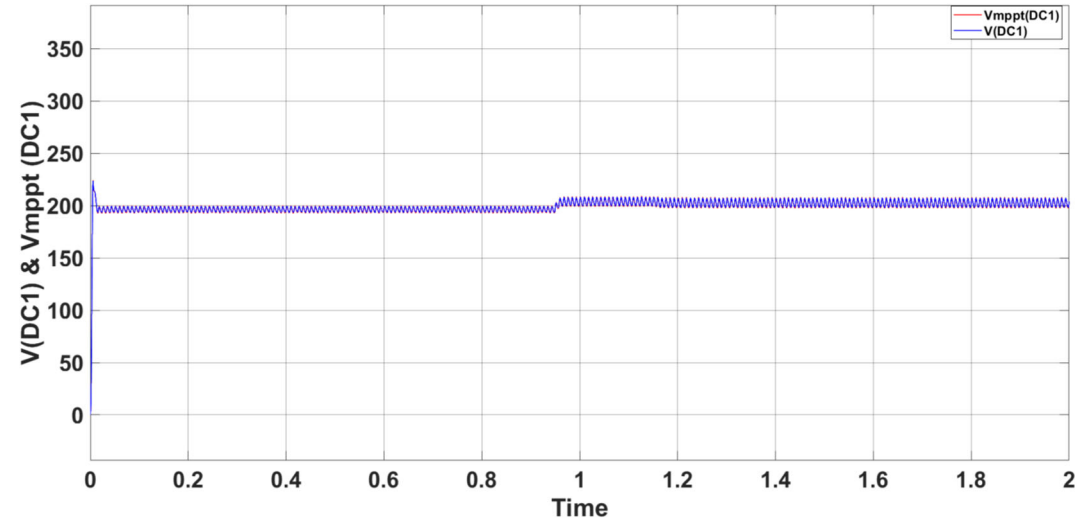

Figure 28. V_{DC1} and $V_{mppt(DC1)}$ during irradiation variation—CSC inverter.

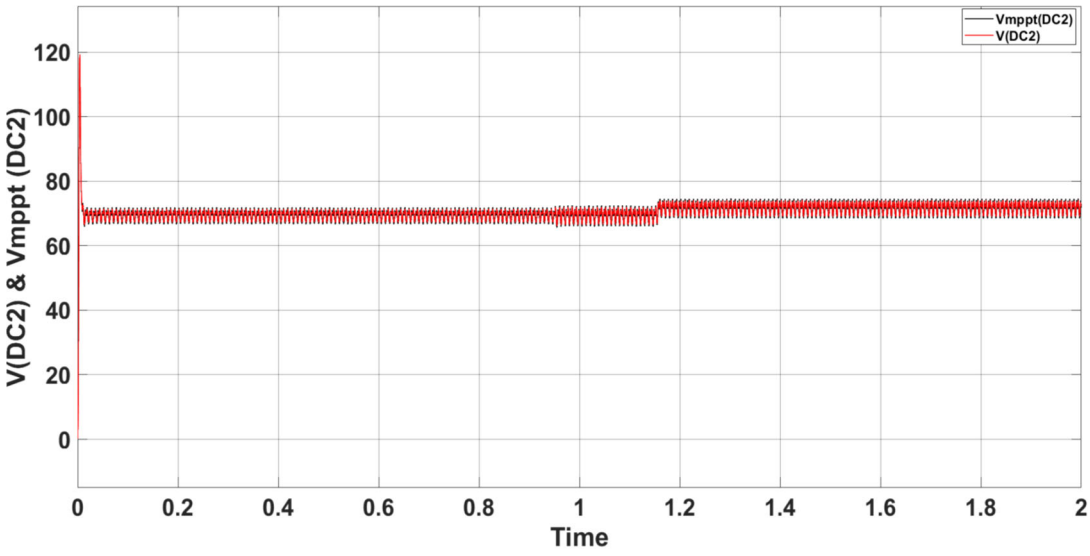

Figure 29. V_{DC2} and $V_{mppt(DC2)}$ during irradiation variation—CSC inverter.

7. Conclusions

In conclusion, the transition to renewable energy sources is imperative for addressing global energy demands and mitigating climate change. In this study, we explored the advancements in MLIs with a specific focus on the PUC inverter and the newly introduced CSC inverter. Both inverters serve the critical function of converting DC power from renewable energy sources into AC power for grid integration.

This paper is contribution for [53] in which it provides a detailed comparison between a new design for the 7-Level PUC inverter and the 9-Level CSC inverter for solar grid-tied application, both utilizing a MPC as a control strategy with Maximum Power Point Tracking (MPPT). The novelty of this paper is represented in integrating PV solar panels in both PUC inverter and CSC inverter in their two DC links and not only in one DC link like the one discussed in [47,51]. This novelty will increase the power density of the system.

The PUC inverter, with its configuration of six active switches and ability to generate up to seven distinct output voltage levels, offers a compact solution that minimizes component count while maintaining high power quality and minimizes harmonic distortion while maintaining cost-effectiveness. It effectively balances the trade-offs between performance and complexity, making it suitable for a variety of medium to high-power applications.

On the other hand, the CSC inverter represents a significant leap forward, functioning as a booster inverter that not only generates nine output voltage levels but also offers voltage levels greater (equals to 4E) than the DC input (V_1 = 3E). This boost capability, achieved through the integration of two crossover bidirectional switches to PUC inverter design, allows for flexibility and efficiency in various applications while reducing the number of required DC sources and components. This enhancement not only improves output voltage quality but also reduces manufacturing cost and complexity, positioning the CSC inverter as an attractive option for applications where minimizing system complexity and costs is essential.

The design solely relies on the MPC to control both inverters, PUC and CSC, eliminating the need for additional controllers such as PI controllers to extract grid reference current. Also, the applied strategy eliminates the need for a separate DC-DC booster converter while integrating PV solar panels to PUC and CSC inverters since the used P&O technique is directly employed to manage power delivery, ensuring efficient operation without added complexity.

Both inverters were subjected to simulations using MATLAB/Simulink to validate their performance, demonstrating robustness under various conditions, including steady state, grid voltage fluctuations, phase shift variation and changes in solar irradiation. The results confirm that the proposed designs maintain stability and efficiency, making them suitable for future integration of renewable energy sources into the grid.

Overall, while both inverter topologies provide significant advantages for renewable energy integration, the CSC inverter stands out for its superior output boosting capability and reduced component requirements as provided in Table 9. This comparison highlights the ongoing innovation within power electronics, underscoring the importance of selecting appropriate inverter technologies to facilitate a sustainable and resilient energy future. As the world moves toward cleaner energy solutions, these advancements will play a crucial role in ensuring efficient energy conversion and maximizing the utilization of renewable resources.

Table 9. Comparison between PUC inverter and CSC inverter.

Comparison Criteria	Packed U-Cell (PUC) Inverter	Cross Switches Cell (CSC) Inverter
• Number of Voltage Levels	• Up to 7 levels	• Up to 9 levels
• Number of DC Sources	• Single DC source	• Single DC source
• Number of DC busses	• Two: isolated DC source functions as the primary DC link and a capacitor functions as a secondary, auxiliary DC link	• Two: isolated DC source functions as the primary DC link and a capacitor functions as a secondary, auxiliary DC link
• Number of Switches	• Six Switches	• Eight Switches
• Number of Switching States	• Eight Switching Sates	• Sixteen Switching States
• Number of PV panels for the same AC grid V_{rms}	• For the primary DC link: 9 panels in series and 1 parallel string • For the secondary DC link: 3 panels in series and 1 parallel string	• For the primary DC link: 6 panels in series and 1 parallel string • For the secondary DC link: 2 panels in series and 1 parallel string
• Total Harmonic Distortion	• Almost 2.8% at steady stat	• Almost 3.12% at steady state
• Voltage Gain	• Almost 1/Limited to input voltage	• Almost 1.3/ Generate voltages greater than the input DC (boost feature)
• Power Boost Capability	• No	• Yes, can generate output voltage levels greater than the DC input (boost feature)
• Output Voltage Quality	• High, with reduced harmonic distortion	• Very high, with improved waveform due to increased voltage levels
• Application Suitability	• Medium to high power applications, grid-connected PV systems	• Similar but with enhanced performance due to boost feature
• Advantages	• Cost-effective, reliable, compact, fewer components • Simple topology • Simple control	• Higher voltage levels, boost capability, fewer switches for higher levels • Simple topology • Simple control

Author Contributions: Conceptualization, R.H., F.S., K.A.-H. and H.Y.K.; methodology, R.H., F.S., K.A.-H. and H.Y.K.; Validation R.H., F.S., K.A.-H. and H.Y.K.; Formal analysis, R.H., F.S., K.A.-H. and H.Y.K.; Investigation, R.H.; Resources, R.H.; Data curation, R.H.; Writing—original draft preparation, R.H.; Writing—review and editing, R.H.; Visualization, R.H.; Supervision, R.H., F.S., K.A.-H. and H.Y.K.; Project administration, F.S., K.A.-H. and H.Y.K. All authors have read and agreed to the published version of the manuscript.

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