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Statistical Performance Analysis Framework for Bundled-Data Asynchronous Circuits With Dynamic Voltage Scaling

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ABSTRACT

As the demand for low-power electronic products grows, asynchronous circuits are considered a good alternative for addressing power consumption issues. Applying dynamic voltage scaling (DVS) in asynchronous circuits can further improve their power efficiency. However, asynchronous circuits face challenges, such as performance analysis considering voltage, temperature, and process variations. This paper proposes a new statistical performance analysis model for asynchronous pipelines. This model can be applied to two different styles of asynchronous circuits. The results show that this model has reasonable accuracy on estimated mean delay (2% error on average) compared to detailed analysis carried out with low-level Monte Carlo (MC) circuit simulations.

1 | Introduction

Nowadays, designers of systems exploiting synchronous architecture face several challenges, such as global clock distribution [1]. In asynchronous circuits, eliminating global clocks offers interesting advantages such as flexible timing requirements, robust operation, improved performance, high modularity, and improved energy efficiency compared to the synchronous design style [2], making them a promising alternative for low-power applications [3]. One way to further reduce power in such systems is to apply dynamic voltage scaling (DVS), a technique widely used in synchronous designs [4]. However, in any digital circuit, process variations are exacerbated when the operating voltage is scaled to near-threshold regions [5] leading to increased delay variability that can compromise functionality and cause system failures [6–10]. Within the asynchronous design space, different circuit styles exhibit different sensitivities to variability. Quasi-delay-insensitive (QDI) circuits [11] are generally more robust to delay variability because their correct operation relies on delay-insensitive communication and completion detection [12, 13]. In contrast, bundle-data (BD) circuits are more sensitive to variability. Despite this sensitivity, BD circuits are often preferred in practice because they can be implemented using standard-cell elements, without special gates such as Muller C-elements, which are typically absent from industrial libraries.

The power and energy advantages of asynchronous circuits are therefore highly design-dependent and vary across styles (QDI vs BD), control schemes, and application domains. Our goal is not to claim that BD circuits are universally more power-efficient than synchronous ones, but to focus on BD pipelines as a practically relevant asynchronous style for which recent silicon implementations (e.g., BD CNN accelerators and RISC-V processors) have demonstrated meaningful energy savings relative to synchronous baselines [14, 15]. This paper concentrates on statistical timing and timing-yield modeling for BD pipelines under process variations and DVS, providing a quantitative framework to analyze how BD timing constraints behave under variability and voltage scaling, rather than attempting a full architectural

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comparison between QDI, BD, and synchronous designs. In this context, it becomes essential to develop models and methods that enable simultaneous evaluation and verification of timing and performance for BD asynchronous circuits in the presence of process variations. The GAELS project [16] is an example of a study that addresses these issues specifically for elastic GALS circuits. Different works addressing these challenges will be examined in the related work section. As process variations have become a significant problem in deep sub-micron technology, concerns were raised over static-timing analysis (STA) accuracy based on deterministic delay [17–20]. In modern industrial flows, deterministic STA combined with on-chip variation (OCV), advanced OCV (AOCV), and parametric OCV (POCV) is the defacto sign-off methodology at advanced technology nodes. Throughout this paper, the term STA is used to denote this conventional deterministic, corner-based timing verification, possibly enhanced with OCV/AOCV/POCV derating. At the same time, fully statistical STA (SSTA) remains particularly attractive for capturing PVT variations in dynamic-voltage and near-/sub-threshold regimes. The term SSTA refers exclusively to probabilistic delay analysis in which delays are treated as random variables, and timing is characterized in terms of distributions (mean and standard deviation) rather than fixed worst-case numbers. In this work, we adopt an SSTA-inspired analytical framework specialized for bundled-data asynchronous circuits under DVS, where conventional synchronous flows provide limited guidance on pulse-based logic constraints and handshake timing [10, 19, 20]. SSTA therefore requires that delays must be modeled as probability distribution functions (PDF) instead of deterministic values. As the performance of those bundled data asynchronous circuits depends on their structure scheme and environment, multiple design parameters must be appropriately selected to satisfy statistical timing constraints (design scheme, architecture configuration, logic structure, and circuit timing yield). Environmental conditions such as temperature variations and voltage scaling can also affect circuit performance [20, 21].

In contrast, SSTA, the statistical parameters used in our model (e.g., the standard deviations of pulse width and gate delay) are obtained from SSTA-style Monte Carlo (MC) simulations and not from deterministic STA.

This paper proposes a statistical analysis framework to efficiently evaluate the constraints of asynchronous circuits belonging to the bundled data class under process variations. We are interested in applying DVS in these asynchronous circuits. First, a delay variability model is presented to estimate the impact of process variation on the targeted asynchronous circuit performance from the nominal to near-threshold region. Then, a statistical analysis model is developed considering various statistical constraints: timing (setup and hold) constraints and logic component (namely pulse width) constraints. For statistical timing constraint verification, both setup and hold constraints are checked using the proposed timing yield metric for different operating voltages. Finally, a new specification is proposed for statistical logic component constraints to prevent system failures and to ensure correct signal propagation when operating voltages decrease. Then, the impact of temperature variations is estimated using the Hspice simulation tool to verify previously defined statistical constraints.

At the combinational logic level, the benchmark paths are conventional gate-level logic clouds, implemented in a 90 nm BSIM4-based standard-cell library and subjected to the same process, voltage, and temperature (PVT) variations as synchronous designs. The distinctive aspect of our study is therefore not the logic clouds themselves, but their integration within self-timed single-rail bundled-data handshake-free (SRBDHF) and Click controllers, where local handshakes and matched delay lines enforce bundled-data timing. As a result, the variability and DVS behavior observed on the logic clouds is representative of synchronous implementations, while the timing constraints we analyze—pulse-based logic constraints and handshake timing margins—are specific to bundled-data asynchronous pipelines. Although BD pipelines share many structural similarities with synchronous pipelines at the combinational datapath level, our framework is specifically targeted at self-timed BD pipelines operating under DVS, as found in our industrial collaboration with Octasic on clockless processors. In this class of designs, execution units (EUs) are self-timed, driven by local launch/done pulses and programable completion delay chains, and timing is governed by local completion detection and matched delay lines rather than a global clock tree. Consequently, the statistical constraints in our framework are formulated on asynchronous handshaking mechanisms (pulse-width conditions, matched delays, and handshake timing margins) instead of clock-based setup/hold constraints. The underlying SSTA engine remains generic and could, in principle, be extended to synchronous pipelines by substituting appropriate clock-tree-based constraints, but this would require explicit modeling of clock-tree variation, skew distributions, and clock-synthesis assumptions, and is left for future work.

The rest of the paper is organized as follows: Section 2 presents the related work. Section 3 provides critical preliminary information. Section 4 presents the proposed statistical analysis framework for asynchronous circuits. Section 5 presents results obtained by applying our proposed framework to a simple asynchronous benchmark circuit. Conclusions drawn from this work are summarized in Section 6.

2 | Related Work

The related literature can be grouped into two main families. The first family consists of bundled-data asynchronous design flows based on deterministic STA, where timing verification is performed with corner-based analyses and fixed margins. The second family comprises statistical or formal approaches for asynchronous or elastic circuits that explicitly consider process variations and, in some cases, dynamic voltage and frequency scaling. For each of these groups, we briefly summarize below the main ideas, typical assumptions, and limitations with respect to our objective: a statistical performance-analysis framework that simultaneously accounts for setup, hold, and pulse-based logic constraints (including propagation-induced pulse broadening [PIPB]) in bundled-data pipelines under DVS.

In deterministic STA-based flows, process variations are recognized as a major concern in the design of bundled-data asynchronous circuits. Threshold voltage and device dimensions are typically identified as primary sources of variability; for example, in the subthreshold region, the threshold voltage dominates performance shifts compared to other parameters such as oxide thickness [22]. The works in [2, 23] propose error-free

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asynchronous circuits suitable for full-range DVS, but do not incorporate process variations into the performance analysis, which leads to uncertainty in the predicted behavior. Other studies explicitly include variability but remain within deterministic STA. In [24, 25], the authors analyze the performance of Click-based asynchronous circuits using corner-based STA. The work in [26] evaluates different asynchronous designs under process variations, yet limits timing analysis to worst-case operating corners to guarantee error-free operation under all physical conditions. Similarly [27], investigates asynchronous circuits with DVS for power reduction and evaluates timing deterministically across operating conditions. A design framework for QDI asynchronous circuits with DVS is presented in [28]; while timing under variability is considered, only global process variations and worst-case corners are modeled. Overall, these studies rely on deterministic STA rather than a fully statistical treatment of timing.

Statistical and formal approaches have also been explored to capture process variations in the performance analysis of asynchronous circuits. In [29], the authors introduce a modeling approach for elastic circuits by translating an xMAS-based formal model into a stochastic activity network (SAN), enabling statistical performance evaluation under process variation; however, low operating voltages, voltage scaling, and logic constraints are not addressed, and functional correctness is checked only through setup constraints. The work in [30] proposes a statistical design methodology for template-based asynchronous circuits using an extended timed petri-net model; the analysis focuses on comparing the mean and variance of leakage power between the proposed approach and MC simulations, without discussing timing or logic verification constraints. In [31], a statistical framework is presented to analyze asynchronous circuits across a wide range of supply voltages using an analytical variability model; the performance analysis includes delay and protocol overhead but does not cover statistical timing and logic constraints such as the pulse width in delay lines, which is critical for the class of circuits considered here. Finally [32], employs formal models based on generalized stochastic petri nets (GSPN) to perform statistical performance analysis, where the probability of meeting setup constraints under process variation is used to verify correct functionality; hold-time constraints, logic constraints, and voltage scaling are not supported in this model.

Table 1 summarizes representative prior works from both families and compares them with the proposed framework across various aspects: statistical logical verification in SRBDHF asynchronous circuits, statistical timing for setup and hold times, the technology used, and dynamic power supply voltage variation. The selection criterion for these works is based on studies that conduct statistical analysis on specific asynchronous circuits. A plus sign (+) indicates that a method considers a specific aspect, while a minus sign (−) means this aspect is not considered. Our approach integrates the verification of statistical logical constraints in SRBDHF asynchronous circuits, distinguishing it advantageously from other works that do not consider this. Regarding statistical timing verification, we consider setup and hold margins for all registers, ensuring the satisfaction of the circuit's overall timing constraints. This broader approach distinguishes itself from other literature focusing only on setup margins. The "Technology (nm)" column indicates the Nanometer manufacturing technology used for each work. For example, our proposed model uses a 90 nm technology. Other literature works used manufacturing technologies of 32, 90, 40, 65, and 180 nm.

Finally, our proposed method considers power supply voltage variation. This means that our method considers the verification of constraints related to power supply voltage variation and ensures that the circuit functions correctly. This constitutes a significant advantage compared to other approaches in the literature that do not consider this.

Note that [28] considers one aspect not covered in our work: spatial correlation. However, it does not consider the DVS effect on the asynchronous circuit or the three verification steps listed in Table 1, which can influence its correct operation.

In contrast, our work introduces a statistical analysis framework for two classes of bundled-data asynchronous circuits that combines variability and performance models to evaluate circuit behavior efficiently overall operating voltages in the presence of parametric and temperature variations. This framework uses analytical modeling rather than extensive MC SPICE simulations, which are employed here only as a reference. Finally, as shown later in this paper, our work exhibits the lowest average error on mean delay values with respect to MC SPICE simulations.

3 | Preliminaries

This section covers the following items: Section 3.1: The basic equations we modified and adapted to our specific purposes, Section 3.2: The timing yield, and Section 3.3: The bundled-data asynchronous circuits we target.

3.1 | Basic Equations

There are two basic equations from which we start to develop our models. The first is a unified gate delay propagation formula developed in [35], which is given by:

TABLE 1 | Summary of prior statistical verification methods versus the proposed framework.

Features	[27]	[29]	[30]	[28]	[33]	[34]	Ours
Statistical logic verification (SRBDHF)	−	−	−	−	−	−	+
Statistical timing verification (setup)	+	+	+	−	−	−	+
Statistical timing verification (hold)	−	−	−	−	−	−	+
Technology (nm)	32	90	32	90	40, 65, 180	130	90
Voltage scaling	−	+	−	−	+	−	+

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$$T_{\mathrm{d}} = \frac{\mathrm{KV}_{\mathrm{DD}}\left\{1+\ln\left[1+\exp\left(\frac{V_{\mathrm{DD}}-V_{\mathrm{th}}}{E_{\mathrm{sat}}L}\right)\right]\right\}}{\left\{\ln\left[1+\exp\left(\frac{V_{\mathrm{DD}}-V_{\mathrm{th}}}{2S}\right)\right]\right\}^{2}}, \quad (1)$$

where the terms are defined as follows: T_{d} represents the gate delay, the time it takes for the gate to transition between states; K is a Proportionality coefficient that can be extracted from simulation data under different conditions of V_{DD}, L, and load capacitance; V_{DD} is the supply voltage; V_{th} is the threshold voltage, marking the point at which the transistor turns on and conducts; S is the subthreshold swing, describing the steepness of the transition between the on and off states; L is the channel length of the transistor; and E_{sat} is the velocity saturation parameter, which limits the carrier speed in the transistor channel at higher voltages.

One of the key strengths of this formula is its adaptability to different technology nodes. As semiconductor technology advances, the parameters that influence gate delay such as channel length, threshold voltage, and subthreshold swing must be adjusted to reflect the properties of smaller transistors. In modern nodes, the channel length typically shrinks, making the transistor's switching behavior more sensitive to the E_{sat} parameter, which becomes a more significant factor in determining gate delay. Smaller nodes also see a reduction in V_{th} due to the need for lower supply voltages and improved switching efficiency. Additionally, as nodes shrink, S tends to become steeper, meaning that transistors switch more sharply between their on and off states, further reducing delay.

By tuning these parameters based on the characteristics of each technology node, the formula can accurately model gate delays for various semiconductor processes, making it a versatile tool for circuit designers.

Temperature variations play a critical role in transistor behavior, particularly by influencing V_{th} and carrier mobility. As the temperature increases, higher temperatures cause V_{th} to decrease, making the transistor more likely to turn on, thus reducing delay. However, higher temperatures also lead to a decrease in carrier mobility, which increases delay. Our current model uses simulation results to analyze the effects of temperature on gate delays. While more detailed temperature models exist, incorporating such temperature-dependent expressions for the relevant parameters will be considered in future work to refine the model further.

The formula can also be adapted to various gate topologies, such as those involving PMOS or NMOS transistors. When evaluating the gate delay, the threshold voltage used in the formula must correspond to the active transistor type: for PMOS transistors, the threshold voltage used is V_{thp}, and for NMOS transistors, it is V_{thn}. This adjustment ensures that the model remains accurate across different gate configurations. By considering the specific transistor type, whether NMOS or PMOS, the model accurately reflects the contributions of each type of transistor to the overall gate delay, making it adaptable to various topologies in CMOS circuit design. For instance, the output transition through serially connected NMOS transistors in a NAND gate determines the high-to-low propagation delay. Conversely, the low-to-high propagation delay occurs via parallel-connected PMOS transistors. This analytical approach can be easily extended to other multiple-input logic gates.

The second basic equation is given by the following expression, ensuring proper pulse propagation in delay lines used in asynchronous circuits [10]:

$$\mathrm{Nb} < \frac{\mathrm{PW}_{V_i}}{|t_{\mathrm{pLH}} - t_{\mathrm{pHL}}|(V_i)}, \quad (2)$$

where Nb is the number of identical gates in the delay line, PW_{V_i} the measured pulse width at voltage V_i, defined as the time interval between the rising and falling 50 % V_{DD} crossings at the node where the pulse enters the delay line. In the following, t_{pLH} and t_{pHL} denote the 50%–50% rise and fall propagation delays, respectively, measured from the 50 % point of the input transition to the 50% point of the output transition. These quantities correspond to the standard $t_{\mathrm{pLH}}$and t_{pHL}timing arcs in static timing analysis (STA); they do not represent output transition times (slews). $t_{\mathrm{pLH}} - t_{\mathrm{pHL}}$ is the difference between rise time and fall time propagation delays at voltage V_{i}, capturing transition imbalances that may distort the pulse, and V_{i} the operating supply voltage.

The formula ensures the pulse width PW_{V_i} is sufficiently large relative to rise and fall delays $|t_{\mathrm{pLH}} - t_{\mathrm{pHL}}|$ for distortion-free propagation through Nb gates. Short pulse widths can fail to preserve the signal. Asymmetric rise and fall times $|t_{\mathrm{pLH}} - t_{\mathrm{pHL}}|$ can accumulate distortion across gates. Appropriate Nb maintains signal shape, and analyzing these at V_i ensures accuracy. Equation (2) is therefore evaluated at the input of the delay line and expresses a global minimum-pulse-width condition: it ensures that an input pulse of width PW_{V_i} can propagate through Nb stages of the homogeneous chain without being annihilated at any internal node. For example, in a delay line consisting of 71 OR gates, a pulse of 6.85 ns width is lost after the 69th stage under the operating conditions (0.7 V, SS, 125°C).

3.2 | Timing Yield

The second item covered in this section is the timing yield [36], a key metric for digital circuits that measures the percentage of chips that meet a specified timing requirement.

In this work, yield always refers to timing yield, that is, the probability that a circuit satisfies its setup- and hold-time constraints under the modeled process variations. This is a design-side quantity that can be computed analytically from the distribution of critical-path delays for a given frequency target and does not require access to proprietary foundry data. It is therefore fundamentally different from manufacturing yield, which depends on defect mechanisms and process control in the fabrication line and is typically confidential. Our framework focuses exclusively on timing yield and is aligned with the standard SSTA literature.

To evaluate timing yield, a timing analysis is first performed to determine the critical-path delay of the circuit, defined as the longest delay path from a flip-flop output to a flip-flop input, which sets the maximum operating frequency. The timing yield is then obtained using statistical methods based on the distribution of delay values in the circuit, typically modeled as Gaussian. The detailed derivation of the timing-yield expression is provided in Section 4.

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3.3 | Targeted Bundled-Data Asynchronous Circuits

The pipelines used in this paper belong to the bundled-data asynchronous circuit class. Two different pipelines are used to validate the statistical analysis framework for asynchronous circuits.

The first is called a SRBDHF pipeline. Successful research has been conducted and published addressing the flow design of this type of circuit [36, 37]. Additionally, these circuits have been tested [37, 38]. These types of circuits are commercialized by Octasic [39]. However, in this work, our focus is on statistical analysis performance.

As its name implies, this pipeline does not use any handshake mechanism. This design style relies on several EUs that communicate in a sequential ring. A simplified example of the basic architecture of an EU is illustrated in Figure 1. It is composed of a combinational logic cloud, a variable delay line (namely, a configurable block adjusted to the operation performed at a given cycle), and source (SRC) and destination (DST) registers. The SRC register is triggered by the pulse from the pulse generator block, which launches the data to the logic cloud. The data from the logic cloud is captured by the DST register, which is triggered by a delayed pulse.

The second targeted pipeline is the click pipeline circuit [40]. It is composed of a combinational logic cloud, source and destination registers, and two communication protocol signal blocks named click-elements (Figure 2). When new data is ready, a transition of the request signal *Req_in* in click_element1 is used to generate a local clock *f*1. The transition of the *Req_in* signal can be delivered to *Req_out* of click_element2, which becomes the *Req_in* signal of the next stage. The signal *f*1 is used to capture the *data_in* and to trigger the click_element2 to generate *f*2. Then, a transition of the acknowledge signal *Ack_in* in click_element2 indicates the end of this action. Both the rising and falling transitions of the request signal indicate the validity of the data, and both the rising and falling transitions of the acknowledge signal indicate that the data has been captured.

4 | Proposed Method

4.1 | Statistical Analysis Framework

This section presents a novel methodology for performing statistical analysis on the target asynchronous circuits. The methodology estimates performance while considering those asynchronous circuits' process, temperature, and voltage variation. We follow a series of steps to ensure correct operation in our statistical timing model. We begin by presenting the variability model used in our proposed model. The next step involves verifying the statistical logic constraints to ensure correct pulse propagation. Finally, we check the statistical timing constraints to ensure the model operates correctly.

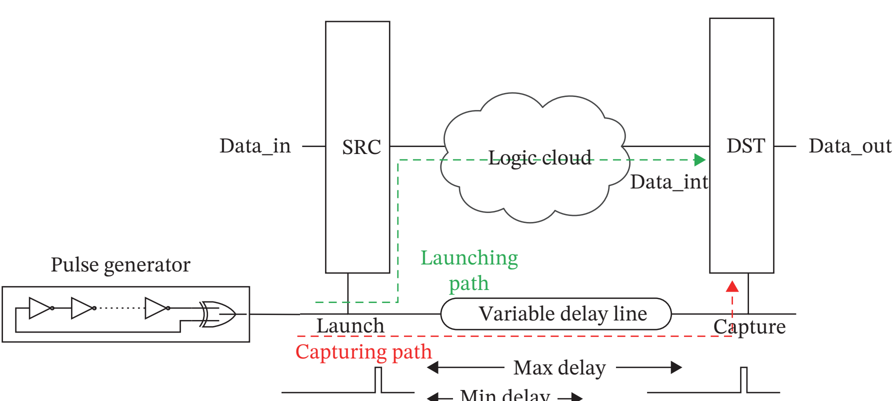

FIGURE 1 | SRBDHF pipeline circuit.

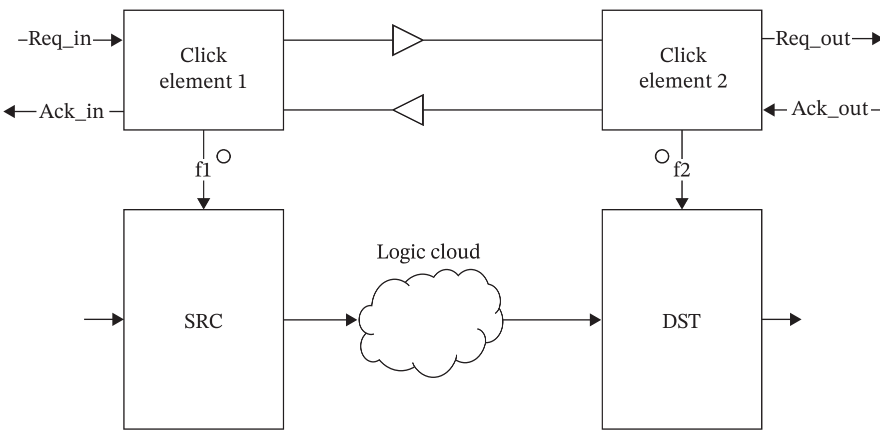

FIGURE 2 | Click pipeline circuit.

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4.1.1 | Variability Model

The variability model follows the canonical first-order SSTA formulation, in which each gate delay is expressed as an affine function of a set of random process parameters with specified means, variances, and correlations. Device-level quantities such as threshold voltages, channel length, mobility, and oxide thickness are modeled as correlated Gaussian variables. This parametric structure is directly compatible with classical SSTA and parametric-yield frameworks: extending the model to a new technology node amount to augmenting the set of random parameters and updating their covariance matrix based on the corresponding PDK, without changing the form of the statistical engine itself. To estimate the delay variability of a gate, we consider two major parametric variation components: threshold voltage variations due to random dopant fluctuations and device length in ambient temperature. Based on Equation (1), the analytical gate delay T_d, now representing the average delay over a pair of gates, is given by Equation (3), considering the effect of the threshold voltage V_{th} and device length L:

$$T_{\mathrm{d}} = K1\frac{V_{\mathrm{DD}}\left(1+\frac{V_{\mathrm{DD}}-V_{\mathrm{thn}}}{E_{\mathrm{sat}}L}\right)}{(V_{\mathrm{DD}}-V_{\mathrm{thn}})^2} + K2\frac{V_{\mathrm{DD}}\left(1+\frac{V_{\mathrm{DD}}-|V_{\mathrm{thp}}|}{E_{\mathrm{sat}}L}\right)}{(V_{\mathrm{DD}}-|V_{\mathrm{thp}}|)^2}, \tag{3}$$

where V_{DD}, V_{thn}, V_{thp}, E_{sat}, L, $K1$, and $K2$ are the operating voltage, NMOS and PMOS threshold voltages, the critical electric field from which carrier velocity saturation appears in the channel, device length, and proportionality factors, respectively. The analysis of temperature variation is performed using the Hspice simulation tool. The best and worst temperature values are considered to verify various statistical constraints defined below.

The statistical delay of T_{d} is composed of two independent random variables V_{th} and L. These random variables correspond to physical and performance parameters. As discussed in [41, 42], although the behavior of these variables may not be strictly normal, it can be approximated as normal distributions, with a mean value of μ and a variance of σ^2. These values are provided by the foundry for the relevant technological and performance parameters.

The mean delay is obtained by evaluating delay function Equation (3) at nominal values of the variation parameter:

$$\mu_{T_{\mathrm{d}}} = \left[K1\frac{V_{\mathrm{DD}}\left(1+\frac{V_{\mathrm{DD}}-V_{\mathrm{thn}}}{E_{\mathrm{sat}}L}\right)}{(V_{\mathrm{DD}}-V_{\mathrm{thn}})^2} + K2\frac{V_{\mathrm{dd}}\left(1+\frac{V_{\mathrm{DD}}-|V_{\mathrm{thp}}|}{E_{\mathrm{sat}}L}\right)}{(V_{\mathrm{DD}}-|V_{\mathrm{thp}}|)^2}\right]_{\mathrm{nom}}. \tag{4}$$

To derive the standard deviation equation, the delay function is first approximated by a first-order Taylor series expansion. Then, by applying the second moment to the expanded expression of the approximated delay function [43], the standard deviation of T_{d} is given by:

$$\sigma_{T_{\mathrm{d}}} = \sqrt{\sum_i S^2_{T_{\mathrm{d}},P_i}\sigma^2_{P_i} + 2\sum_{i=1}^{n-1}\sum_{j=i+1}^{n}\mathrm{cov}\left(P_i,P_j\right)}. \tag{5}$$

Here, $S^2_{T_d,P_i}$ are the sensitivities of T_{d} with respect to each process parameter, $\sigma^2_{P_i}$ are the variances of the individual parameters, and $\mathrm{cov}\,(P_i, P_j)$ are the covariance terms that account for correlations between parameters.

The sensitivities of T_{d} to key process parameters are calculated as:

$$S^2_{T_{\mathrm{d}},V_{\mathrm{thn}}} = \left(\frac{\partial T_{\mathrm{d}}}{\partial V_{\mathrm{thn}}}\right)^2, \tag{6}$$

$$S^2_{T_{\mathrm{d}},V_{\mathrm{thp}}} = \left(\frac{\partial T_{\mathrm{d}}}{\partial V_{\mathrm{thp}}}\right)^2, \tag{7}$$

$$S^2_{T_{\mathrm{d}},L} = \left(\frac{\partial T_{\mathrm{d}}}{\partial L}\right)^2. \tag{8}$$

These partial derivatives quantify the sensitivity of T_{d} to threshold voltages (V_{thn}, V_{thp}) and device length (L).

The covariance between parameters, such as V_{thn}, V_{thp} and L, is incorporated to model their correlation. The covariance $\mathrm{cov}(P_i, P_j)$ is calculated as:

$$\mathrm{cov}\left(P_i, P_j\right) = \rho_{P_i,P_j}\,\sigma_{P_i}\,\sigma_{P_j}, \tag{9}$$

where ρ_{P_i,P_j} is the correlation coefficient between the distributions of P_i and P_j, and σ_{P_i}, σ_{P_j} are their standard deviations.

Thus, the total variance of the delay T_{d} is given by:

$$\begin{aligned}\sigma^2_{T_{\mathrm{d}}} &= S^2_{T_{\mathrm{d}},V_{\mathrm{thn}}}\sigma^2_{V_{\mathrm{thn}}} + S^2_{T_{\mathrm{d}},V_{\mathrm{thp}}}\sigma^2_{V_{\mathrm{thp}}} + S^2_{T_{\mathrm{d}},L}\sigma^2_L \\ &+2\sum_{i=1}^{n-1}\sum_{j=i+1}^{n} S_{T_{\mathrm{d}}P_i}S_{T_{\mathrm{d}}P_j}\rho_{P_i,P_j}\,\sigma_{P_i}\,\sigma_{P_j}.\end{aligned} \tag{10}$$

This paper will use Equations (4) and (5) as our delay variability models to estimate the delay variability of asynchronous circuits under process variations. More parametric variation components can be incorporated in Equation (5) to improve model accuracy.

4.1.2 | Statistical Logic Constraint

When the propagation of rise and fall transitions is not perfectly balanced, the propagation of a pulse may be stopped in a delay line and cause a system failure. A pulse width can be decreased/increased by the difference between the respective durations of the two transitions [44, 45]. In this work, the condition in Equation (11) is evaluated for homogeneous delay lines composed of identical standard-cell gates, as used in the SRBDHF controllers considered here. This setting captures the steady-state pulse-propagation behavior of the delay elements under DVS. Extending this propagation condition to heterogeneous chains that combine different gate types, drive strengths, and longer interconnect segments would require a more general, stage-by-stage modeling of pulse distortion akin to PIPB analyses in the literature [33, 34, 46, 47]. Considering process variation and DVS, the effects of the broadening/shrinking phenomenon are generally amplified. Based on Equation (2), we can derive the following statistical expression, ensuring proper pulse propagation based on the usual 3 sigma limit in the SRBDHF targeted type of circuits:

$$(\mathrm{PW} - 3\sigma_{\mathrm{DIFF}})_{V_i} > (\mathrm{Nb}\,|\mathrm{diff}| + 3\sigma_{\mathrm{PW}})_{V_i}, \tag{11}$$

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$$\mathrm{diff} = t_{\mathrm{pLH}} - t_{\mathrm{pHL}}, \tag{12}$$

where t_{pLH} and t_{pHL} are still, respectively, the (50%–50%) rise and fall transition propagation delays at a specified voltage, Nb the number of identical gates in the delay line, PW the pulse width associated to a specified voltage V_{i}, σ_{DIFF} the standard deviation of the difference delay between rise and fall transition over the entire delay line composed of Nb gates ($\mathrm{Nb}\,\sigma_{\mathrm{diff_gate}}$), $\sigma_{\mathrm{diff_gate}}$ of the difference delay between rise and fall transition over one gate, σ_{PW} the standard deviation of the pulse width parameter and V_{i} the operating supply voltage. As the propagation delay associated with rise and fall transitions increases when the supply voltage decreases, the pulse injected in a delay line of the SRBDHF circuit should satisfy the condition defined in Equation (11) for all given DVS conditions. In Equation (11), the number of stages Nb in the delay line appears explicitly because both the deterministic drift of the pulse width and its variance accumulate along the chain. At each stage, the difference between the rise and fall propagation delays contributes a small change to the local pulse width; the total deterministic change grows approximately in proportion to Nb $|\mathrm{diff}|$. Similarly, assuming independent or weakly correlated per-stage variations, the variance of the accumulated broadening term increases with Nb, so the standard deviation σ_{PW} scales with $\sqrt{\mathrm{Nb}}$. The form of Equation (11) therefore reflects the fact that longer delay lines are more susceptible to PIPB-induced pulse distortion and to variability in that distortion.

In Click pipeline circuits, the correct operation relies on generating well-defined control signal pulses ($f1$ and $f2$), which do not rely on launching pulses in the delay lines. This implies that the control signal pulse width must be larger than the minimum pulse width defined in the technology library.

In Click-style pipelines, the control pulse that triggers the flip-flop must satisfy the minimum pulse-width constraint specified by the standard-cell library on the clock pin. Within our statistical framework, this constraint can be expressed in terms of the random pulse width at the flip-flop input: a deterministic safety margin corresponds to $\mu_{\mathrm{PW}} \geq \mathrm{MPW}$, where MPW is the library min_pulse_width, while a statistical formulation for a target timing yield requires $\mu_{\mathrm{PW}} - k \cdot \sigma_{\mathrm{PW}} \geq \mathrm{MPW}$ for a chosen margin factor k. These inequalities show how the quantities μ_{PW} and σ_{PW} extracted from our model can be directly related to the conventional min_pulse_width constraint used in synchronous timing sign-off.

4.1.3 | Statistical Timing Constraints

Here we derive the statistical timing constraints, namely the setup and hold time constraints. We assume here that the variability of combinatorial logic and delay lines in SRBDHF and Click circuits can be modeled by a normal distribution with probability density functions (PDFs) f_{logic}, f_{De}, and f_{T1}, respectively. To analyze the impact of manufacturing process variations on the performance of these circuits, we can express these three PDFs as:

$$f_{\mathrm{logic}} = N\left(\mu_{\mathrm{logic}}, \sigma^2_{\mathrm{logic}}\right), \tag{13}$$

$$f_{\mathrm{De}} = N\left(\mu_{\mathrm{De}}, \sigma^2_{\mathrm{De}}\right), \tag{14}$$

$$f_{T1} = N\left(\mu_{T1}, \sigma^2_{T1}\right). \tag{15}$$

Starting with the setup time constraint, to ensure the reliability of synchronization constraints while accounting for manufacturing process variations, the line's delay must always be greater than the critical path delay. The statistical specification requires that the probability of meeting this constraint is, in theory, equal to 1. These synchronization constraints for two types of asynchronous circuits (SRBDHF and Click, respectively) are theoretically defined as follows:

$$P\left(f_{\mathrm{logic}} < f_{\mathrm{De}}\right) = 1, \tag{16}$$

and

$$P\left(f_{\mathrm{logic}} < f_{T1}\right) = 1. \tag{17}$$

In practice, a small probability of failure exists despite compliance with the constraints, related to the timing yield (discussed later). Note that this is also the case for static analysis constraints. The statistical constraint preventing (with a very high probability) a violation of the setup time constraints based on the traditional 3 sigma limit for SRBDHF and Click asynchronous circuits, respectively, for a given supply voltage V_{i} is:

$$\mathrm{MS}_i = \left((a_i \mathrm{De}) - b_i D_{\mathrm{CLmax}}\right) - 3c_i \sigma_{\mathrm{Dclmax}} - 3d_i \sigma_{\mathrm{De}} - \mathrm{su}\right)_{V_i} > 0, \tag{18}$$

$$\mathrm{MS}'_i = \left(a'_i T1\right) - \left(b_i\, D_{\mathrm{clmax}}\right) - \left(3c_i\, \sigma_{\mathrm{Dclmax}} - 3d'_i\, \sigma_{T1} - su\right)_{V_i} > 0, \tag{19}$$

where D_{CLmax} represents the mean value of maximum path delay in the logic cloud, De the mean value of maximum propagation delay in the delay line of the SRBDHF circuit, and $T1$ the mean value of maximum propagation delay from the rising edge $f1$ to $f2$ in the Click circuit. The terms σ_{Dclmax}, σ_{De}, and σ_{T1} correspond to their respective standard deviation, while V_i is the operating voltage and su the required setup time. For simplicity, we assume that zero value of su can be used for all voltage values. Finally, the terms a_i, a'_i, b_i, c_i, d_i, and d'_i are growth factors (≥1) to model the increase in delay mean and standard values when the operating voltage is decreased. Note that the terms b_i and c_i are common to both (Equation 18) (SRBDHF) and (Equation 19) (CE) as both use the same combinational logic. We call MGF the mean growth factors associated to the delay mean values (namely terms a_i, a'_i, b_i) and SGF the ones associated with the delay standard deviation values (namely c_i, d_i, and d'_i). The MGFs (SGFs) are expressed as the ratio of the delay mean (standard deviation) at V_{i} over the same delay mean (standard deviation). It is worth noting that the difference between statistical and STA is that the 3 sigma limit is here applied to the entire delay line or logic cloud. In contrast, it is applied separately to each gate for the latter. These equations (Equations 18, 19) ensure that the delay through logic does not exceed those of the delay line to avoid synchronization failure.

The second required statistical timing constraint is the hold time one. As mentioned before, hold time violations occur when race-through is possible. The statistical constraint based on the traditional 3 sigma limit for SRBDHF and Click asynchronous circuit, respectively for a given operating voltage V_i is:

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$$\mathrm{MH}_i = \left((e_i\, D_{\mathrm{CLmin}}) + (f_i T_c) - (a_i \mathrm{De}) - 3d_i\sigma_{\mathrm{De}} - 3g_i\sigma_{T_c} - 3h_i\,\sigma_{\mathrm{Dclmin}} - \mathrm{hold}\right)_{V_i} > 0, \tag{20}$$

$$\mathrm{MH}_i' = (e_i D_{\mathrm{CLmin}} + j_i T2 - 3h_i\,\sigma_{\mathrm{Dclmin}} - 3l_i\sigma_{T2} - \mathrm{hold})_{V_i}, \tag{21}$$

where D_{CLmin} represents the mean value of minimum path delay in the logic cloud, T_c the launch pulse cycle duration (namely, the time required for a token to cycle back to an EU and relaunch a pulse), and $T2$ propagation delay from rising edge $f2$ to $f1$. The terms σ_{Dclmin}, σ_{Tc}, and σ_{T2} correspond to their respective standard deviation, while hold is the required hold time margin Similarly to *su*, we assume that zero value of *hold* can be used for all voltage values. As for the setup time constraints, we use growth factors in Equations (20) and (21). The terms e_i, f_i and j_i, are the MGFs, while the terms g_i, h_i, and l_i are SGFs. These equations (Equations 20 and 21) ensure the logic delay is not so fast that signals overlap improperly, causing race-through.

The setup time constraints have a small probability of failure despite compliance with the hold time constraints. The previous comment about the difference between statistical and STA also applies here.

4.1.4 | Timing Yield

Given a specific voltage value V_i, let's consider the setup margin MS_i as a random variable given by:

$$\mathrm{MS}_i \sim N\left(\mu_{\mathrm{MS}_i}, \sigma_{\mathrm{MS}_i}\right), \tag{22}$$

where μ_{MS_i} and σ_{MS_i} are the mean and standard deviation of the normally distributed random variable MS_i.

To find the probability that the random variable MS_i is greater than zero, the PDF of MS_i is denoted as $P(\mathrm{MS}_i)$. If $P(\mathrm{MS}_i) > 0$, the circuit satisfies the statistical setup constraint. Thus, the timing yield for a setup margin is the probability that $P(\mathrm{MS}_i) > 0$:

$$Y_{\mathrm{MS}_i} = P\left(\mathrm{MS}_i > 0\right), \tag{23}$$

$$Y_{\mathrm{MS}_i} = \left[1 - P\left(\mathrm{MS}_i < 0\right)\right], \tag{24}$$

$$P(\mathrm{MS}_i < 0) = \frac{1}{2}\left(1 + \mathrm{erf}\left(\frac{-\mu_{\mathrm{MS}_i}}{\sqrt{2}\,\sigma_{\mathrm{MS}_i}}\right)\right), \tag{25}$$

where $P(\mathrm{MS}_i < 0)$ is the well-known cumulative distribution function (CDF) [48] of the normal distribution of MS_i.

$$Y_{\mathrm{MS}_i} = 1 - \frac{1}{2}\left(1 + \mathrm{erf}\left(\frac{-\mu_{\mathrm{MS}_i}}{\sqrt{2}\,\sigma_{\mathrm{MS}_i}}\right)\right). \tag{26}$$

The development of the timing performance expression for a hold margin, $Y_{\mathrm{MH}_i} = P(\mathrm{MH}_i > 0)$, is similar to that previously described for the setup margin. Thus, Y_{MH_i} becomes:

$$Y_{\mathrm{MH}_i} = 1 - \frac{1}{2}\left(1 + \mathrm{erf}\left(\frac{-\mu_{\mathrm{MH}_i}}{\sqrt{2}\,\sigma_{\mathrm{MH}_i}}\right)\right). \tag{27}$$

We want both MS_i and MH_i of the circuit to be greater than zero (with a very high probability). To obtain the combined performance for MH_i and MS_i, we assume that MH_i and MS_i are independent. The combined statistical timing performance is thus given by:

$$Y(\mathrm{MS}_i, \mathrm{MH}_i) = Y_{\mathrm{MS}_i}\, Y_{\mathrm{MH}_i}. \tag{28}$$

The goal is to ensure that both MS_i and MH_i are greater than zero, which ensures reliable circuit operation within desired timing constraints. The combined performance is calculated as the product of their individual probabilities. This product gives a single value representing the circuit's overall performance, with higher values indicating a greater likelihood of meeting the required conditions for both metrics. This method provides a simple yet effective way to evaluate the circuit's statistical timing performance.

5 | Results From Our Proposed Model and MC Simulations

This section presents and discusses the results collected from our proposed model and simulations of the chosen benchmark circuits (Figures 3 and 4). All transistor-level simulations used in this work are based on a 90 nm BSIM4-based standard-cell library. This technology choice is not a limitation of the proposed

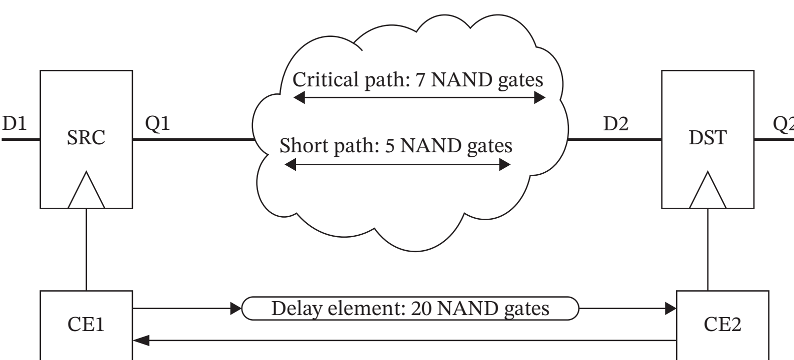

FIGURE 3 | Click-element benchmark circuit.

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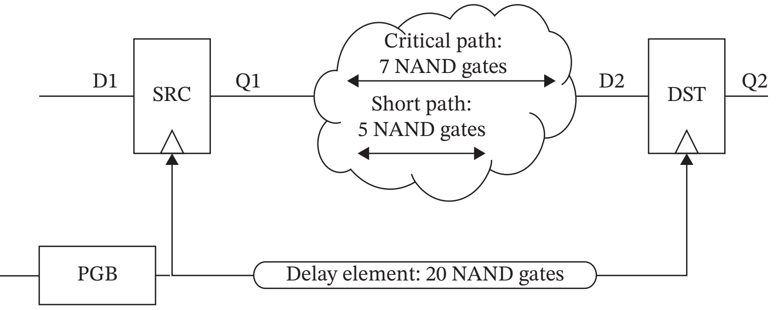

FIGURE 4 | SRBDHF benchmark circuit.

framework, but a deliberate selection motivated by three factors: (i) it is publicly documented, (ii) it enables reproducible experiments by other researchers, and (iii) it is representative of industrial design styles used in asynchronous circuits. Academic and predictive BSIM3/BSIM4 libraries around 90 and 65 nm are widely adopted in SSTA and variability research for exactly these reasons [49, 50]. Porting the methodology to more advanced nodes such as 28 or 16 nm requires only a re-characterization of the process parameters and delay statistics, as in conventional SSTA flows. While multi-node, silicon-proven validation would be desirable, it remains outside the scope of this paper due to the lack of open, publishable PDKs at several technology nodes.

All statistical analyses reported in Section 5 are performed at pre-layout (schematic) level using HSPICE and a characterized 90 nm CMOS BSIM4-based standard-cell library at nominal $V_{\text{DD}} = 1.1$ V. We use the foundry SVT BSIM4 transistor models provided by the 90 nm PDK. The nominal device-level threshold voltages (V_{thn}, V_{thp}) and their corner offsets, as listed in the mos_bsim4_svt.lib files, are used to set the means and variances of the corresponding process parameters in Table 2. The nominal V_{DD} value is 1.1 V. Several temperature values of 0°C, 25°C and 85°C are used to evaluate statistical constraints as a function of temperature variations. For DVS, the supply voltage values vary between 1.1 and 0.7 V. In all benchmarks, delay lines are implemented as homogeneous chains of NAND gates with identical drive strength. This choice mirrors the industrial SRBDHF and Click-style implementations we target, in which delay elements are typically built from identical standard-cell primitives. In our broader work [51], we have also characterized inverter, AND, OR, and NOR chains under DVS, and observed that NAND and AND gates exhibit similar delay-growth behavior, while OR and NOR are slightly less sensitive. Using NAND gates therefore provides a representative case for DVS sensitivity. All simulations were conducted using Hspice, based on a standard cell library implemented with the BSIM4 model of the adopted 90 nm CMOS process technology [52].

- SRBDHF benchmark: A single-stage SRBDHF pipeline in which source and destination registers are modeled as standard D flip-flops from the library. The combinational logic cloud contains two instruction paths (a short path of 5 NAND2 gates and a long path of 7 NAND2 gates). The control delay line is implemented as a homogeneous chain of 20 NAND2 gates with fan-out-of-one loading, driven by a pulse generator block.
- Click benchmark: A Click pipeline built around the same logic cloud and delay-line structure (20 NAND2 gates) as the SRBDHF case. Two Click elements, implemented at gate level using standard-cell primitives as in Figure 3, generate local clocks *f*1 and *f*2 and implement the request/acknowledge handshake between stages.
- Large-scale benchmark: A larger bundled-data pipeline including a pulse generator with a chain of 200 inverters and one XOR gate, a logic block with two potential critical paths (20 OR + 30 AND gates, and 17 OR + 50 AND gates) and one shorter path (30 NAND gates), and a delay element composed of 41 AND gates and 26 OR gates.

TABLE 2 | Specifications of process variations.

Parameter	V_{thn} (V)	V_{thp} (V)	L (nm)
Nominal (μ)	0.2715	−0.188	90
Variation (σ)	0.02715	0.0188	9

In the reported benchmarks, the delay lines are implemented as homogeneous chains of NAND gates. As mentioned before, this choice reflects the implementation style of industrial SRBDHF and Click-based pipelines, where NAND is a widely used standard-cell primitive for both logic and control. In our broader work [51], other gate types and delay-line architectures (e.g., inverter chains and mixed-gate topologies) have also been analyzed and exhibit similar qualitative DVS trends. In our model, we assume that the correlation coefficients and the elements of the covariance matrices are equal to zero.

5.1 | Our Model Versus MC Simulations

To verify the results of our statistical approach, we used a 1000-iteration MC simulation as a reference for comparison. In Tables 3 and 4, we report the relative errors expressed as the ratio between the absolute difference between the value obtained by an MC simulation and those computed with our model over the MC value as a function of V_{DD} for the SRBDHF and Click circuit, respectively, when the temperature is set to 25°C. For each delay measurement, the mean and the standard deviation of the differences observed between the delays predicted by MC and the proposed method are reported.

Tables 3 and 4 present the relative error (in %) for the mean and standard deviation of various propagation delays (Dclmin, Dclmax, *T*1, De) as a function of supply voltage between MC simulation and the proposed method in this model for the Click and SRBDHF circuits, respectively. In Table 3, for example, the relative error in the mean of the Dclmin delay is 1.3% and 2.79%

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TABLE 3 | Relative errors of mean and standard deviation of delays in (%) between MC and the proposed model (PM) for the click circuit; error = |PM −MC|/MC.

Voltage	Dclmin		Dclmax		$T1$	
	μ	σ	μ	σ	μ	σ
1.1	1.30	18.2	0.93	22.3	1.00	33.3
1.0	1.65	24.3	1.15	27.6	1.65	37.6
0.9	1.94	32.4	1.45	38.2	1.98	44.7
0.8	2.13	48.2	2.18	50.9	2.43	55.9
0.7	2.79	53.1	2.83	58.1	2.99	62.1

for a supply voltage of 1.1 and 0.7 V, respectively. Similarly, the relative error in the standard deviation of the Dclmin delay is 18.2% and 53.1% for a supply voltage of 1.1 and 0.7 V, respectively. Likewise, in Table 4, the relative error in the mean of the De delay is 1.55% and 3.17% for a supply voltage of 1.1 and 0.7 V, respectively. In comparison, the relative error in the standard deviation of the De delay is 28.3% and 58.5% for a supply voltage of 1.1 and 0.7 V, respectively. It can be observed that as the supply voltage decreases, the error in both mean and standard deviation tends to increase.

The results of the proposed model for mean delay values are close to the MC results, with errors ranging between 1% and 3.17% for both types of asynchronous circuits. As we approach the subthreshold region, additional parameters may be included for better accuracy in delay estimation.

On the other hand, the relative error in standard deviation varies from 18% to 62.1%. Note that all error values for the metrics compared between the model and MC simulations are negative if absolute value is not considered. This can be explained by the absence of the correlation coefficient term in the proposed model. As in [53], where the relative error in standard deviation varies from 18% to 51.3% (in absolute values), we attribute this error to the assumption of zero correlation coefficients, given that there is a correlation in the statistical definition of the V_{th} and L parameters in the MC simulation library files on Hspice BSIM4. Accounting for correlation to enhance accuracy is part of our future work.

To analyze the impact of the standard deviation error shown in Tables 3 and 4, we look at how these standard deviation errors affect the μ/σ values of the Click and SRBDHF circuits, used in Equations (26)–(28) to verify if the target statistical timing yield constraint can be reached. The outcomes presented in Figures 5 and 6 are derived through two distinct calculation approaches: one relying on the Hspice simulator and the other utilizing the model established within the context of this paper. Figures 5 and 6 present the μ/σ of the two statistical timing constraints related to setup and hold margins. The ratio obtained from the Hspice simulator, for example, for setup margin constraint varies from 17.44 for a supply voltage of 1.1 V to 10.02 for a supply voltage of 0.7 V for the Click circuit and from 10.73 for a supply voltage of 1.1 V to 7 for a supply voltage of 0.7 V for the SRBDHF circuit. Similarly, the μ/σ ratio obtained by the proposed model for setup constraint varies from 29.98 for a supply voltage of 1.1 V to 31.87 for a supply voltage of 0.7 V for the Click circuit and from 17.27 for a supply voltage of 1.1 V to 18.29 for a supply voltage of 0.7 V for the SRBDHF circuit. The μ/σ ratio obtained in Hspice simulations tends to decrease slightly with decreasing supply voltage for both Click and SRBDHF circuits. On the other hand, the μ/σ ratio obtained by the proposed model tends to increase slightly with decreasing supply voltage for both types of circuits. It is also noticeable that the μ/σ ratio values predicted by the proposed model are higher than those calculated by Hspice simulations.

TABLE 4 | Relative error of the mean and standard deviation of delays in (%) between MC and the proposed model for the SRBDHF circuit; error = |PM−MC|/MC.

Voltage	Dclmin		Dclmax		De	
	μ	σ	μ	σ	μ	σ
1.1	1.12	16.2	1.15	20.3	1.55	28.3
1.0	1.44	26.3	1.74	29.6	1.74	33.6
0.9	1.67	30.4	1.88	33.2	1.98	39.7
0.8	2.13	46.2	2.43	50.9	2.63	52.6
0.7	2.45	50.2	2.86	55.1	3.17	58.5

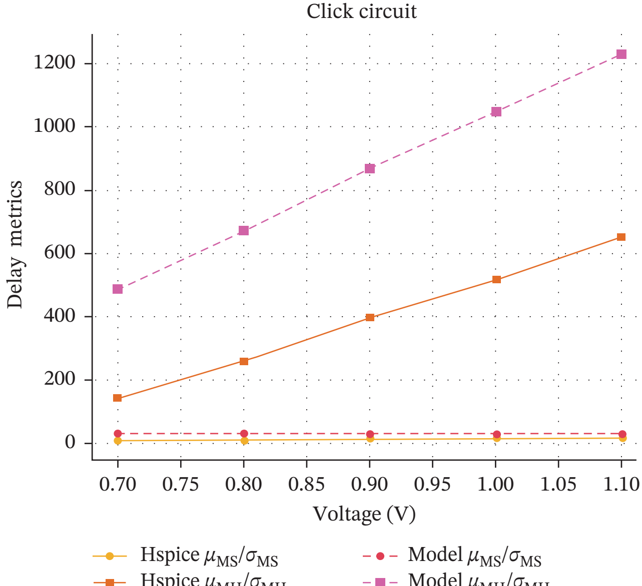

FIGURE 5 | Comparison of μ/σ ratio for setup and hold margins estimated by Hspice measurements and proposed model for the Click circuit.

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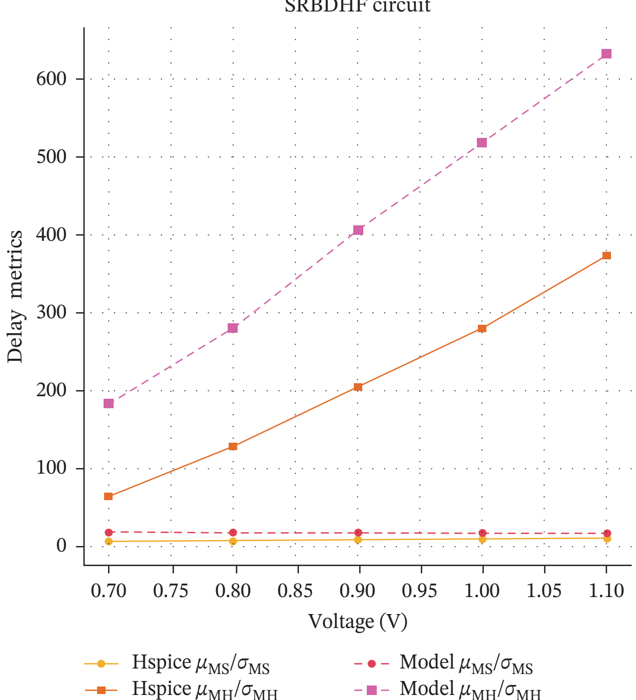

FIGURE 6 | Comparison of μ/σ ratio for setup and hold margins estimated by Hspice measurements and proposed model for SRBDHF circuit.

The model calculates lower values for σ_{MS}, σ_{MH} compared to those obtained by Hspice, primarily due to the omission of the correlation term in Equation (5).

Even with the error percentage ranging from 18% to 62.1% for sigma values, it results in only an additional 1.12e–12 yield loss (using Equations (26) and (27)) for our model, considering the lower value of μ/σ from Figures 5 and 6, which presents the setup constraint for the ratio μ_{MS}/σ_{MS} for the SRBDHF circuit at a voltage of 0.7 V. Thus, we conclude that the standard deviation error between the model and MC simulations does not significantly impact the statistical timing yield constraint. In this specific study, it is noted that the timing constraint is satisfied both by the model and by Hspice simulations.

Another aspect to consider is our model's run time concerning MC simulations. The previous circuit was analyzed for all statistical constraints proposed in 25.6 h with MC simulations, while our model takes only 3 s when executed on an Intel Core i7 machine.

5.2 | Impact of Voltage, Temperature, and Process Variations

Next, we assess the impact of voltage, temperature, and fabrication process variations on the pulse propagation in the SRBDHF circuit. Using Equation (11), we examine the statistical parameters for different operating voltages. The parameter "*param1*" represents the measure of pulse width derived from PW − $3\sigma_{DIFF}$, while "*param2*" represents the measure of Nb $|diff| +$ $3\sigma_{PW}$. Note that *param1* and *param2*, are both timing margins expressed in units of time and derived from the same STA-style pulse-width constraint in Equation (11). The term *param1* corresponds to the available input-pulse margin when the nominal pulse width PW is reduced by the variability term $3\sigma_{DIFF}$, whereas *param2* corresponds to the worst-case accumulated pulse broadening (or shrinking) along the delay line, including its variability term $3\sigma_{PW}$. Comparing *param1* and *param2* therefore does not mix pulse width and slew; it compares two margins extracted from the same timing inequality, one at the input of the line and one at its output. Table 5 presents the effect of process variation and voltage on the width of the pulse injected into the delay line (composed of 20 NAND gates) of the SRBDHF circuit at a temperature of 25°C, while Table 6 illustrates the effect of temperature variation on this type of circuit. All the measurements in Tables 5 and 6 were carried out using the HSPICE tool.

Table 5 shows that the mean pulse width μ_{PW} increases as V_{DD} decreases (for example, from 1.36 ns at 1.1 V to 3.21 ns at 0.7 V).

TABLE 6 | Evaluation of statistical logic constraint for SRBDHF circuit at different temperature values under voltage variation (ns), using Hspice simulations.

	"param1-param2"		
Voltage	**0°C**	**25°C**	**85°C**
1.1	1.08	1.21	1.24
1.0	1.25	1.40	1.42
0.9	1.52	1.70	1.76
0.8	1.96	2.16	2.22
0.7	2.49	2.90	3.54

TABLE 5 | Evolution of statistical logic performance for SRBDHF circuit under voltage variation.

	PW		diff			
Voltage	μ_{PW} **(ns)**	σ_{PW} **(ps)**	μ_{diff} **(ps)**	σ_{diff} **(ps)**	**param1 (ns)**	**param2 (ns)**
1.1	1.36	3.05	5.07	0.69	1.32	0.111
1.0	1.57	4.40	5.03	0.89	1.52	0.114
0.9	1.89	5.84	4.88	1.24	1.82	0.115
0.8	2.39	9.05	4.67	1.80	2.28	0.121
0.7	3.21	12.9	4.42	3.00	3.03	0.127

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In our analysis, μ_{PW} is computed only over pulses that generate two valid logic transitions at the end of the delay line, that is, two 50% V_{DD} crossings (one rising and one falling); pulses that fail to produce these two transitions at low supply voltage are classified as lost pulses and are excluded from the statistics. The PDK model decks used in this work provide transistor-level BSIM4 parameters but no standard-cell timing views and therefore no explicit max_transition constraint at the cell-library level. We consequently do not enforce a numerical max_transition limit in our analysis. Instead, we classify pulses as valid only if they produce two complete logic transitions at the end of the delay line (two 50% V_{DD} crossings, one rising and one falling). Pulses that become too slow or too small to switch the output are treated as lost and excluded from the computation of μ_{PW}. This lost-pulse region plays the role of a practical max-transition or minimum-amplitude constraint on the propagated pulses. As V_{DD} is reduced towards the near-threshold region, both the rising and falling propagation delays of a gate increase, but not at the same rate. In our 90 nm library the PMOS-limited transition (typically the rising edge) degrades faster, so the difference $|t_{pLH} - t_{pHL}|$ becomes larger at low supply voltages. In a homogeneous delay line, this asymmetric delay is applied stage after stage to the rising and falling edges, so the small per-stage mismatch accumulates along the chain and modifies the interval between the edges. When the rising edge is slower, the pulse widens progressively from one stage to the next; when the falling edge is slower, it shrinks. In our measurements, μ_{PW} is computed only for pulses that still produce two valid 50% V_{DD} transitions at the output of the delay line, while pulses that fail to switch are classified as lost and excluded from the statistics. Under these conditions, the cumulative effect of the increasing rise–fall delay asymmetry explains why the mean pulse width measured at the end of the delay line increases as V_{DD} decreases, up to the point where pulses become too degraded to switch and are counted as lost [10]. It can also be observed from Table 5 that *param1* varies between 1.32 and 3.03 ns for voltages of 1.1 and 0.7 V, respectively, and *param2* varies between 0.111 ns and 0.127 for voltages of 1.1 and 0.7 V, respectively. Both *param1* and *param2* values increase with decreasing supply voltage. Additionally, the gap between *param1* and *param2* measurements increases with decreasing voltage. Consequently, param1 is consistently greater than param2 in the SRBDHF circuit in this case study example.

It is worth noting that with other SRBDHF circuit architecture configurations, where the pulse width is not sufficiently large or has shrunk due to variations in supply voltage, a decrease in pulse width with decreasing supply voltage may be observed. Since σ_{diff} and σ_{PW} tend to increase with decreasing supply voltage, the "param1" measurement may decrease on one side, while the "param2" measurement may increase with the sum $Nb|diff| + 3\sigma_{PW}$ This could impact the correct propagation through the delay line, potentially leading to an unreliable circuit at low voltage. Hence, the proposed model becomes relevant, allowing verification of the viability of a potential SRBDHF circuit configuration with DVS.

Considering different temperature conditions, we assessed the statistical logic constraint in different temperature scenarios, 0°C and 85°C using two analysis methods: deterministic STA and statistical SSTA. We recorded the evolution of "param1-param2" to determine if this measure is still positive regardless of temperature variations and conforms to the condition defined in Equation (11).

According to Table 6, the measure "param1-param2" is consistently positive for temperatures of 85 and 0°C. It varies from 1.08 ns for 1.1 V to 2.49 ns for 0.7 V for the temperature value 0°C and from 1.24 ns for 1.1 V to 3.54 ns for 0.7 V for the temperature value 85°C.

The value "param1-param2" satisfies the condition specified in Equation (11) for all studied temperature conditions. Therefore, we can conclude that the statistical logic constraint is validated.

To illustrate the effect of temperature on the statistical timing constraints for both types of circuits, the ratio μ/σ is calculated for two distinct temperatures, 0°C and 85°C, for both setup and hold margins. This ratio is then used to calculate yield losses. Results are presented in Table 7. From Table 7, we observe that the ratio obtained for temperature 0°C for setup margin constraint, for example, varies from 19.23 for a supply voltage of 1.1 V to 11.6 for a supply voltage of 0.7 V for the Click circuit. At 85°C the ratio μ/σ varies from 9.67 for a supply voltage of 1.1 V to 6.98 for a supply voltage of 0.7 V for the SRBDHF circuit.

Examining Table 7 reveals that temperature influences the timing statistical constraints for both circuits, namely the Click and the SRBDHF circuit. Specifically, the values of the ratio μ/σ increase as the temperature decreases, transitioning from 85°C to 0°C.

Considering the variations in manufacturing processes and supply voltage from Figures 5 and 6, along with the temperature variation from Table 7, the condition representing the smallest value μ/σ occurs at 85°C for 0.7 V for the setup constraint margin for the SRBDHF circuit, resulting in a yield loss of only 1.3e–12.

These findings underscore the importance of considering both temperature and supply voltage in the design of these circuits. Understanding how these parameters influence performance is

TABLE 7 | Comparison of μ/σ ratio estimated by Hspice measurements for the click and SRBDHF circuits under temperature variation.

Click circuit Voltage	**0°C**		**85°C**	
	$\frac{\mu_{MS}}{\sigma_{MS}}$	$\frac{\mu_{MH}}{\sigma_{MH}}$	$\frac{\mu_{MS}}{\sigma_{MS}}$	$\frac{\mu_{MH}}{\sigma_{MH}}$
1.1	19.23	1240.0	12.55	241.77
1.0	17.34	1006.6	14.45	231.25
0.9	15.61	467.32	13.78	222.24
0.8	13.30	340.76	11.88	172.31
0.7	11.60	227.54	9.87	127.82
SRBDHF circuit Voltage	**0°C**		**85°C**	
	$\frac{\mu_{MS}}{\sigma_{MS}}$	$\frac{\mu_{MH}}{\sigma_{MH}}$	$\frac{\mu_{MS}}{\sigma_{MS}}$	$\frac{\mu_{MH}}{\sigma_{MH}}$
1.1	19.88	637.73	9.67	355.43
1.0	19.15	389.69	9.34	167.87
0.9	18.13	296.46	8.73	145.82
0.8	13.60	147.13	7.05	102.58
0.7	12.47	69.31	6.98	61.11

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crucial for maintaining the constraints of these circuits verified under variable conditions.

5.3 | Statistical Versus Deterministic STA

To illustrate the importance of the statistical approach when assessing the performance of asynchronous circuits, we analyzed timing margins for Click and SRBDHF circuits using two analysis methods: deterministic and statistical. The deterministic analysis relies on the worst-case scenario, evaluating circuit performance by assuming that all the most unfavorable conditions in terms of process delays, temperature, and voltage occur simultaneously. This approach aims to ensure the proper operation of the circuit under the most critical conditions, thus ensuring its functionality in all real-world situations.

In this section, we find that MS (setup margin) is always smaller than MH (hold margin). In Table 8, we therefore present only MS to avoid cluttering the table with excessive values; the same conclusions hold for the two margins. Table 8 presents the setup constraint timing margins required for both circuits, Click and SRBDHF, to ensure correct circuit functionality. The necessary timing margins are calculated for two scenarios: the first uses STA to compute the worst-case setup margin (WCMS). In contrast, the second uses the statistical approach proposed in our model to calculate the statistical setup margin (SMS). Note that the worst-case scenario selected here due to the asynchronous nature of the circuit is (FF corner, 85°C) for 1.1, 1, and 0.9 V voltages, and (FF corner, 0°C) for 0.8 and 0.7 V. The PVT corners used for the SRBDHF and Click benchmarks are chosen to reflect the specific nature of bundled-data asynchronous pipelines. The FF/85°C and FF/0°C corners are selected empirically because they produce the tightest margins on the handshake and pulse-based timing constraints over the considered voltage range, not to emulate the split worst-case/best-case combinations adopted in synchronous sign-off flows. Our goal is thus to identify the operating conditions that most strongly stress the asynchronous timing constraints within a single-corner setting, rather than to reproduce a multi-corner synchronous STA methodology. Note that in our 90 nm study we do not observe a full temperature-inversion phenomenon of the type reported for some sub-65 nm technologies. Instead, under deep voltage-scaling conditions (around V_{DD} ≈0.7 V), we observe a temperature-reversal effect: the reduction in threshold voltage with temperature partially compensates for mobility degradation, so the delay-versus-temperature dependance is reduced and can even exhibit a slight reversal in this operating region [10]. Finally, in all reported results, the critical logic paths and their matched delay lines are always analyzed under the same PVT corner; we do not mix different worst-case and best-case corners between logic and control paths.

TABLE 8 | Worst case vs statistical setup margins comparison.

	Click circuit		SRBDHF circuit	
Voltage	WCMS	SMS	WCMS	SMS
1.1	2.74E−10	3.22E−10	1.17E−10	1.27E−10
1.0	3.11E−10	3.75E−10	1.33E−10	1.49E−10
0.9	3.64E−10	4.50E−10	1.57E−10	1.82E−10
0.8	4.47E−10	5.71E−10	1.93E−10	2.31E−10
0.7	5.70E−10	7.91E−10	2.50E−10	3.26E−10

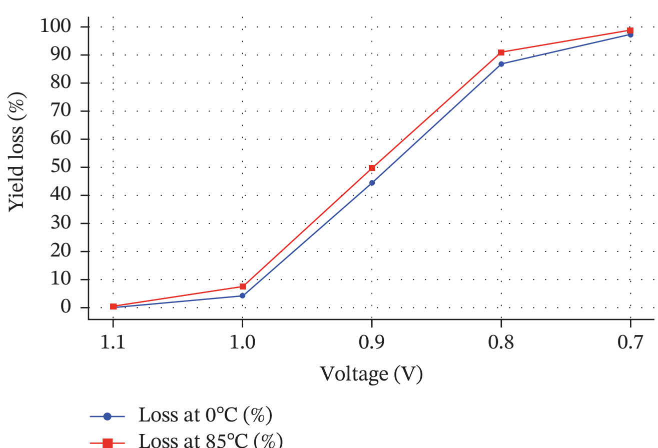

FIGURE 7 | Yield loss (%) as a function of voltage, process, and temperature variation.

According to Table 8, SMS varies from 3.22E−10 to 7.91E−10 for the 1.1 and 0.7 V, respectively, for the Click circuit, while it varies and ranges from 1.27E−10 to 3.26E−10 for the 1.1 and 0.7 V, respectively, for the SRBDHF circuit.

When comparing the statistical values of MS margin obtained in Table 8 with the worst-case values of MS margin for both circuits, for example, in the SRBDHF circuit for 0.8V operating voltage, the case MS value is 1.93E−10, and the statistical MS value is 2.31E−10. Noticeably, the margins observed in the deterministic analysis are smaller than those obtained for the statistical analysis. This holds for asynchronous Click and SRBDHF circuits and all voltage values. This implies that the deterministic approach tends to be conservative and pessimistic, requiring an extension of delay lines to meet the timing constraint and subsequently reducing circuit performance. Thus, it confirms that using the statistical approach for synchronization constraint analysis can avoid the introduction of pessimistic margins, as is commonly observed [54].

The STA approach is highly conservative by design, assuming worst-case scenarios to ensure reliability in all situations. However, this inherent conservatism introduces significant pessimism, often resulting in overly restrictive designs and compromised performance. In contrast, based on SSTA, the proposed method provides probabilistic estimates of timing variations, thereby avoiding overly pessimistic margins and enabling performance gains by focusing on more realistic scenarios.

A key question is whether the proposed method can achieve the same level of reliability as STA under the most pessimistic conditions. Theoretically, SSTA models variations in PVT statistically, providing predictions with a confidence-bound interval, such as $\pm 3\sigma$. This implies that while SSTA does not guarantee absolute worst-case coverage like STA, it accounts for realistic tail-end scenarios with extremely low failure probabilities. By selecting an appropriate confidence interval (e.g., 3σ or higher), SSTA achieves a balance between reliability and performance, ensuring that the circuit functions correctly under almost all practical conditions.

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It is important to note that in SSTA, there is a small probability that the timing constraints will not be met. This small percentage of failure is variable, and as the sigma (σ) value increases, the likelihood of such failures decreases significantly.

Therefore, the proposed method remains a secure and reliable alternative to STA. It significantly reduces unnecessary pessimism while ensuring a very low failure probability, thereby maintaining reliability in practical applications.

5.4 | Large Scale Example

In the previous example, we demonstrated the validation of the proposed approach by using a reference circuit, as shown in Figures 3 and 4. This example focused on a simple circuit with a limited number of logic gates. It is motivated by the fact that the operation of high-performance circuits is determined by their critical paths that, once sensitized, closely resemble chains of passing gates, and designers optimize them by minimizing the number of gates they comprise, making such a configuration representative of real-world scenarios in high-performance circuits.

In this section, we opted to incorporate a more diverse combination of logic gates to evaluate the impact of this variety on circuit performance, particularly under the influence of voltage, temperature, and manufacturing process variations.

The graph in Figure 7 illustrates the impact of voltage and temperature variations on circuit performance yield loss of the SRBDHF circuit, considering the statistical timing constraints with the configuration described above. The parameters $\frac{\mu_{MS}}{\sigma_{MS}}$ and $\frac{\mu_{MH}}{\sigma_{MH}}$ were used to calculate Y_{MS} and Y_{MH}, representing the probabilities that the circuits meet statistical setup and hold timing constraints. Yield loss was calculated using: $\text{Yield loss}\,(\%) = (1 - (Y_{MS}\,Y_{MH})) \times 100$, expressing the percentage of circuits that fail to meet these constraints under varying conditions.

At higher voltages, such as 1.1 V, the yield loss is negligible (e.g., 0.01% at 0°C and 0.07% at 85°C), indicating operation with sufficient timing margins. However, as the voltage decreases, the yield loss increases significantly. For instance, at 0.9 V, the yield loss reaches 44.28% at 0°C and 49.39% at 85°C, highlighting the difficulties in maintaining timing constraints at lower supply voltages. Temperature further amplifies this effect; for example, at 1.0 V, the yield loss increases from 3.75% at 0°C to 7.18% at 85°C, demonstrating the adverse impact of thermal variations on circuit reliability.

Timing margins also exhibit critical trends. The $\frac{\mu_{MS}}{\sigma_{MS}}$ values decline markedly as voltage decreases, turning negative at 0.8 and 0.7 V, indicating violations of setup timing constraints. Similarly, $\frac{\mu_{MH}}{\sigma_{MH}}$ values decrease but remain positive. At critical voltage levels like 0.8 and 0.7 V, the yield loss becomes greater, reaching 86.76% at 0.8 V and 97.23% at 0.7 V at 0°C, revealing circuits are no longer reliable.

Figure 7 underscores the trade-offs between reducing supply voltage for energy efficiency and maintaining circuit reliability under varying temperatures. While lower voltages reduce power consumption, they result in significant timing margin violations and increased yield loss, especially at elevated temperatures. Circuit designers must carefully balance these factors to ensure reliable performance under real-world conditions, which the developed model needs to verify.

To address the timing constraint violations caused by voltage, temperature, and process parameter variations, the configuration was adjusted by adding additional logic gates to the delay line. The delay line now consists of 41 AND gates and 26 OR gates.

According to the results in Table 9, the $\frac{\mu_{MS}}{\sigma_{MS}}$ values for the setup constraint became positive for all supply voltages, even under extreme temperatures of 0°C and 85°C. At 0°C, these values range from 12.27 at 1.1 V to 1.20 at 0.7 V, while at 85°C, they range from 11.96 at 1.1 V to 2.04 at 0.7 V. The performance yield loss is very small for the supply voltage values from 1.1 to 0.8 V, demonstrating that the new configuration performs effectively under this specific voltage range. It also reveals that one single delay line might not be sufficient to meet the specifications and that a configurable (variable) delay line would be required to get lower yield loss at 0.7 V. Back to Figure 1, it means that the variable delay line should be adjusted not only for the operation performed but also at which supply voltage it is performed.

From this example, it can be concluded that configuring critical paths, short paths, and delay elements is crucial in meeting statistical timing constraints. These constraints are essential to ensure whether the circuit will function as intended. The results also highlight the significant impact of DVS, combined with variations in temperature and fabrication processes, on the overall performance of the SRBDHF circuit.

5.5 | Our Model Versus Literature

Table 10 compares our proposed method with several works in the literature in terms of average error on mean delay values. Our

TABLE 9 | Impact of voltage, process, and temperature variation on yield loss.

	0°C			85°C		
Voltage	$\frac{\mu_{MS}}{\sigma_{MS}}$	$\frac{\mu_{MH}}{\sigma_{MH}}$	**Yield loss (%)**	$\frac{\mu_{MS}}{\sigma_{MS}}$	$\frac{\mu_{MH}}{\sigma_{MH}}$	**Yield loss (%)**
1.1	12.27	1487.17	0	11.96	1374.55	0
1	8.38	1064.23	0	8.36	1038.78	0
0.9	5.51	696.97	0	6.01	709.98	0
0.8	3.03	408.51	0.11	3.9	441.12	0.004
0.7	1.2	194.89	11.32	2.04	239.06	2.02

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TABLE 10 | Comparison of our proposed method with the literature.

Metric	[27]	[29]	[30]	[28]	[33]	[34]	Ours
Average error (%)	—	5	5	10	—	2.8	2

method achieves an average error of only 2% with respect to MC reference simulations, while the other works report average errors between 2.8% and 10% when available.

5.6 | Scalability to Advanced Technology Nodes

The proposed method is adaptable to advanced technology nodes (below 65 nm), as it already integrates critical effects such as DIBL, V_{th} roll-off, and subthreshold conduction through parameters like V_{th}, S, and E_{sat}. At shorter channel lengths, the threshold voltage V_{th} is updated using the equation: $V_{th} = V_{th0} - V_{DD} \exp(-a_{Vth}L)$ to account for DIBL and V_{th} roll-off effects, with V_{th0} as the long-channel threshold voltage and a_{Vth} the DIBL coefficient. Similarly, the subthreshold swing S is revised to: $S = S_0\,[1 + \exp(-a_S\,L)]$, capturing its dependency on L and enabling accurate modeling at smaller nodes, with S as the subthreshold swing parameter, S_0 the nominal subthreshold swing for long-channel devices, a_s the coefficient describing the effect of L on S [35]. The delay equation remains structurally unchanged, requiring only updates to V_{th} and S to reflect advanced node effects.

The model relies on parameters such as V_{DD}, L, V_{th}, S, and E_{sat}, ensuring adaptability across technology nodes. This scalability integrates short-channel effects seamlessly without altering the fundamental equation. Including DIBL and V_{th} roll-off into V_{th} enables accurate timing analysis even under severe short-channel effects. It should also be emphasized that all benchmarks considered in this paper are pre-layout, gate-level schematic netlists that are representative of the cell-dominated timing regime used in SRBDHF and Click controllers. Interconnect between stages is limited to short local routing and is represented by the load capacitances already included in the standard-cell models, so no post-layout RC extraction of long global wires is performed. Consequently, the statistical parameters capture variability dominated by the cells and their local wiring. Wire-dominated global paths and explicit statistical modeling of RC variations in long interconnects are outside the scope of this work and are left for future extensions of the framework.

6 | Conclusion

This paper presented a comprehensive analysis of statistical performance in bundled-data asynchronous circuits, focusing mainly on the SRBDHF and Click element-based pipelines. Our proposed model incorporates process variations and DVS, enabling a thorough evaluation of statistical constraints across different operating conditions. Based on a 90 nm CMOS process technology, the estimations revealed valuable insights into the circuit's behavior.

The verification of our model against MC simulations showed its efficacy in predicting mean delay values with an average error of about 2%. However, the standard deviation error ranged from 18% to 62.1%, underscoring the need for future work to account for correlation coefficients to improve accuracy. Nevertheless, despite the standard deviation errors, the statistical timing yield constraints were satisfactorily met.

Examining statistical logic and timing constraints across different temperatures and supply voltages highlighted the intricate interactions among these factors. The results emphasized the importance of considering temperature and voltage variations to maintain circuit constraints.

We showed that the proposed framework could save significant margins that are added to compensate for process variation in the static analysis approach. The impact of voltage scaling, temperature, and process variation was efficiently estimated, accounting for statistical logic and timing constraints. Finally, the model's runtime was only a few seconds, compared to MC simulations that lasted 25.6 h, further underscoring its practical value.

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Conflicts of Interest

The authors declare no conflicts of interest.

Data Availability Statement

Data will be available upon request.

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