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Wide Linear Range Voltage-Controlled Delay Unit for Time-Mode Signal Processing

Soheyl Ziabakhsh*, Ghyslain Gagnon* and Gordon W. Roberts†
*École de technologie supérieure, Université du Québec, Montreal, Canada
†Department of Electrical and Computer Engineering, McGill University, Montreal, Canada
soheyl.ziabakhsh@lacime.etsmtl.ca, ghyslain.gagnon@etsmtl.ca, gordon.roberts@mcgill.ca

***Abstract*—A voltage-controlled delay unit (VCDU) for low-voltage time-mode signal processing is presented in this paper. The proposed VCDU uses a signal conditioning circuit to achieve wider-range and higher linearity than state-of-the-art VCDUs. Circuit-level simulations in 0.18μm CMOS process show a linearity error of less than $\pm$ 0.2% for a 0.15 V to 1 V input range. The proposed VCDU consumes 315 μW from a 1.8 V supply at its maximum sampling frequency of 500 MHz. The proposed VCDU is validated in a first-order time-mode $\Delta\Sigma$ modulator application. Circuit-level simulation results of the $\Delta\Sigma$ modulator show a peak SNDR of 58 dB when clocked at 140 MHz with a 400 kHz bandwidth.**

I. Introduction

Analog and mixed-mode circuits based on a signal representation in the voltage or current domain suffer from many limitations as a consequence of CMOS finer scale geometries [1], [2]. Some of these limitations are namely: increased leakage current through the gate of transistors, reduced voltage swing, increased switching noise and increased power consumption [3]. Time-mode signal processing (TMSP), which relies on a time-mode representation of signal amplitudes, is a promising approach to mitigate these limitations [4]. For example, TMSP implementations of phase-locked loops [5], IIR filters [6] and built-in self-test circuits [7] were recently demonstrated.

One of the basic component of TMSP circuits is a voltage-controlled delay unit (VCDU), which converts input voltage signals into proportionally-delayed versions of a reference clock signal [4]. Signal processing can then be performed on these time-mode signals using either a synchronous or asynchronous approach to implement analog or mixed-signal circuits.

The linearity of VCDUs is important because it defines the dynamic range of the TMSP circuits that follow. Previously published VCDU designs exhibit a linear input range of 200 mV [8] to 400 mV [4]. This paper proposes a novel VCDU design which uses a signal conditioning circuit to extend the input voltage linear range. The proposed circuit works without any operational amplifier or comparator, which would increase chip area and power consumption.

This paper is organized as follows. In Section II, the design of the proposed VCDU is presented, including the novel signal conditioning circuit. Section III reports the circuit-level simulation results of the proposed VCDU. In Section IV, the behavior of the VCDU is validated in an example application of $\Delta\Sigma$ modulation. Concluding remarks are provided in Section V.

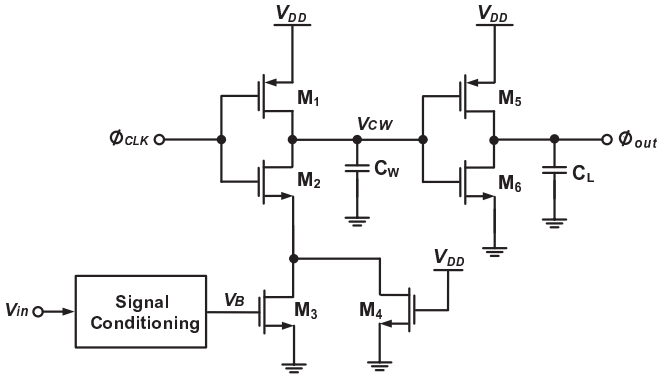

Fig. 1. Schematic of the proposed VCDU.

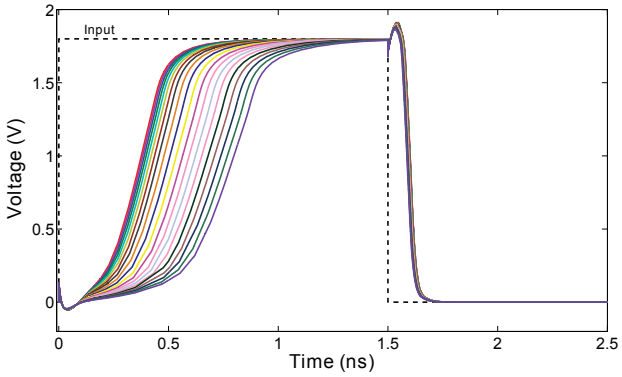

Fig. 2. Transient response of the proposed VCDU for various input voltages (circuit-level simulation results).

II. Proposed VCDU design

The proposed VCDU, which is based on the design in [4], is shown in Fig. 1. The circuit works by charging and discharging capacitor C_w, which is formed by the parasitic drain capacitors of M_1 and M_2 and the gate capacitors of M_5 and M_6. If the reference signal ϕ_{clk} is high, M_1 is turned off and the capacitor discharges from V_{DD} to zero through NMOS transistors M_{2-4}. During the discharging phase, when the voltage of capacitor C_w is less than the threshold of inverter transistors M_{5-6}, the output ϕ_{out} switches to high.

The discharging of the capacitor C_W begins on the rising edge of the reference signal ϕ_{clk} through transistors M_{2-4}.

The discharge rate of the capacitor is:

$$\frac{dV_{CW}}{dt} = \frac{-I_{D2}}{C_W} = \frac{-(I_{D3} + I_{D4})}{C_W} \quad (1)$$

where V_{CW} is the voltage across C_w, and I_{D3} and I_{D4} are the drain currents of M_3 and M_4, which are in triode in most of the input voltage range. When ϕ_{clk} is high, M_2 is ON and $V_{DS3} = V_{DS4} \simeq V_{CW}$. Therefore [9],

$$I_{D3} = \mu_n C_{ox} \frac{W_3}{L_3} \left((V_B - V_{tn}) V_{CW} - \frac{1}{2} V_{CW}^2 \right) \quad (2)$$

$$I_{D4} = \mu_n C_{ox} \frac{W_4}{L_4} \left((V_{DD} - V_{tn}) V_{CW} - \frac{1}{2} V_{CW}^2 \right) \quad (3)$$

where μ_n is the mobility of the carriers, C_{ox} is the gate oxide capacitance per unit area, W/L is the aspect ratio of the respective transistors and V_{tn} is the threshold voltage of NMOS transistors. Eq. (1) and (2) indicate how the voltage V_B changes the time constant of the discharging path and thus controls the delay of the output signal.

The time-difference interval between rising edges of ϕ_{clk} and ϕ_{out} is a representation of the input signal in the time domain. This time-difference is controlled by capacitor C_w, control voltage V_B, and transistors in the discharging path. This design is linear for an input voltage between 0.8 V to 1.2 V [4], the nonlinearity at lower input voltages being mainly caused by M_3 entering the subthreshold region.

In order to increase the linear input range of the VCDU, the signal conditioning circuit of Fig. 3 is proposed. This circuit improves the linearity range by two mechanisms. A DC offset is applied to the input voltage while the circuit has an exponential response in the midrange (from 0.5 V to 1.2 V). This is achieved by combining two voltage sources through transistors M_{12} and M_{13}. The DC offset is realized with the voltage divider formed by R_1 and R_2 and two NMOS transistors, M_{7-8}. The input voltage is increased through the diode-connected transistor M_8 and the gate-source of M_7. This DC offset ensures that M_3 is in saturation at low input voltages. Finally, the combination of transistors M_{9-11} with the DC offset generates the desired exponential response in the midrange.

The transfer characteristics of the signal conditioning block is shown in Fig. 4, including the effect of a $\pm$ 1% and $\pm$ 5% mismatch on the value of R_1. To our knowledge, this circuit is the first structure that applies transformations to the input signal to improve the linearity of TMSP circuits without using any operational amplifier.

III. Simulation Results

The Taillefer VCDU [4] and the proposed VCDU were designed and simulated using Spectre in a TSMC 0.18 μm CMOS process with a 1.8 V supply voltage. Fig. 5 shows that the linear range of the VCDU was effectively extended using the proposed signal conditioning circuit, and that the conversion gain was also improved. For both VCDUs, the output data was exported to MATLAB, and a linear regression was performed to evaluate the linearity error.

Since a typical application of TMSP circuits is analog-to-digital conversion, we define the linear range of the VCDU as

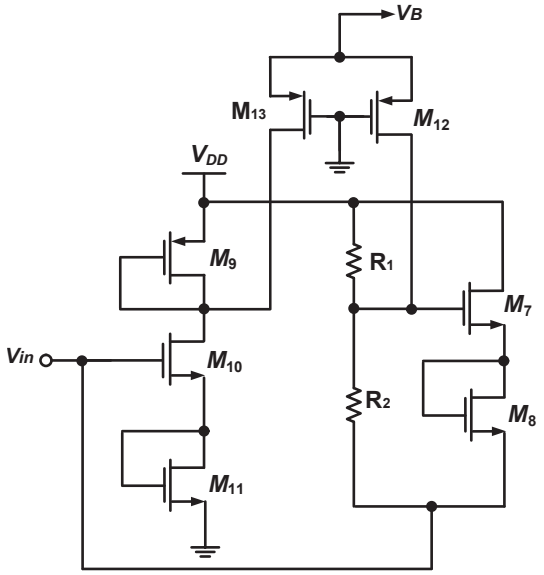

Fig. 3. Circuit diagram of the proposed signal conditioning block.

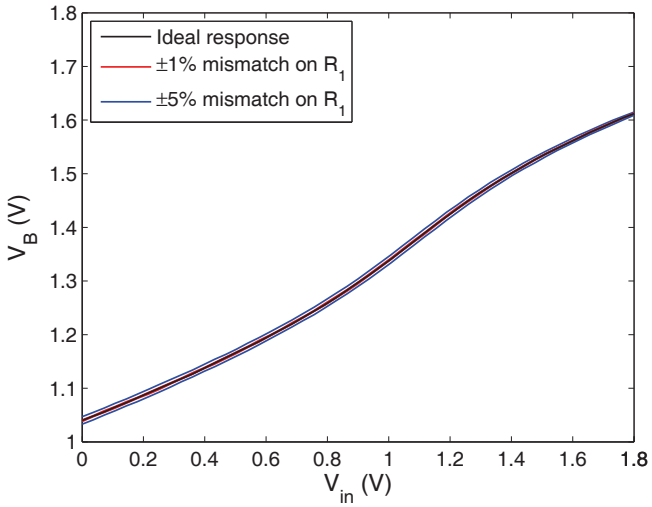

Fig. 4. DC response of the signal conditioning block.

the input range for which the linearity error is less than half the step of the least significant bit (LSB) for an 8-bit ADC. For this purpose, the following relative linearity error calculation is used:

$$\epsilon = \frac{E}{FS} * 100\% \quad (4)$$

where E is the largest deviation from the ideal (linear) behavior over the full scale linear range FS of input voltage. As shown in Fig. 6, the linear range which provides 8-bit resolution ($\pm$ 0.2%) for the proposed VCDU is from 0.15 V to 1 V, which is suitable for low-voltage TMSP.

One of the anticipated issue with the proposed signal conditioning circuit is the sensitivity to the ratio of the values of resistors R_1 and R_2. To evaluate this sensitivity, simulations were performed by forcing a 1% error on the value of R_1. Fig. 6 shows that the linearity error was not affected by this mismatch on R_1 and R_2, i.e. the linear range for 8-bit

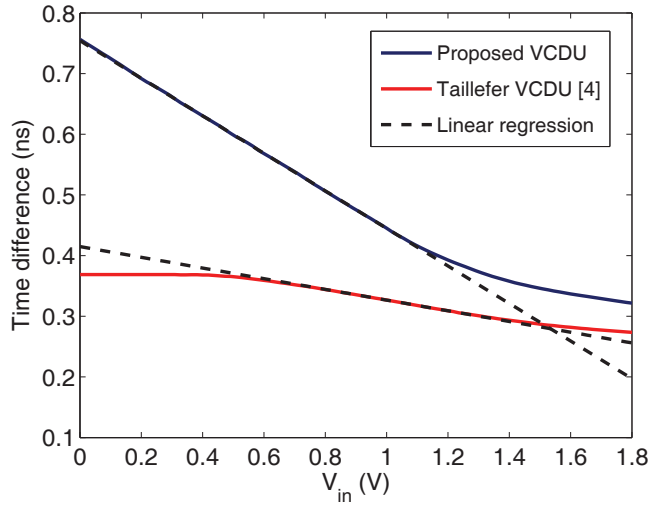

Fig. 5. Transfer characteristic of Taillefer VCDU and proposed VCDU.

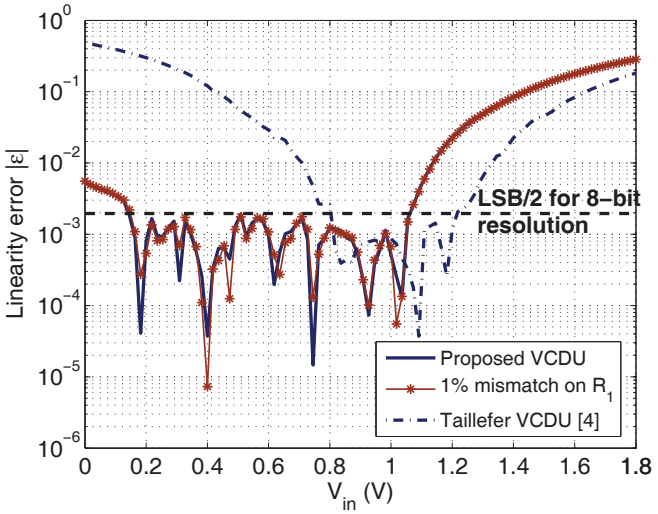

Fig. 6. Linearity error of Taillefer VCDU and proposed VCDU.

resolution is the same with the forced mismatch. Careful layout should ensure that the mismatch between R_1 and R_2 is kept below 1%.

The performances of the proposed architecture is summarized in Table I and compared with some reported VCDUs. In order to compare VCDU performances, we propose the following figure of merit (FOM):

$$FOM = \frac{P}{FS^2 \times f_s} \tag{5}$$

where P is power dissipation and f_s is the sampling frequency. The proposed FOM is in line with the commonly used FOM for ADCs [10]. Using this metric, the proposed VCDU achieves a FOM of 0.86 pJ/V^2.

IV. Application to $\Delta\Sigma$ Modulation

Wide-range linear VCDUs have many applications in TMSP such as $\Delta\Sigma$ modulators, time-to-digital converters and digital phase-locked loops. In this section, the simulation of a time-mode $\Delta\Sigma$ modulator using the proposed VCDU is performed to evaluate its performance for this application.

TABLE I. Performance summary and comparison.

	[4]	[8]	Proposed
Conversion gain G_ϕ	-92 ps/V	-250 ps/V	-311 ps/V
8-bit linear range FS	0.82 V - 1.2 V	-0.1 V - 0.1 V	0.15 V - 1 V
Max. sampling freq. f_s	1 GHz	7.5 GHz	500 MHz
Power consumption P	175 μW	4 mW	315 μW
FOM [pJ/V^2]	1.22	13.33	0.86

Simulation results are obtained at the maximum sampling frequency.

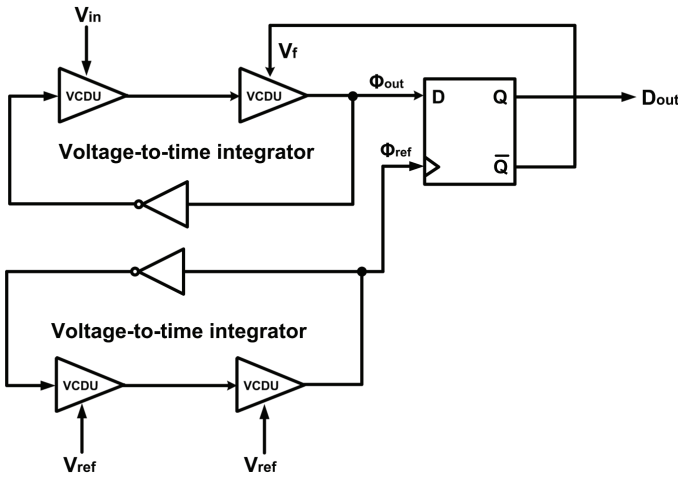

Fig. 7. First-order single-bit time-mode $\Delta\Sigma$ modulator [4].

The modulator introduced in [4] employs a VCDU in a time-mode ADC implementation with first-order noise shaping. The authors in [4] suspected that the VCDU linearity might be the limiting factor for the signal-to-noise and distortion ratio (SNDR) performances.

The modulator is realized by two voltage-controlled ring oscillators, a D flip-flop, and some digital inverters, as shown in Fig. 7. The top ring oscillator converts the input signal to a time-difference information and adds it to the inverse of the digital output. The frequency of the bottom voltage-to-time integrator (reference oscillator) is controlled by the reference voltage V_{ref} to provide the sampling frequency. The D flip-flop is a one-bit quantizer to convert the time difference between the input and the reference oscillators to a digital representation.

The differential equation between the output and input of this modulator is given by:

$$V_{out}[n] = V_{in}[n-1] + \frac{1}{G_\phi}(\Delta T_\epsilon[n] - \Delta T_\epsilon[n-1]) \tag{6}$$

where G_ϕ is the voltage-to-time conversion gain and $\Delta T_\epsilon[n]$ is the quantization error made by the D flip-flop.

This $\Delta\Sigma$ modulator was designed and simulated using Cadence Spectre in 0.18μm CMOS technology using the proposed VCDU. The modulator operates over a range of input voltage from 0.15 V to 1 V. The signal ring oscillator is biased at a DC offset of 0.6 V with 400 mV peak-to-peak amplitude for a 111 kHz sinusoid input signal. The reference voltage of the bottom voltage-to-time integrator V_{ref} is set to 1V to

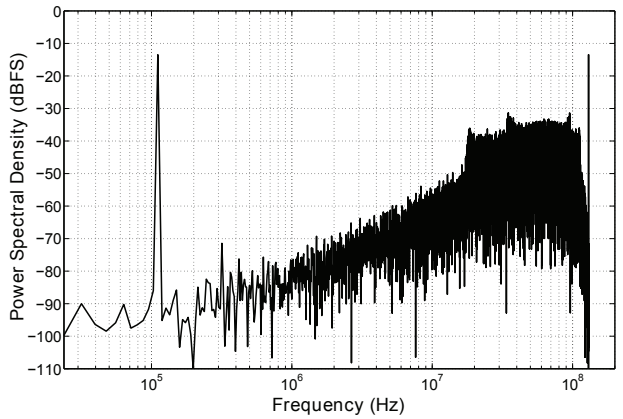

Fig. 8. PSD of the first-order $\Delta\Sigma$ modulator using the proposed VCDU.

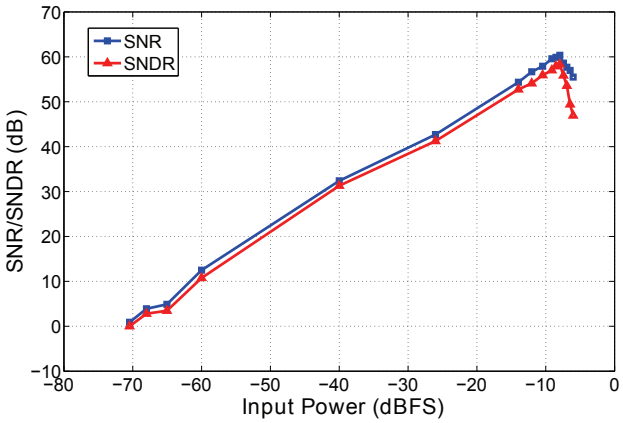

Fig. 9. SNR/SNDR versus input power.

provide a 140 MHz sampling frequency. The signal bandwidth is 400 kHz, yielding an oversampling ratio of 175.

Fig. 8 plots the power spectral density (PSD) of the modulator's output using the proposed VCDU, showing the 111 kHz input signal and first order noise shaping. The spur at 317 kHz is not an harmonic of the input signal caused by nonlinearity; it is caused by periodic quantization noise of the first order $\Delta\Sigma$ modulator. This spur, which could be removed by dithering, actually limits the SNDR of the modulator.

The signal-to-noise ratio (SNR) and SNDR versus input amplitude of the modulator are plotted in Fig. 9. These simulation results show that the peak SNR is 60 dB and peak SNDR is 58 dB. In comparison, the single-ended modulator in [4], also using 0.18μm CMOS technology, the same bandwidth and sampling frequencies, achieves a peak SNDR of 42 dB, thereby confirming that by increasing the VCDU linearity, improved performances are obtained for the time-mode $\Delta\Sigma$ modulator.

V. Conclusion

A new design of a VCDU with signal conditioning is proposed which provides a wider linear range than previously published VCDUs. The circuit-level simulations confirm that the proposed architecture is linear from 0.15 V to 1 V with an equivalent 8-bit linearity error ($\pm$ 0.2%). The obtained voltage-to-time conversion gain is -311 ps/V and its power consumption is 315 μm being supplied by a 1.8 V source. This makes is suitable for time-to-digital conversion application and analog-to-digital conversion of built-in self-test circuits, operating at low supply voltages. The performance which can be expected from this VCDU are confirmed by simulations in an example application of time-mode $\Delta\Sigma$ modulation, showing a 16 dB peak SNDR improvement over a previously reported design.

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