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The Peak-SNR Performances of Voltage-Mode versus Time-Mode Circuits

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***Abstract*—Representing signals in the time domain, as pulses of variable time duration, is a promising solution for analog signal processing in CMOS technologies with low supply voltages. This paper aims at determining the peak SNR of a PMOS-NMOS transistor stack used in both voltage-mode and time-mode circuits. A detailed noise analysis which includes both thermal and flicker noise contributions is performed in both domains. The analysis is applied to different CMOS technology nodes and compared to Spectre transient noise analysis tools. A silicon prototype was fabricated in the IBM 130-nm CMOS technology. Measurements confirm the accuracy of the proposed analysis.**

***Index Terms*—Flicker noise, jitter, signal-to-noise ratio (SNR), technology node length, time-mode, voltage-mode.**

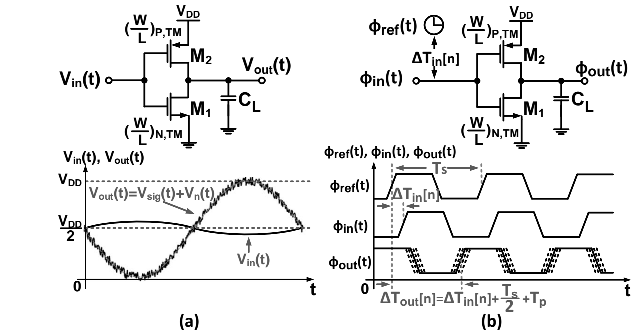

Fig. 1. Basic primitive circuit element consisting of a PMOS-NMOS transistor stack in presence of noise: (a) VM, (b) TM.

I. Introduction

It is widely known that the scaling of CMOS transistors reduces the energy-delay product per transition and increases the overall transistor density, which greatly benefits the realization of complex digital circuits. However, the performance of analog circuits tends to degrade in finer-lined CMOS processes on account of transistor gate leakage effects and reduced signal swings [1], [2]. One possible alternative to perform analog signal processing is to represent signals in the time domain using discrete-time time-differences instead of continuous-time voltage differences [3].

As the time difference between two signals is independent of the amplitude of either signal, intuitively, a time-mode (TM) signal representation is believed to be more compatible with newer CMOS processes that operate at lower power supply levels. It is the objective of TM circuit architects and researchers to identify new circuit architectures that can perform basic signal processing operations such as adding, subtracting, multiplications, etc. At the heart of these efforts is the need to identify TM circuits that perform such operation at high performance levels; levels that equal or exceed those of voltage-mode (VM) circuits at similar power levels. One question that naturally arises is: can TM circuits provide higher operating performance than VM circuits? Today, all empirical data suggests that VM circuits outperform TM circuit realizations at similar power levels.

The objective of this paper is to identify whether future TM circuits will achieve performance levels on par or higher than what is expected from future VM circuits. To do so, the maximum achievable signal-to-noise ratio (SNR) of the most basic circuit element common to both designs: a PMOS-NMOS transistor stack, will be analyzed and used to predict the peak-SNR performance of VM and TM circuits over various technology nodes. In [4], a model for VM and TM noise analysis was proposed; however, the noise model only describes the effect of thermal noise on circuit operation, and therefore is limited in its performance prediction as it ignores the flicker noise component. The accuracy of our proposed analysis is validated by measurement results and transistor-level transient noise simulations.

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II. PMOS-NMOS Transistor Stack: Performance Definitions

A core circuit common to both VM and TM topologies is the PMOS-NMOS transistor stack shown in Fig. 1.

A. Voltage-Mode Analysis

In VM, the output instantaneous voltage signal can be expressed in terms of the input voltage signal $v_{in}(t)$ as

$$v_{out}(t) = Gv_{in}(t) \quad (1)$$

where G represents the voltage gain of the amplifier. As the power supply level V_{DD} limits the maximum output signal, the maximum sinusoidal output signal will have an amplitude of

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$V_{DD}/2$ assuming the output quiescent operating point is set at $V_{DD}/2$. Correspondingly, the rms value of this output signal is $\left(V_{DD}/2\sqrt{2}\right)$. The noise generated by the PMOS-NMOS stack limits the maximum SNR to:

$$SNR_{VM} = 10\log_{10}\left(\frac{V_{sig,rms}^2}{V_{n,rms}^2}\right) \quad (2)$$

where $V_{sig,rms}$ is the rms value of the output signal and $V_{n,rms}^2$ is total rms output noise signal over the bandwidth $f_H - f_L$ (where f_H and f_L are the upper and lower frequency bounds, respectively) that can be expressed as

$$V_{n,rms}^2 = \int_{f_L}^{f_H}\left(\sum_{i=1}^{M} S_{n,i}(f)|H_i(j2\pi f)|^2\right)df \quad (3)$$

Here $S_{n,i}(f)$ $(i = 0, 1, 2, ..., n)$ represents the noise spectral densities (PSD) for each transistor which can include thermal and flicker noise components and $H_i(j2\pi f) = 1/\left(1 + (2\pi R_o C_L f)^2\right)$ is the transfer function from each noise source to the output. To calculate the output-referred noise voltage, the input signal is shorted to the ground and the output noise voltages of M_1 and M_2 is calculated as:

$$V_{n,rms}^2 = \int_{f_L}^{f_H}\left(\left(\left(g_{m,N}^2 S_{n,N}(f) + g_{m,P}^2 S_{n,P}(f)\right)R_o^2\right)|H_i(j\omega)|^2\right)df \quad (4)$$

where

$$S_{n,N/P}(f) = 4kT\gamma\frac{1}{g_{m,N/P}} + \frac{K_{f,N/P}}{W_{N/P}L_{N/P}C_{ox}}\frac{1}{f} \quad (5)$$

and k is Boltzman's constant, T is the temperature, γ is a coefficient which depends on channel length (γ=1 for short-channel), $R_o = r_{oN} \parallel r_{oP}$ (r_{oN} and r_{oP} are output resistance of the NMOS and PMOS transistors, respectively), and $g_{m,N}$ and $g_{m,P}$ are the transconductance of NMOS and PMOS, respectively. The thermal and flicker noise of the transistors are modeled as uncorrelated voltage sources in series with their gates [5]. The second term on the right-hand side of (5), $K_{f,N/P}$ is a process-dependent constant, WL is the product of the transistor's dimensions, and C_{ox} represents the gate capacitance per area. In order to compute the total output noise power, the output PSD is integrated across the bandwidth of the amplifier (from f_L to f_H). The expected SNR is thus

$$SNR_{VM} = 10\log_{10}\left(\frac{\left(\frac{V_{DD}}{2\sqrt{2}}\right)^2}{\left(V_{n,rms,Thermal}^2 + V_{n,rms,Flicker}^2\right)}\right) \quad (6)$$

where

$$V_{n,rms,Thermal}^2 = 4KT\gamma R_o\left(g_{m,N} + g_{m,P}\right)\frac{tan^{-1}(f_H - f_L)}{2\pi C_L}$$

$$V_{n,rms,Flicker}^2 = \left(\frac{K_{f,N}g_{m,N}^2}{W_N L_N C_{ox}} + \frac{K_{f,P}g_{m,P}^2}{W_P L_P C_{ox}}\right)\left(\frac{R_o^2}{2}\right)\times \ln\left(\frac{(2\pi C_L R_o)^2 + \left(\frac{1}{f_H}\right)^2}{(2\pi C_L R_o)^2 + \left(\frac{1}{f_L}\right)^2}\right)$$

B. Time-Mode Analysis

In TM circuits, on the other hand, signals are represented as time differences between two time-varying signals, one acting as the reference (or ground). For instance, the time-difference between the rising edge of an input signal $\phi_{sig}(t)$ and the rising edge of a periodic reference clock signal $\phi_{ref}(t)$ during the n-th clock cycle defines a TM discrete-time signal as

$$\Delta T_{in}[n] = \phi_{in}(t) - \phi_{ref}(t), \quad \text{during n-th clock cycle} \quad (7)$$

For the PMOS-NMOS stack (Fig. 1(b)), with input and output time-varying signals $\phi_{in}(t)$ and $\phi_{out}(t)$, the output TM signal can be expressed in terms of input TM signal as

$$\Delta T_{out}[n] = \Delta T_{in}[n] + \frac{T_s}{2} + T_p \quad (8)$$

where T_s is the sampling period and T_p represents the propagation delay of the PMOS-NMOS stack.

In TM circuits, the signal amplitude is not limited by the power supply level and thus can be made to be arbitrarily large simply by using larger time-difference signals. However, TM signals are discrete by nature. Consequently, to satisfy the Nyquist sampling criterion, a tradeoff exists between the signal amplitude and its bandwidth. A large TM signal will inherently occupy a small bandwidth, and vice-versa [6]. Unfortunately, small-signals are masked in various noise signals, such as jitter from the clock reference circuit, or jitter created by the thermal and flicker noise. As a result, the maximum achievable output SNR will be limited by both the desired bandwidth and output jitter.

Let us assume that the maximum output signal level is bounded by the sampling period, T_s, with maximum output power $\left(T_s/2\sqrt{2}\right)^2$. The noise power is limited by the noise-induced jitter, denoted here by $\sigma_{t_{zc},rms}$. Consequently, the output SNR expressed in dB would be stated as

$$SNR_{TM} = 10\log_{10}\left(\frac{\left(\frac{T_s}{2\sqrt{2}}\right)^2}{\sigma_{t_{zc},rms}^2}\right) \quad (9)$$

An expression of the output timing jitter can be derived from an analysis of the time at which the output signal crosses the threshold level at $V_{DD}/2$ during low-to-high transition. An equivalent circuit with noise representation is shown in Fig. 2(a). The timing diagram of the circuit under test is shown in Fig. 2(b) with the top plot showing the ideal reference signal ($\phi_{ref}(t)$), the second plot showing the input and output voltage signals of the PMOS-NMOS stack, respectively. It should be noted that $\phi_{out}(t)$ is plotted with different rising times in order to show its impact on the output events.

In this section, we describe a method to comprehend the dominant noise sources in TM circuits. While the timing jitter analysis has been described in previous publication [4], it was limited to a small-signal perspective; one that does not apply to TM, as they operate in a digital or large-signal manner. In the following analysis, the large-signal perspective of TM circuits is taken into account to calculate its jitter period. In addition, this analysis includes both thermal and flicker noises in contrast to the work of [4], which performed only a thermal noise analysis.

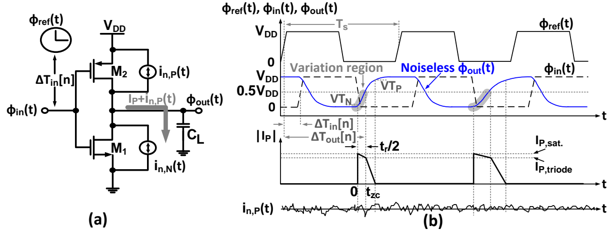

Fig. 2. PMOS-NMOS stack jitter analysis: (a) equivalent circuit with noise representation, (b) timing diagram with noise superimposed.

We begin by assuming that PMOS transistor is turning on and the output signal, $\Phi_{out}(t)$, begins to rise. The charging current flowing into capacitor, C_L, during the initial low-to-high transition is essentially constant at a level of $I_{P,sat}$. While there are minor variations from this constant value, their effects are low enough to be ignored in our analysis. After the low-to-high transition crosses the threshold $V_{DD}/2$, the charging current rapidly decreases to zero. In addition, during this initial time, a noise component from the PMOS transistor $(i_{n,p}(t))$ also contributes to the charge on C_L, resulting in timing jitter. This time will be designated as t_{zc}; which, due to jitter, is a random variable. It is during this time interval that the noise affects the zero crossing. Any noise appearing after this time, has no effect, as the circuit has fully changed state. Here t_{zc} can be expressed in terms of the circuit parameters as follows

$$t_{zc} = \frac{t_r}{2} = \frac{V_{DD}/2}{SR} \quad (10)$$

where t_r is the rise time of $\Phi_{out}(t)$ and $SR = I_{P,sat}/C_L$ is the slew rate during the time interval [0, $V_{DD}/2$]. The PSD of t_{zc} can be expressed as in [7]

$$S_{t_{zc}}(f) = \frac{(t_r/2)^2}{I_{P,sat}^2}\left(sinc^2(\pi f t_r/2) \times S_{i,n}(f)\right) \quad (11)$$

where $S_{i,n}(f)$ in units of A^2/Hz is the PSD of noise current across C_L in terms of both thermal and flicker noise that can be calculated:

$$S_{i,n}(f) = S_{thermal}(f) + S_{flicker}(f) = 4KT\gamma g_m + \frac{K_{f,P}g_m^2}{WLC_{ox}f} \quad (12)$$

The variance of the timing jitter can be found by integration of $S_{i,n}(f)$ from dc to infinite frequency [7], [8] and can be derived as

$$\sigma_{t_{zc}}^2 = \frac{4KT\gamma g_m (t_r/2)^2}{I_{P,sat}^2}\int_0^\infty \left|\frac{sin(\pi f t_r/2)}{\pi f t_r/2}\right| df + \frac{(t_r/2)^2 g_m^2 K_{f,P}}{I_{P,sat}^2 WLC_{ox}}\int_0^\infty \left(\frac{sin(\pi f t_r/2)}{\pi f t_r/2}\right)^2 \frac{1}{f} df \quad (13)$$

The first and second terms in (13) indicate the jitter amount caused by thermal and flicker noise during low-to-high transition. Evaluating the integral for the first term, [7] gives the thermal noise contribution

$$\sigma_{t_{zc},thermal}^2 = \frac{2KT\gamma g_m t_r/2}{I_{P,sat}^2} \quad (14)$$

The solution to the second term integration due to transistor flicker noise contribution is slightly more complicated. However, an approximation can be found by moving the lower limit of dc to a non-zero frequency limit denoted as f_l. In practice, one typically selects an offset frequency of 10 Hz or less from the reference clock frequency, depending on phase noise requirements. Such an analysis was performed in [9] resulting in the following closed-form solution,

$$\sigma_{t_{zc},flicker}^2 = \frac{(t_r/2)^2 g_m^2 K_{f,P}}{I_{P,sat}^2 WLC_{ox}}\left(\frac{3}{2} - Ci\left(2\pi f_l t_r/2\right)\right) \quad (15)$$

where $Ci(x)$ is cosine integral function. Substituting (14) and (15) into (13) and using the expression given previously for t_{zc} in (10), the standard deviation of total jitter due to thermal and flicker noise can be written as follows

$$\sigma_{t_{zc}} = \sqrt{\left[\frac{2KT\gamma g_m V_{DD} C_L}{2I_{P,sat}^3} + \frac{V_{DD}^2 C_L^2 g_m^2 K_{f,P}}{4I_{P,sat}^4 WLC_{ox}}\left(\frac{3}{2} - Ci\left(2\pi f_l \frac{V_{DD}C_L}{2I_{P,sat}}\right)\right)\right]} \quad (16)$$

Although it is not directly evident, depending on the actual rise-time of the circuit, one of the two terms dominates the expression. For instance, when the circuit rise time in a 180 nm process is greater than 65 ns, the flicker noise component will be two times larger than the thermal noise component. Conversely, when the rise time is less than 15 ns, the thermal noise will be two times larger than the flicker noise.

III. Simulation Results

In this section, we shall demonstrate the accuracy of the VM and TM noise and SNR expressions with a Spectre simulation using different CMOS technologies. To begin, our theoretical analysis will be based on device parameters extracted from a TSMC 180 nm CMOS process. These predictions will then be compared with the simulated Spectre results corresponding to VM and TM circuits under the assumption of maximum output signal swing (zero voltage and time offsets). A convenient way to scale down the transistor device parameters is to make use of Dennard's scaling law [10], whereby a scaling factor $1/S$ is used to reduce the device dimensions. Table I consists of two groups of transistor aspect ratios: the initial transistor aspect ratios and another that was optimized for maximum signal swing operation. The initial transistor sizes for the 180 nm process were selected through simulation. The sizes for other technologies were selected by scaling them using Dennard's scaling law. Using the physical parameters shown in Tables I and II, the device parameters (i.e., I_D or $I_{P,sat}$, g_m and r_o) across to three technologies was calculated using a square-law transistor model and is shown in Table III under the columns denoted Theoretical. A second set of columns denoted Simulation is also listed. These are values computed by Spectre using the optimized transistor sizes in Table I.

To show the effectiveness of the proposed analysis, VM output noise and TM jitter as a function of the technology node length is shown in Fig. 3(a) and (b), respectively. In Fig. 3(a) the circuit-level simulated data in different transistor

TABLE I
INITIAL TRANSISTOR SIZES AND OPTIMIZED SIZES FOR SIMULATION.

Mode	Aspect Ratio	Unit	Initial Transistor Sizes: TSMC 180 nm	Dennard's Scaling Rule Applied: IBM 130 nm-svt	Dennard's Scaling Rule Applied: TSMC 65 nm-svt	Optimized Transistor Sizes: TSMC 180 nm	Optimized: IBM 130 nm-svt	Optimized: TSMC 65 nm-svt
VM	$(W/L)_{PMOS}$	$[\mu m/\mu m]$	8/0.54	5.79/0.39	2.88/0.19	8/0.54	4.2/0.36	1.8/0.24
	$(W/L)_{NMOS}$	$[\mu m/\mu m]$	1.8/0.54	1.30/0.39	0.65/0.19	1.8/0.54	1.0/0.36	0.6/0.24
TM	$(W/L)_{PMOS}$	$[\mu m/\mu m]$	2/0.18	1.44/0.13	0.72/0.065	2/0.18	1.5/0.12	0.72/0.065
	$(W/L)_{NMOS}$	$[\mu m/\mu m]$	1/0.18	0.72/0.13	0.36/0.065	1/0.18	0.55/0.12	0.6/0.065

TABLE II
PHYSICAL PARAMETERS OF THE CMOS TRANSISTORS USED IN SIMULATIONS.

Technology node	$\mathbf{V_{TH,P}}$ $[mV]$	$\mathbf{V_{TH,N}}$ $[mV]$	$\mathbf{K_{f,P}}$ $[V^2F]$	$\mathbf{K_{f,N}}$ $[V^2F]$	$\mu_\mathbf{P}\mathbf{C_{ox}}$ $[A/V^2]$	$\mu_\mathbf{N}\mathbf{C_{ox}}$ $[A/V^2]$	**T** $[°K]$
TSMC 180 nm	463	489	1.6×10^{-25}	20×10^{-25}	97.48×10^{-6}	263×10^{-6}	300
IBM 130 nm	289	249	3.4×10^{-25}	22.4×10^{-25}	87.65×10^{-6}	249×10^{-6}	300
TSMC 65 nm	357	320	5.4×10^{-25}	24.6×10^{-25}	34.6×10^{-6}	113.4×10^{-6}	300

TABLE III
THEORETICAL PREDICTION AND SIMULATION RESULTS FOR THE VM AND TM DEVICE PARAMETERS.

Mode	Parameter	Unit	TSMC 180 nm Theoretical	TSMC 180 nm Simulation	IBM 130 nm-svt Theoretical	IBM 130 nm-svt Simulation	TSMC 65 nm-svt Theoretical	TSMC 65 nm-svt Simulation
VM	I_D	$[\mu A]$	104.42	110.7	67.74	66.02	33.35	18.59
	$g_{m,N}$	$[\mu S]$	448.3	488.46	329.65	284.7	162.3	170.7
	r_{oP}	$[K\Omega]$	6.93	4.97	2.83	2.95	17.58	20.74
	r_{oN}	$[K\Omega]$	13.51	15.26	10.52	14.76	30.15	32.79
TM	$I_{P,sat}$	$[\mu A]$	128.8	132.6	93.02	104.8	46.51	48.8
Both	C_L	$[fF]$	150	150	108.33	105	54.16	50

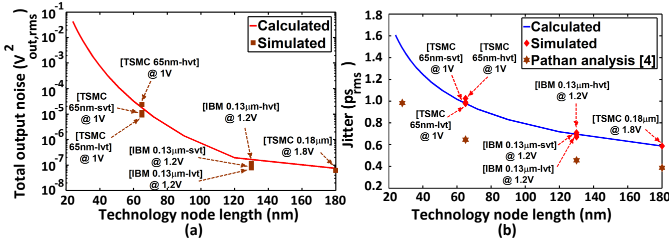

Fig. 3. Output noise and jitter as a function of technology node length: (a) VM circuit, and (b) TM circuit (lvt, std, and hvt are low, standard, and high threshold voltage, respectively).

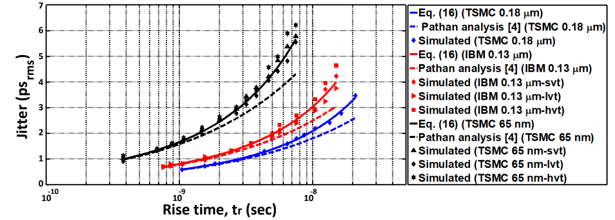

Fig. 4. TM rms jitter versus rise time, t_r.

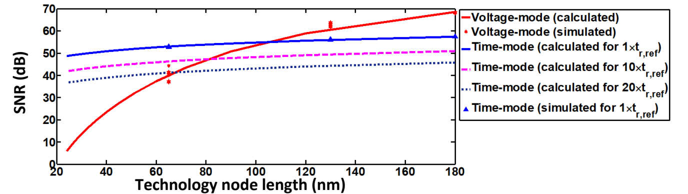

Fig. 5. Peak-SNR performance for VM and TM PMOS-NMOS transistor stack versus technology node length ($t_{r,ref}$=250 ps).

types (e.g., lvt, svt, hvt) together with the theoretical results produced by (6) are displayed. As is evident, the output noise power increases with decreasing node length. In Fig 3(b), the proposed analysis 16 agree with Spectre transient noise simulations within an error of 5%, while it differs by as much as 35% to the thermal noise analysis from [4].

Another result that supports the proposed analysis is by visualizing the TM jitter using (16) against the rise time t_r, as shown in Fig. 4. This can be done by increasing C_L from the values shown in Table III for three technologies while other parameters are maintained constant. As can be seen from Fig. 4, the rms jitter increases with increasing rise time t_r. The discrepancy between simulation results and the analysis in [4] highlights the importance of including the effect of flicker noise as the rise time increases. The analysis is extrapolated to various technology nodes as shown in Fig. 5 to provide insight as to whether TM circuits with different values of rise time, t_r, can surpass SNR performances of VM circuits. Here the reference rise-time $t_{r,ref}$ is set to 250 ps. Our analysis shows that the SNR performances of VM circuits decreases at a faster rate than TM circuits with technology scaling. This can be accounted for by the reduction in power supply level. This is confirmed by our simulation results. Below approximately 100-nm, TM circuits have the potential to provide a better dynamic range than VM circuits.

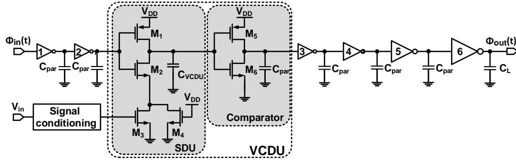

Fig. 6. Schematic of the VCDU.

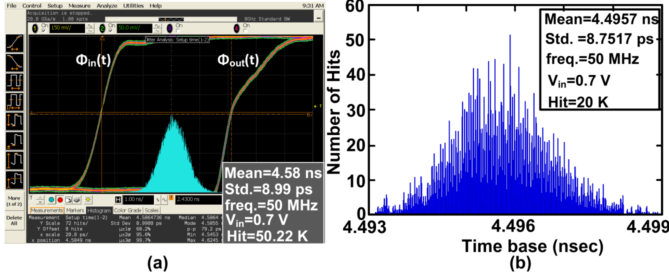

Fig. 7. Jitter histogram of the VCDU, (a) measurement and (b) simulation.

IV. Experimental Validation Of Proposed Theory

In order to verify experimentally the jitter expression proposed in this paper, a voltage-controlled delay unit (VCDU) has been designed based on [11] and fabricated in a 130-nm IBM CMOS process. Fig. 6 shows the schematic of the VCDU which is buffered by a series of inverters at its input and output. From a noise perspective, the circuits of Fig. 2(a) and Fig. 6 are equivalent. As the effect of the noise at the output of the TM circuit occurs during the charging phase of the VCDU, only the top PMOS transistor contributes to the output noise. The NMOS transistors are essentially turned off during the charging phase.

Fig. 7(a) shows the jitter histogram of the time difference between $\phi_{in}(t)$ and $\phi_{out}(t)$ of the fabricated VCDU using a real-time digital oscilloscope (Agilent DSA80000B). The measured mean and rms timing jitter are 4.58 ns and 8.99 ps, respectively, for 50,000 samples for V_{in}=0.7 V and 50 MHz clock frequency. Fig. 7 (b) presents the simulated jitter histogram of the VCDU, showing typical mean and rms jitter of 4.49 ns and 8.75 ps, respectively, at the same condition of experimental setup. Using (16) together with the jitter introduced by the digital input and output drivers, the jitter for VCDU can be calculated as

$$\sigma^2_{t_{zc},total} = \sigma^2_{t_{zc},SDU} + \sigma^2_{t_{zc},Comparator} + \sum \sigma^2_{inv1-6} \tag{17}$$

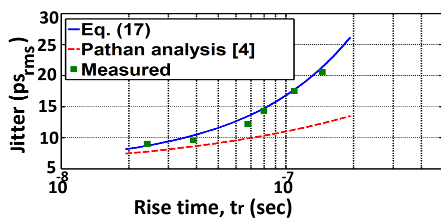

Fig. 8. Comparison of jitter prediction with experimental results.

One finds similar results for rms jitter: 8.73 ps, assuming Gaussian distributed noise. The results show a level of matching between our proposed analysis, simulation and experimental results. As a last test, we measured the rms jitter versus rise time for the VCDU circuit of Fig. 6. These results, shown in Fig. 8, again show the accuracy of the proposed analysis. The discrepancy being attributed to a statistical deviation.

V. Conclusion

An analytical expression for the noise operation of both a VM and TM PMOS-NMOS transistor stack was derived, leading to the expression of the peak-SNR of both architectures. These results can easily be extended to more complicated TM circuits. This work extended the noise analysis of [4] for TM circuits to include both thermal and flicker noise components, as well as the fact that the noise level will be influenced by the rise-time of the TM signals. The proposed noise theory was found to be consistent across different technology nodes through extensive transistor-level transient simulations and through noise experiments involving a custom chip in a 130-nm CMOS process. Our analysis shows that by around 90 nm feature size, TM circuits should provide better SNR than VM circuits for the same bandwidth. However, VM circuits having a longer history of design, they typically perform better than their TM counterparts. More research is therefore required to develop TM circuits that implement complex signal processing (mixing, conversion, filtering, etc.) with a high dynamic range.

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