IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS-I: REGULAR PAPERS, VOL. X, NO. X, 2018 1
Authors accepted manuscript. Article published in Vol. 66, Issue 4, April 2019)
The final published version available at https://doi.org/10.1109/TCSI.2018.2882892

A Second-Order Bandpass $\Delta\Sigma$ Time-to-Digital Converter With Negative Time-Mode Feedback

Soheyl Ziabakhsh, *Student Member, IEEE,* Ghyslain Gagnon, *Member, IEEE,* and Gordon W. Roberts, *Fellow, IEEE*

***Abstract*—This paper presents an all-digital bandpass $\Delta\Sigma$ time-to-digital converter (BP$\Delta\Sigma$TDC) for IF data conversion. The proposed TDC is based on a second-order resonator implemented by a cascade of two time-mode lossless discrete integrators (LDI), and a digital-to-time converter (DTC) in a feedback loop. The DTC is based on a new topology of double-edge voltage-controlled delay unit (VCDU). The proposed TDC achieves bandpass quantization noise shaping and it does not require any complex calibration circuit to compensate for timing errors. To realize the time-mode LDI-based resonator, time-latches with some digital gates are employed. Moreover, a direct feed-forward compensation is utilized in the TDC to attain high signal-to-noise and distortion ratio (SNDR) by reducing the internal time-mode swing, thus relaxing the speed and area requirements on digital circuits leading to low-voltage operation. The prototype BP$\Delta\Sigma$TDC achieves a 39.5 dB peak SNDR over a 0.2 MHz signal bandwidth at 42.8 MS/s while consuming less than 5 mW in a 1.2 V IBM 130 nm CMOS process. The proposed TDC is highly digital and occupies a core area of only 0.048 mm^2.**

***Index Terms*—Bandpass $\Delta\Sigma$ TDC, digital-to-time converter (DTC), lossless discrete integrator (LDI), negative time-difference, noise-shaping, synchronization, time-to-digital converter (TDC), time-latch, negative time-mode feedback.**

I. Introduction

TIME-TO-DIGITAL converters (TDCs) are increasingly used in many applications, such as time-of-flight (ToF) [1], jitter measurement [2], medical imaging [3], all-digital PLL (ADPLL) [4], and time-domain analog-to-digital converters (ADCs) [5], [6]. It is mainly because of this reason that TDCs seem to offer the means to get around many of the obstacles facing analog circuits as one moves to advanced CMOS technology nodes (40 nm or less) [7]. In addition, TDCs provide the opportunity to employ highly efficient digital circuits to realize very complex mixed-signal circuits [8]. Consequently, it is expected that TDCs achieve high-performance (i.e., reoslution, bandwidth, dynamic range, etc.) with the continued scaling the technology nodes.

Various implementations of TDCs have been proposed to process time-mode (TM) information in the range of sub-nanosecond or even sub-picosecond resolution. Some successful examples of Nyquist-rate TDC are Flash TDC [9], pulse shrinking TDC [10], vernier delay line (VDL) TDC [11], two and three dimension vernier TDCs [12], [13], and delay-locked-loop-based (DLL) vernier TDC [14], [15]. However, mismatch between delay elements, leakage, and limited sampling frequency range degrade the performance of such TDCs. Oversampling TDCs with quantization noise shaping have recently emerged as a viable alternative approach to improve the time-resolution and overall conversion dynamic range. Recently, there have been some studies on TM$\Delta\Sigma$ data conversion, as in [16], [17], that have achieved second-order and third-order noise shaping, respectively. However, these TM$\Delta\Sigma$ TDCs rely on analog intensive approaches as the TM signals are converted back to voltage or current signals. These approaches are less attractive in advanced CMOS processes with low supply voltage. To address this issue, a gated-ring oscillator (GRO) based TDC [18], [19] and switched-ring oscillator (SRO) TDC [20] were implemented in an all-digital solution. These approaches nearly halve the chip area and power consumption compared to the conventional designs. In all of the oversampling TDC implementations published thus far, the operation of these circuits is restricted to low-pass (LP) baseband operation.

In this paper, we take a step further by proposing for the very first time a second-order BP$\Delta\Sigma$TDC using digital-like TM arithmetic circuits suitable for bandpass data conversion. The BP$\Delta\Sigma$TDC is designed to operate over a wide range of sampling frequencies, while taking advantage of the technology scaling. The closed-loop TDC is designed using a TM LDI-based resonator, TM subtractor, and an all-digital DTC in a feedback loop. Two different techniques with digital implementation are applied to adjust the timing variations from the main system clock, synchronization and TM phase alignment. In addition, a feed-forward topology is employed to improve the SNDR. The prototype BP$\Delta\Sigma$TDC was fabricated in a IBM 130 nm CMOS process. It operates from 4 MHz to 42.8 MHz sampling frequency and achieves 39.5 dB SNDR, 39.9 dB SNR, and 45.4 dBc SFDR at 0.2 MHz bandwidth in a 42.8 MHz sampling frequency. It dissipates only 4.9 mW from a 1.2 V supply. The active area is 275.1 $\mu m \times 174.4$ μm.

The reminder of this paper is organized as follows. Section II introduces new TM building blocks and extensions to some old ones. In Section III, the architecture of the TM LDI-based resonator and operation details are described. Circuit implementation of the proposed BP$\Delta\Sigma$TDC and simulation results are discussed in Section IV. Section V provides the measurement setup and experimental results, and section VI presents the conclusion.

S. Ziabakhsh and G. Gagnon are with the Department of Electrical Engineering, Ecole de technologie superieure, University of Quebec, Montreal, QC H3C 1K3, Canada. (e-mail: soheyl.ziabakhsh@lacime.etsmtl.ca; ghyslain.gagnon@etsmtl.ca).

Gordon W. Roberts is with the Department of Electrical and Computer Engineering, McGill University, Montreal, QC H3A 2A7, Canada (e-mail:gordon.roberts@mcgill.ca).

II. New TM Building Blocks And Extensions To Some Old Ones

A. Previous Work

The architecture of the proposed BPΔΣTDC is based on a TM memory cell (TLatch) that is able to store (or write) the input time-difference and latch it for further processing (i.e., addition, subtraction, multiplication, or division) [21]. To realize this concept, an inverter-like structure called a switched-delay unit (SDU) is employed to provide the voltage-controlled delay cell with an on-off switch (SW) in the discharging path. The circuit schematic of the SDU is shown in Fig. 1(a). PMOS transistor M_1 serves as a current source to charge capacitor C and $M_2 - M_4$ provides a discharging path for the capacitor. An additional digital inverter is employed to provide a suitable digital signal at the output when the voltage of the capacitor (V_{Cap}) crosses the threshold voltage of the inverter (V_{TH}). The time-difference between the rising edge of CLK to the rising edge of Φ_{out} is a fixed value and denoted as T_{SDU}. The timing diagram of the SDU is illustrated in Fig. 1(b). The capacitor starts to discharge from V_{DD} to ground when CLK is set high. However, if SW is activated low with some pulse-width ΔT_{SW}, the discharge process will be stopped and the voltage across capacitor V_{Cap} will be kept constant. In essence, this action has delayed the discharge time by exactly ΔT_{SW} seconds, resulting in a low-to-high transition appearing at the output T_{SDU} + ΔT_{SW} seconds later.

Fig. 1(c) displays the block diagram of the TLatch, which is composed of a pair of SDUs and some digital gates. During the write mode when $\overline{W}$=0 and $\overline{R_{ref}}$=$\overline{R_{sig}}$=1, the time-difference between the rising edges of $\Phi_{in,ref}$ and $\Phi_{in,sig}$, denoted as ΔT_{in}, is stored in the form of charge into the capacitors of the two SDUs and retrieved after the arrival of the two falling edges at the read ports, $\overline{R_{ref}}$ and $\overline{R_{sig}}$. In the read mode, the stored TM information with the same value of input (ΔT_{in}) can be detected at the output after some internal propagation delay (i.e., T_{SDU}) [21], [22].

The timing diagram of the input/output ports as well as the internal connections of the TLatch are illustrated in Fig. 1(d). The top two plots show the ideal reference ($\Phi_{in,ref}$) and signal clocks ($\Phi_{in,sig}$); the next plot below shows the write signal ($\overline{W}$). This signal is activated on the rising edge of the $\Phi_{in,ref}$ and deactivated on the rising edge of $\Phi_{in,sig}$. The reset signal as depicted in the fourth plot from the top is a global signal and initializes the digital gates of TLatch in each clock cycle. Read signals ($\overline{R_{ref}}$ and $\overline{R_{sig}}$) are set equal to $\Phi_{in,ref}$ so that the output can be read shortly after the arrival of the falling edge at $\Phi_{in,ref}$. Two internal signals, $Trig$ and $SW_{R,S}$, are plotted to illustrate the operation of each digital block. The bottom two plots show the two output signals with time-difference ΔT_{out}. Relative to the input TM signal, the output TM signal is set after a half-period delay of the reference clock $\Phi_{in,ref}$ having a 50% duty cycle. Mathematically, the output TM signals ΔT_{out} can be written as the addition/subtraction of a half-period delay of ΔT_{in} and the time-difference between the two input read signals $\overline{R_{ref}}$ and $\overline{R_{sig}}$ as follows

$$\Delta T_{out}[n] = \Delta T_{in}[n - \frac{1}{2}] \pm \Delta T_R[n] \quad (1)$$

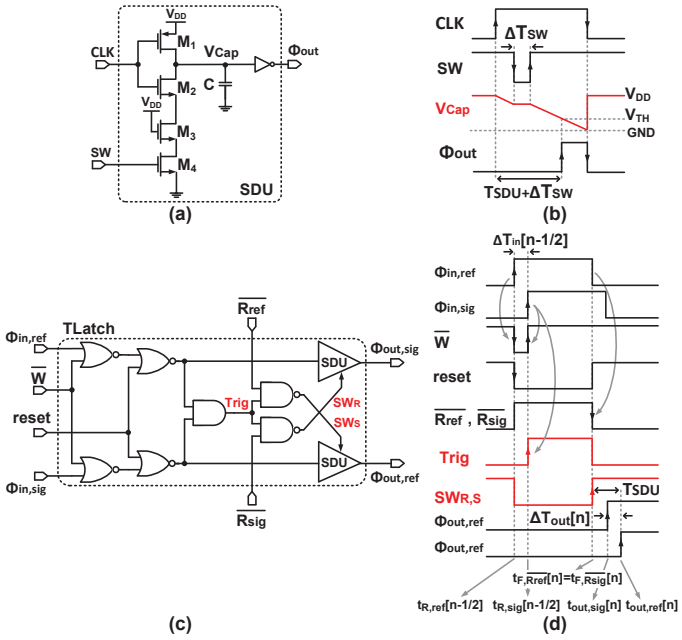

Fig. 1. (a) Schematic of SDU, (b) timing diagram of SDU, (c) circuit diagram of TLatch, (d) timing diagram showing the operation of the TLatch.

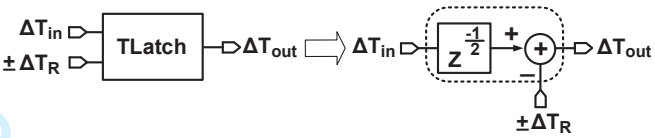

Fig. 2. TLatch equivalent model in z-domain.

where

$$\Delta T_{in}[n - \frac{1}{2}] = t_{R,ref}[n - \frac{1}{2}] - t_{R,sig}[n - \frac{1}{2}] \quad (2)$$

and

$$\Delta T_R[n] = t_{F,\overline{R_{ref}}}[n] - t_{F,\overline{R_{sig}}}[n] \quad (3)$$

Here, t_R and t_F are denoted as the time instance of arrival of the rising and falling edges of input digital signals, respectively. In addition, to represent the half-period delay, we make use of the time index (n-1/2) to represent the second half portion of the nth-cycle of the reference clock signal $\Phi_{in,ref}$. An equivalent z-domain model for the TLatch can then be described with the block diagram shown in Fig. 2.

In the following subsections, we shall describe several the new TM building blocks used in this work: (B) the half-period delay unit, (C) cascading of two half-period delay units, (D) adaptive time offset correction, (E) a TM subtractor and (F) the half-period delay DTC. Ultimately, these will be combined to form the TM LDI-based resonator circuit - the core component of the BPΔΣTDC.

B. Half-Period Delay Unit

The circuit schematic of the half-period delay unit is shown in Fig. 3(a). At its core is a TLatch with some random and sequential logic to control its read, write, and reset signals. These signals are generated by a block identified in the

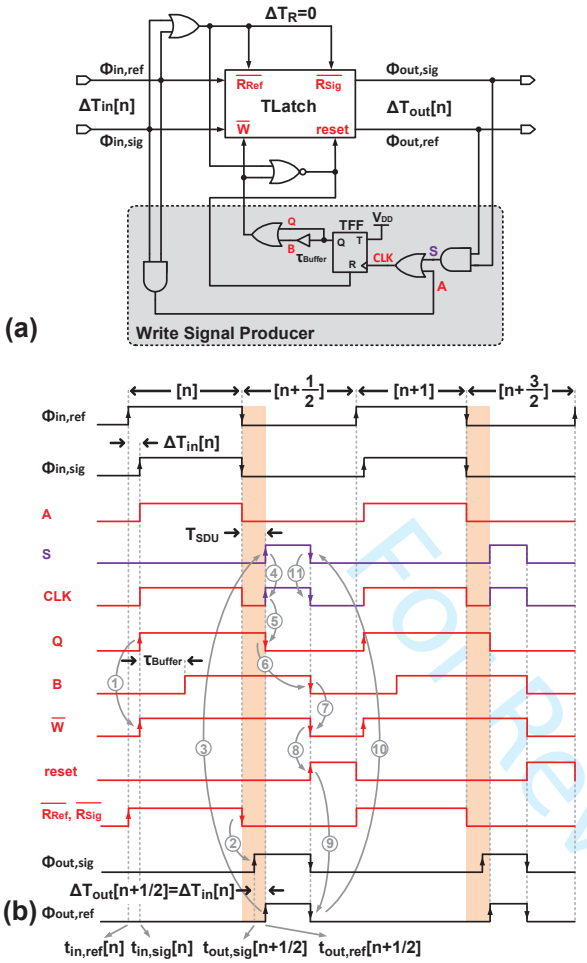

Fig. 3. (a) Circuit implementation of the TLatch with improved timing precision, (b) operational timing diagram.

diagram as the Write Signal Producer. The operation of the overall circuit can be described with the aid of the timing diagram shown in Fig. 3(b). Let us first consider two input signals, $\Phi_{in,ref}$ and $\Phi_{in,sig}$. Here $\Phi_{in,ref}$ is assumed to be a periodic signal with period T_s having a 50% duty cycle. To explain the operation of the circuit, we start from the initial condition when the $\overline{W}$="0", $\overline{R_{ref}}$=$\overline{R_{sig}}$="1", and the T-Flip-Flop (TFF) is reset to its logic low state (i.e., Q =0). In this situation, the TLatch captures the time-difference between two rising edges at $\Phi_{in,ref}$ and $\Phi_{in,sig}$. Upon the arrival of the rising edge at $\Phi_{in,sig}$, say at time $t_{in,sig}[n]$, the CLK input of the TFF will be set to "1" and this changes the output of TFF (Q) from "0" to "1". When Q=1, the write signal of the TLatch ($\overline{W}$) will be set to "1" and the TLatch will be placed into an idle state.

On the arrival of the falling edge at $\Phi_{in,ref}$, both $\overline{R_{ref}}$ and $\overline{R_{sig}}$ go logically low, the two SDUs inside the TLatch begin to discharge towards ground, and deliver the rising edges at the output of the TLatch. When the signal $\Phi_{out,ref}$ is set to a logic high, the digital AND gate connected to the output ports in the Write Signal Producer will set the signal S to "1" in order to reset the TFF to "0" and change the state of $\overline{W}$ to "0." There is a small intensional delay τ_{Buffer} created by a buffer between

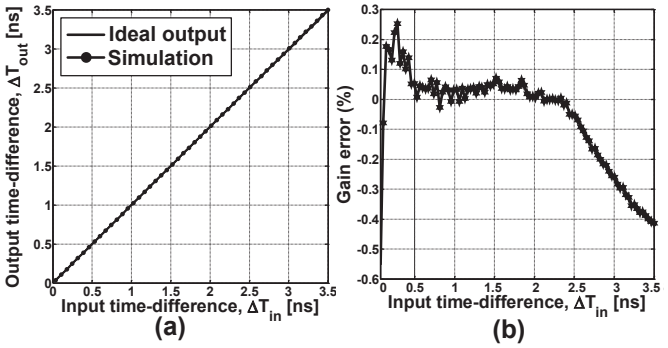

Fig. 4. (a) Input-output transfer characteristic, and (b) gain error for the TLatch circuit shown in Fig. 3(a) as found by Spectre simulation. Note that the time offset is zero for ΔT_{out}.

the output of TFF and the B input to the OR gate. This delay is used to set the pulse-width of the output signal $\Phi_{out,ref}$. After the output rising edges are read out completely (i.e., both TLatch outputs are set high), the TLatch and TFF will be reset by a NOR gate and ready to store the next TM sample value. Assuming this condition is met, the half-period delay cell will automatically store positive/negative TM signals, latch, deliver, and reset itself after each cycle. As a result, the output pair of the rising edges will appear at

$$t_{out,ref}[n+\frac{1}{2}] = \frac{T_s}{2} + T_{SDU} \tag{4}$$

and

$$t_{out,sig}[n+\frac{1}{2}] = \frac{T_s}{2} + T_{SDU} - \Delta T_{in}[n] \tag{5}$$

where T_{SDU} represents the propagation delay of SDUs inside the TLatch, and T_s is the period of the ideal reference clock. This propagation delay introduces a signal-independent time offset for both paths. Using (4) and (5), a difference equation representing the output from the TLatch ($\Delta T_{out}[n]$) can be written as

$$\begin{aligned}\Delta T_{out}[n+\frac{1}{2}] &= t_{out,ref}[n+\frac{1}{2}] - t_{out,sig}[n+\frac{1}{2}] \\ &= \Delta T_{in}[n]\end{aligned} \tag{6}$$

As seen from (6), $\Delta T_{out}[n+\frac{1}{2}]$ is not dependent on the time offset term $T_s/2 + T_{SDU}$.

The output time-difference, ΔT_{out}, for the half-period delay unit is simulated in a 1.2 V IBM 130 nm CMOS process for different input time-differences ranging from 0 to 3.5ns operating with a reference clock of f_s=42.8 MHz. The output response versus input time-differences is shown in Fig. 4(a). As is evident, the simulated ΔT_{out} follows quite closely with a straight line behavior. The relative gain error transfer curve shown in Fig. 4(b) was found to be less than 0.5% in magnitude across the input range from 0 to 3.5ns, which is approximately 15% of the reference clock period. This range can be increased up to the full clock period T_s at the expense of a lower operating frequency, as larger SDU capacitors will be required to reduce charge leakage effects.

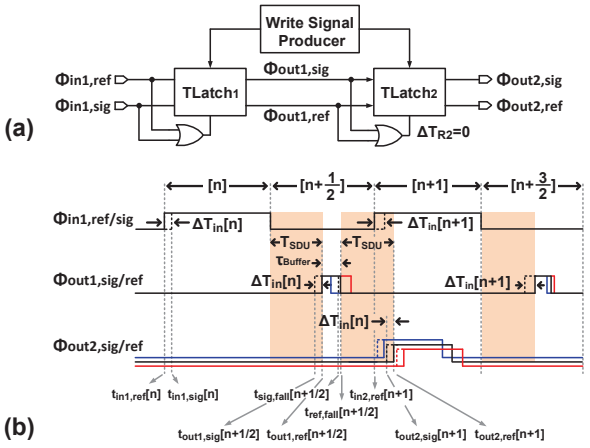

Fig. 5. (a) Block diagram of a cascaded two half-period delays without TFFs, (b) timing diagram ($T_{SDU} = T_s/4$). $\Phi_{in1,ref/sig}$ represents the signals $\Phi_{in1,ref}$ and $\Phi_{in1,sig}$, respectively, and $\Phi_{out1-2,sig/ref}$ represents the signals $\Phi_{out1-2,sig}$ and $\Phi_{out1-2,ref}$, respectively.

C. Cascading Of Two Half-Period Delay Units

An essential feature of the half-period delay circuit shown in Fig. 3(a) is its ability to be cascaded to create a larger delay. For instance, a one-period delay (z^{-1}) can be realized by cascading two half-period delay cells. To complete the circuit, the input and read ports of the second TLatch (TLatch$_2$) are connected directly to the output ports of the first TLatch (TLatch$_1$). This is shown in Fig. 5(a). However, prototypes of the realization have been found to be sensitive to device mismatches among elements in the Write Signal Producer (i.e., digital buffer, digital gates) and the SDU elements of the TLatches leading to a nonlinear transfer characteristic.

Fig. 5(b) shows the timing diagram of a TLatch cascade. To simplify our presentation, the input and reference signals are superimposed on top of one another, thereby highlighting the time-difference signal. This notation will be used extensively throughout this paper. The input TM signal is delayed by a half-period clock to generate the signals $\Phi_{out1,ref}$ (solid line) and $\Phi_{out1,sig}$ (dashed line). In this situation, the time difference between $\Phi_{out1,ref}$ and $\Phi_{out1,sig}$ is latched by the TLatch$_2$ and is kept until the falling edge of the sum of these two signals arrive to initiate the read out of this TLatch (using OR gate in Fig. 5(a)). Unlike the time-to-time integrator in the TM biquadratic filter realization [23], where the output signals of TLatch$_1$ are propagated through the next TLatch and connected to the read signals of TLatch$_2$, in our case it is much more convenient to use the falling edges of $\Phi_{out1,ref}$ and $\Phi_{out1,sig}$ to read out the latched data at the output of the TLatch$_2$ at the proper time. However, the falling edges at the output of the TLatch$_1$, say at time $t_{ref,fall}[n+1/2]$ and $t_{sig,fall}[n+1/2]$, can occur at any time between the rising edge of $\Phi_{out1,ref}$ and the next rising edge of $\Phi_{in1,ref}$, where

$$t_{ref,fall}[n+\frac{1}{2}] = \frac{T_s}{2} + T_{SDU1} + \tau_{Buffer1} \quad (7)$$

and

$$t_{sig,fall}[n+\frac{1}{2}] = \frac{T_s}{2} + T_{SDU2} + \tau_{Buffer2} \quad (8)$$

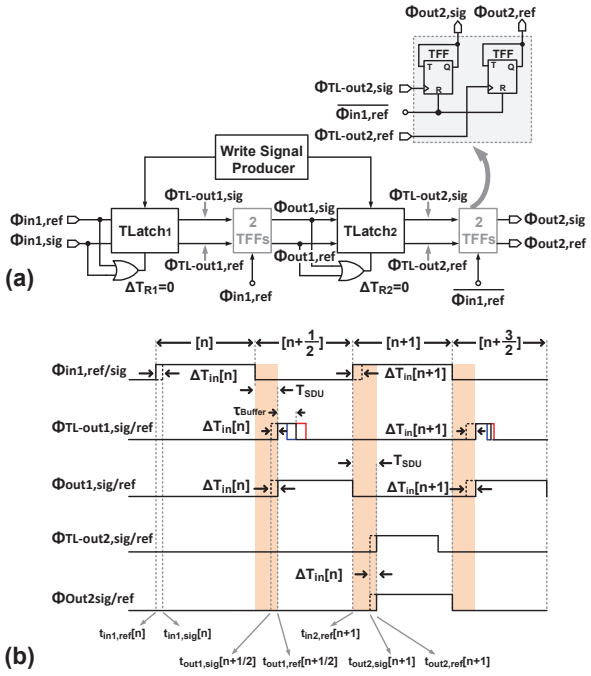

Fig. 6. (a) Block diagram of a cascaded two half-period delays with TFFs, (b) timing diagram ($T_{SDU} < T_s/4$).

Here T_{SDU1} and T_{SDU2} represent the propagation delay of SDU$_1$ and SDU$_2$, respectively, inside TLatch$_1$, and $\tau_{Buffer1}$ and $\tau_{Buffer2}$ represent the individual delay of each buffer in the two Write Signal Producer circuits. The rising edges at $\Phi_{out2,ref}$ and $\Phi_{out2,sig}$ as a function of the n-th cycle of the input reference clock, $\Phi_{in1,ref}$, occur at

$$t_{out2,ref}[n+1] = \frac{T_s}{2} + 2 \times T_{SDU1} + \tau_{Buffer1} \quad (9)$$

and

$$t_{out2,sig}[n+1] = \frac{T_s}{2} + 2 \times T_{SDU2} + \tau_{Buffer2} - \Delta T_{in}[n] \quad (10)$$

Equations (9) and (10) illustrate that the output pair of rising edges of TLatch$_2$ are dependent on T_{SDU1} and T_{SDU2} and the digital buffer delay of the Write Signal Producer block in TLatch$_1$, which is often difficult to set precisely. This issue becomes more serious in face of PVT variations. In addition, the T_{SDU} of each TLatch needs to be designed exactly equal to $T_s/4$ in order to realize the desired transfer function z^{-1}. Using (9) and (10), a recursive difference equation representing the output of the cascaded half-period delays can be written as

$$\begin{aligned} \Delta T_{out}[n+1] &= t_{out2,ref}[n+1] - t_{out2,sig}[n+1] \\ &= \Delta T_{in}[n] + 2 \times (T_{SDU1} - T_{SDU2}) \\ &\quad + \tau_{Buffer1} - \tau_{Buffer2} \end{aligned} \quad (11)$$

Clearly, the differences in the delays along each signal path introduces a unique time offset. To minimize this offset, two additional TFFs can be placed in cascade with the output of each TLatch as shown in Fig. 6(a). The TFFs are synchronize with the falling edges of signals $\Phi_{TL-out1,ref}$ and $\Phi_{TL-out1,sig}$ together with the next rising/falling edge of

$\Phi_{in1,ref}$. In the circuit of Fig. 6(a), the outputs of each TLatch are connected to the clock ports of TFFs. Upon the arrival of a pair of rising edges at $\Phi_{TL-out1,ref}$ and $\Phi_{TL-out1,sig}$, the outputs of the TFFs will change their states to "1" and will be remained unchanged. On occurrence of the rising/falling edge of the reference clock $\Phi_{in1,ref}$ (rising edge for the first pair of TFFs and falling edge for the second pair of TFFs), the outputs of TFFs will be changed to "0" resulting in a synchronization of the falling edges of TLatches with the reference clock $\Phi_{in1,ref}$. Consequently a pulse of fixed width is produced at the TLatch output independent of any digital component mismatch. Subsequently, the output signals $\Phi_{out2,ref}$ and $\Phi_{out2,sig}$ are no longer dependent on any internal buffer delay, as a detail analysis reveals (see Fig. 6(b)) that the rising edge transitions are located at the following time instances:

$$t_{out2,ref}[n+1] = T_s + T_{SDU1} \tag{12}$$

and

$$t_{out2,sig}[n+1] = T_s + T_{SDU2} - \Delta T_{in}[n] \tag{13}$$

Using (12) and (13), the recursive time-difference equation for the $(n+1)$-th time instance will be equal to $\Delta T_{out}[n+1] = \Delta T_{in}[n] + T_{SDU1} - T_{SDU2}$. As is evident, the addition of the TFFs eliminate the effect of the buffer mismatches on the Tlatch time offset.

To see the sensitivity of the rising edges of TLatch_2 with and without TFFs in the presence of transistor mismatches among the digital components in the Write Signal Producer and TLatches, the circuits shown in Fig. 5(a) and Fig. 6(a) were simulated at the transistor level using the Monte-Carlo analysis within Spectre. In this simulation, the widths of individual transistors were assigned a random value drawn from a Normal distribution with a mean value set to its nominal value and a sigma equal to 10% of this value. Two digital square-wave signals at a frequency of 42.8 MHz with a time offset $\Delta T_{in}[n]$ set to 500ps was applied to the input of the unit delay cell (cascade of two half-delay cells). The time-difference between the input rising reference signal $\Phi_{in1,ref}$ and the corresponding output reference signal $\Phi_{out2,ref}$ was evaluated relative to the period of the reference clock T_s, i.e., $\frac{t_{out2,ref}[n+1]-t_{in1,ref}[n]}{T_s}$. Fig. 7(a) shows the histogram of the input-output delay for the circuit shown in Fig. 5(a). Here the input-output time delay exceeded the reference period with a mean value 12% larger than the ideal expected value. Moreover, the overall input-output delay experienced a standard deviation σ of 0.49%. In contrast, Fig. 7(b) shows the histogram of the output delay when TFFs are used at the output of the TLatches. Here one sees that the input-output delay increased slightly to 18% but, more importantly, its σ reduced to 0.34%. While the latter circuit approach introduced a larger output-referred time offset, this offset can be further reduced with the introduction of an adaptive delay circuit.

D. Adaptive Time Offset Correction

While the cascading of two half-period delay block described in the previous section (Fig. 6(a)) offers full-period delay, its input-output delay contains a fairly large time offset.

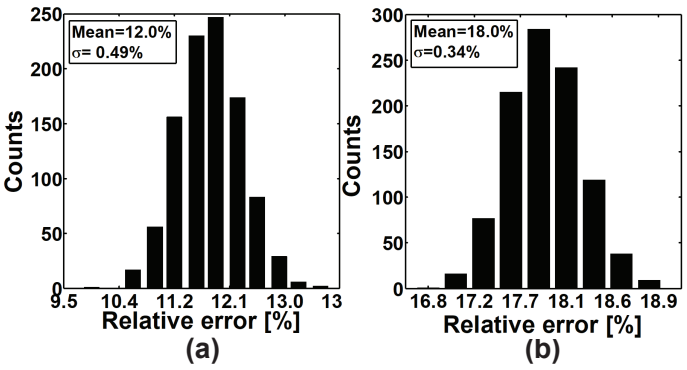

Fig. 7. Monte-Carlo simulations ($N = 1000$ samples) of the cascaded half-period delays (a) without TFFs, (b) with TFFs. The mean and the std have been calculated for the output delay from $t_{in1,ref}[n]$ to $t_{out2,ref}[n+1]$.

Fortunately, this problem can be reduced by designing an adaptive delay block, which is capable of producing a fractional-period delay to compensate for any time offset. The block diagram of the cascaded half-period delay with an adaptive delay along with its detailed timing diagram is shown in Fig. 8. The adaptive delay block receives the output time-difference of TLatch_1 (time-difference between the rising edges of signals $\Phi_{out1,ref}$ and $\Phi_{out1,sig}$) and produces an output signal $\Delta\Phi_{out}$ that is aligned with the rising edge of the reference signal $\Phi_{in1,ref}$. It consists of two main components: a phase-detector and a TM phase alignment circuit. The phase detector provides a pulse-width signal that corresponds to the time-difference between the rising edges of $\Phi_{out1,sig}$ and $\Phi_{out1,ref}$. This can be realized by using a digital XOR gate at the output of TLatch_1. However, this time-difference extraction may contain significant nonlinear components related to the falling edges of $\Phi_{out1,ref}$ and $\Phi_{out1,sig}$. To remove these, the output node of the XOR gate labeled Φ_X is synchronized by the reference clock with an additional digital AND gate to eliminate the unwanted pulse-width signal that occurs after the falling edges of $\Phi_{out1,ref}$ and $\Phi_{out1,sig}$. The output of the phase-detector (signal Φ_{PD}) is directly connected to a TM phase alignment circuit for precise edge placement.

The TM phase alignment circuit is shown in Fig. 8(a). It contains a switch controller block, a multiplexer, an inverter-based delay line, extra pulse remover blocks and a digital ten-input OR gate. The output of the switch controller block is initially low (S="0") and enables the Φ_{PD} pulse signal to arrive at the output port of the multiplexer (MUX). The MUX output then propagates through the inverter-based delay line to generate signals $Q < 1 >$ to $Q < 10 >$. After the arrival of the falling edge of signal Φ_{PD}, selection signal S is set to a logic "1" and stay at this level until a T_{SDU} delay after the next rising edge of the reference clock $\Phi_{in1,ref}$. The second input to the MUX labeled IN_2 is now connected to the MUX output (OUT). This, in turn, closes the loop around the delay line allowing the line to reset itself. Using this technique, there will always be one signal of $Q < i >$ (i=1 to 10) that is aligned with the reference clock.

The ten outputs from the delay line are compared to the low-portion of the reference clock (labeled as T_H) using a bank

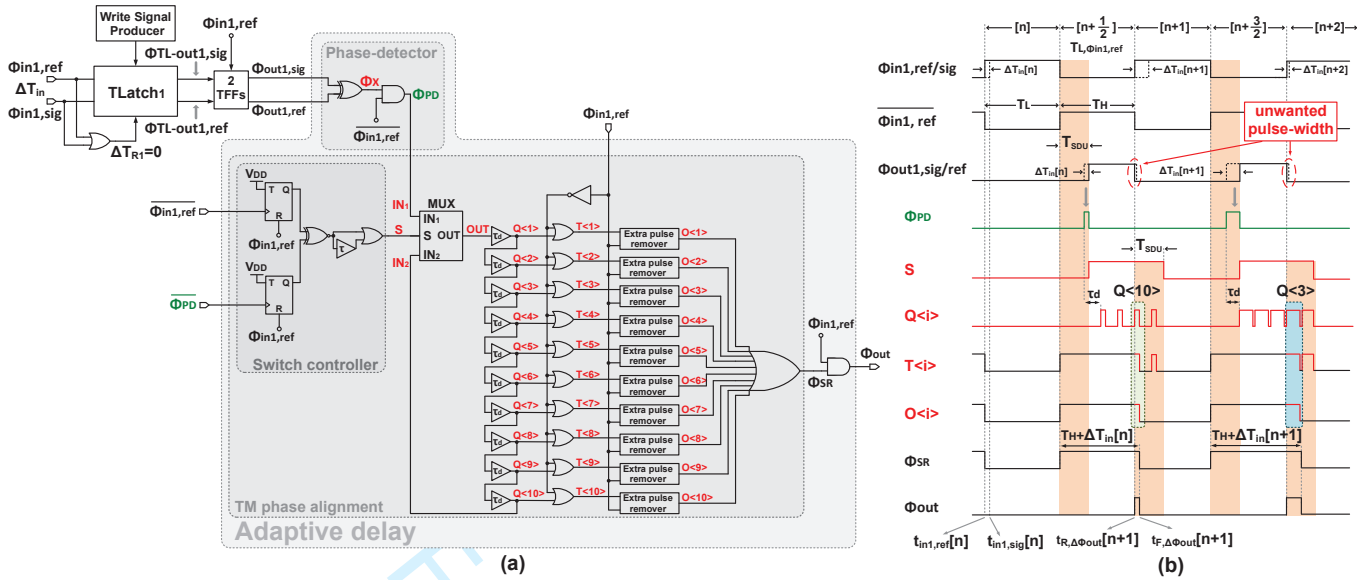

Fig. 8. (a) Circuit diagram of the cascaded half-period delay with an adaptive delay block, and (b) timing diagram.

of two-input OR gates. Subsequently, only those pulses that overlap with the low-portion of the reference clock $\Phi_{in,ref}$ are passed (signals $T<i>$). In order to remove additional pulses that appear after the low activation of $T<i>$, some additional filtering is performed using the extra pulse removal circuits. The outputs of the circuits are then added together by a ten-input OR gate to produce Φ_{SR}. Consequently, Φ_{SR} will be set high for a duration equal to the duration of the low-portion of the reference clock and the duration of the Φ_{PD} signal. The time difference between the falling edge of Φ_{SR} and the rising edge of $\Phi_{in,ref}$ is used to generate an output signal Φ_{out} with a pulse-width equal to that established by Φ_{PD} using a two-input AND gate with no offset with respect to the rising edge $\Phi_{in,ref}$.

To illustrate this operation, a timing diagram is presented in Fig. 8(b)). During the n-th clock cycle, $Q<10>$ is aligned with the falling edge of $\overline{\Phi_{in,ref}}$ and during the next clock cycle, $Q<3>$ is aligned with the falling edge of $\overline{\Phi_{in,ref}}$. Here, the extra pulse remover block eliminates the extra shifted of the Φ_{PD} signal and generate signal Φ_{SR} whose pulse-width is $T_H + \Delta T_{in}$. Digitally multiplying the Φ_{SR} with $\overline{\Phi_{in1,ref}}$ results in a well-aligned output signal, Φ_{out}.

Fig. 9 shows the circuit schematic and the timing diagram of the extra pulse remover circuit. The *valid controller logic* generates the signals $\overline{En}$ and reset (R) for the TFF with a delay of $\tau = T_{SDU}$ from the input reference clock $\Phi_{in1,ref}$. The signal $\overline{En}$ is digitally multiplied by the input signal $T<i>$ to produce the signal A which eliminates the most shifted signal of Φ_{PD}. Signal R sets the $\overline{Q}$ of TFF to level "1" and keeps its state until the falling edge of $T<i>$ has arrived. The $\overline{Q}$ and A are then multiplied together using a two-input AND gate to produce the output $O<i>$ signal without any additional pulses.

To verify the operation of the circuit shown in Fig. 8(a), a Monte-Carlo simulation was performed to obtain the output delay from the rising edge of the reference clock, say at time

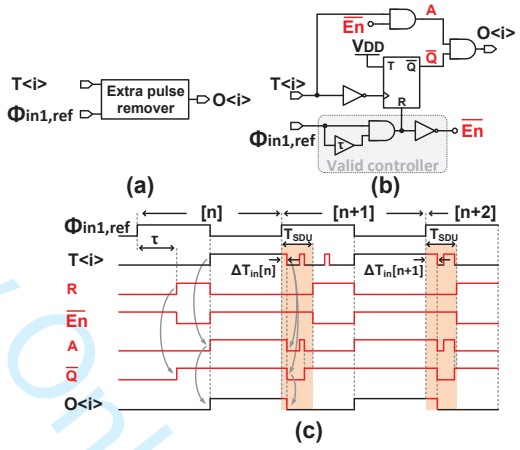

Fig. 9. Extra pulse remover: (a) block diagram, (b) circuit schematic, (c) timing diagram.

$t_{in1,ref}[n]$, to the rising edge of Φ_{out} when subject to the same device mismatches described earlier. Fig. 10 shows the relative error histogram for the cascaded half-period delay with an adaptive delay circuit. The error histogram appears Gaussian with a mean and a standard deviation of 0.1% and 0.095%, respectively. As is evident, the offset has been greatly reduced without increased sensitivity to device mismatches.

E. TM Subtractor

Fig. 11(a) illustrates the circuit schematic of the TM subtractor, which is a modified form of the TM subtractor first described in [22]. Here the subtractor circuit uses a TLatch in the feedforwad path, and an adaptive delay, a negative time-difference detector block as well as two MUXs in the read path. The TLatch is considered as the computational memory that stores the input time-differences, ΔT_{in1}, and performs basic arithmetic operations (i.e., addition or subtraction) from

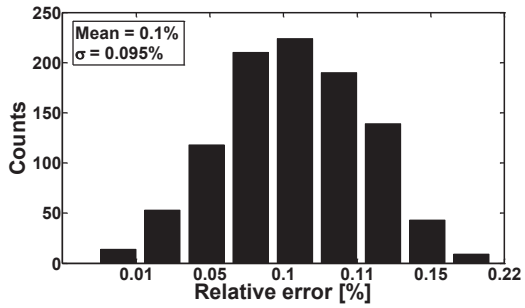

Fig. 10. Monte-Carlo analysis (N = 1000 samples) for the transistor mismatches (ΔT_{in} = 500 ps, $T_{SDU} = T_s/8$, and f_s = 42.8 MHz).

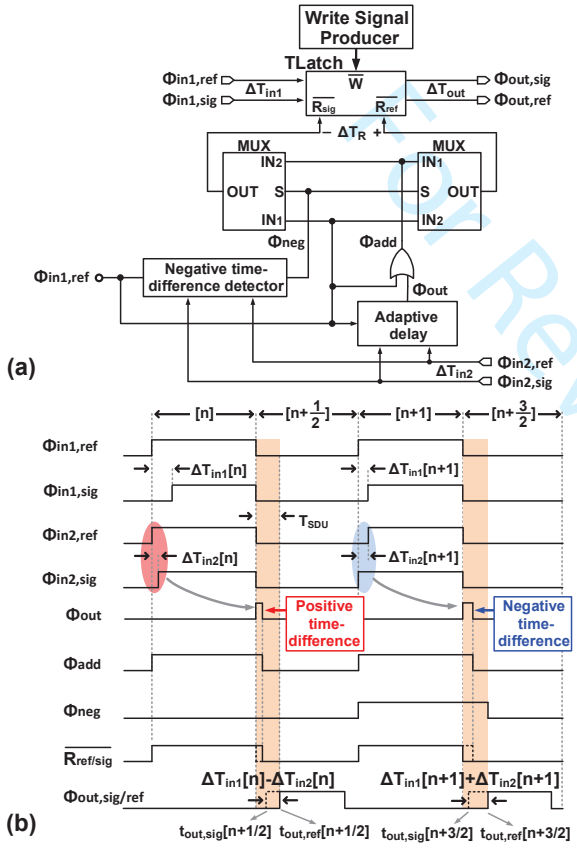

Fig. 11. (a) Block diagram of the modified TM subtractor and (b) timing diagram.

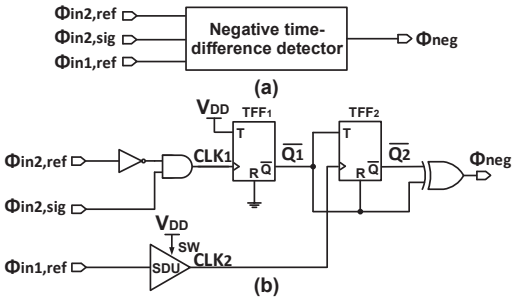

Fig. 12. Circuit schematic of the negative time-difference detector.

the second input signal, ΔT_{in2}. In this implementation, the time-difference of ΔT_{in2} is first extracted and aligned with the reference clock, $\Phi_{in1,ref}$. At the same time, the polarity of ΔT_{in2} (i.e., positive or negative) is detected at each sampling instant by the negative time-difference detector and flips the roles of $\overline{R_{ref}}$ and $\overline{R_{sig}}$ by changing the selector inputs of each MUX (S pin).

To better understand the TM subtractor, the subtraction of two categories of signals will be illustrated in Fig. 11(b): one involving a positive TM signal $\Delta T_{in2}[n]$, and another involving a negative TM value. Beginning with the positive TM signal case, during the n-th clock cycle, both TM input samples, $\Delta T_{in1}[n]$ and $\Delta T_{in2}[n]$, are positive and connected to the input and read ports, respectively, of the TLatch. As seen in Fig. 11(b), the TLatch captures the $\Delta T_{in1}[n]$ at its input ports and waits for the $\Delta T_{in2}[n]$ to be aligned with the falling edge of the reference clock $\Phi_{in1,ref}$ then generates the signal Φ_{out}. The signal Φ_{out} is then added with $\Phi_{in1,ref}$ to produce signal Φ_{add}, which is connected to either $\overline{R_{ref}}$ or $\overline{R_{sig}}$, depending on the positive/negative sign of ΔT_{in2}. The edge alignment and time addition are performed by the adaptive delay line and a digital OR gate, respectively. At the arrival of an input pair of falling edges labeled with $\overline{R_{ref}}$ and $\overline{R_{sig}}$, the subtraction of two TM signals will be read out. As a result, the rising edges at the output of the TLatch occurs at

$$\begin{aligned}\Delta T_{out}[n+\frac{1}{2}] &= t_{out2,ref}[n+\frac{1}{2}] - t_{out2,sig}[n+\frac{1}{2}] \\ &= \Delta T_{in1}[n] - \Delta T_{in2}[n]\end{aligned} \quad (14)$$

During the $(n+1)$-th clock cycle, when $\Delta T_{in1}[n] > 0$ and $\Delta T_{in2}[n] < 0$, the negative time-difference detector will change Φ_{neg} to "1", thereby forcing the multiplexers to change the connection of read signals. In this situation, $\Delta T_{in1}[n+1]$ stored in the TLatch will be added to the $\Delta T_{in2}[n+1]$. As shown in Fig. 11(b), the time difference between the output rising edges for the $(n+1)$-th cycle of the reference clock can be written as

$$\begin{aligned}\Delta T_{out}[n+\frac{3}{2}] &= t_{out2,ref}[n+\frac{3}{2}] - t_{out2,sig}[n+\frac{3}{2}] \\ &= \Delta T_{in1}[n+1] + \Delta T_{in2}[n+1]\end{aligned} \quad (15)$$

The circuit schematic of the negative time-difference detector is shown in Fig. 12. In this circuit, the negative time-difference at the input signals $\Phi_{in2,ref}$ and $\Phi_{in2,sig}$ is detected by an AND and a NOT digital gate to produce the CLK_1 signal. Upon the arrival of the rising edge at Φ_{neg}, $\overline{Q_1}$ is set to "0", which activates the TFF$_2$ to change its state when the rising edge of CLK$_2$ arrives. To synchronize the TFF$_2$ with the input reference clock of the TM subtractor, $\Phi_{in1,ref}$, a SDU with a propagation delay of T_{SDU} is utilized. The additional XOR gate at the output sets the Φ_{neg} to logic "1" whenever the rising edge occurs on either $\overline{Q_1}$ or $\overline{Q_2}$.

Fig. 13 shows the Spectre simulation of the output time-difference versus ΔT_{in2} for the TM subtractor with and without digital circuits to control the read ports. As is evident, when the multiplexers and negative time-difference detector shown in Fig. 11(a) are used in the read path, the TM subtractor circuit is able to distinguish between the positive

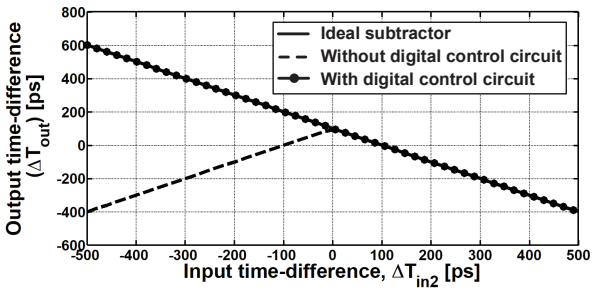

Fig. 13. Simulation results of the TM subtractor: output time-difference (ΔT_{out}) versus ΔT_{in2} with ΔT_{in1}=100 ps at 42.8 MHz.

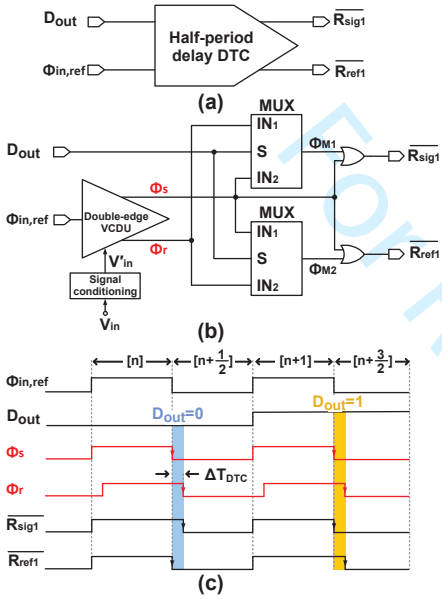

Fig. 14. Half-period delay DTC: (a) block diagram, (b) circuit schematic, (c) operational timing diagram.

or negative TM signals carried by ΔT_{in2} and subtract it from ΔT_{in1}. The output response (line with black circles) is compared with the ideal (solid line only) and the subtractor without digital control (dashed line only) responses. As can be seen from the simulation, there is a good agreement between the simulation of circuit shown in Fig. 11(a) and the ideal subtractor.

F. Half-Period Delay DTC

A final building block necessary to realize a BP$\Delta\Sigma$ modulator is the digital-to-time converter (DTC). A detailed schematic of the DTC used in this work together with its timing diagram are shown in Fig. 14. The circuit corresponding to this block will take as input a 1-bit digital signal on the rising edge of $\Phi_{in,ref}$ and produce a corresponding output TM signal ($\overline{R_{ref1}}$ and $\overline{R_{sig1}}$) centered around the falling edge of the $\Phi_{in,ref}$. More specifically, for a digital input of logic "0" the DTC will produce an output TM signal $\overline{R_{sig1}}$ that lags the reference signal $\overline{R_{ref1}}$ by 1 ns. $\overline{R_{ref1}}$ will be activated on the falling edge of $\Phi_{in,ref}$. Conversely, for a input of logic "1" the output $\overline{R_{ref1}}$ will be made to lag behind the $\overline{R_{sig1}}$ by 1 ns, when $\overline{R_{sig1}}$ is activated on the falling edge of $\Phi_{in,ref}$. The magnitude of 1 ns pulse-widths were selected to ensure that the subtractor at the front-end of the modulator does not saturate. Numerous transistor-level simulations were performed using Spectre to identify this value. At the core of the DTC is a new type of delay element block which will be referred to as the double-edge VCDU. This block is an extension of previous proposed VCDUs [24]. Past VCDUs would delay the incoming rising edge of a digital signal by an amount determined by an input voltage level V_{in}. In this work, a signal conditioning block is used at the input control voltage port to increase the VCDU linear operating region. Readers can refer to [25] for more details.

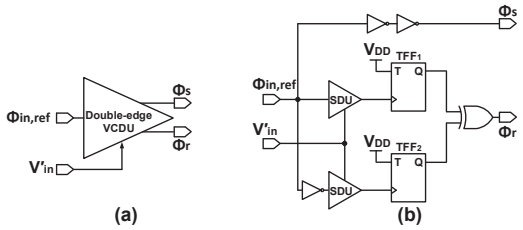

Fig. 15. (a) Block diagram of the double-edge VCDU, (b) circuit schematic of the double-edge VCDU.

In the case of a double-edge VCDU, both the rising and falling edges of the incoming digital signal are delayed in equal portion with respect to the input control voltage V_{in}. In other words, a double-edge VCDU delays both transitions of the input reference signal $\Phi_{in,ref}$ by the exact same amount set by V_{in}. This provides an opportunity to run TM circuits at twice their normal operating speed, or as demonstrated here, to provide a half-period delay DTC. Another key benefit of using the double-edge VCDU is that the output time-difference of the DTC, denoted by ΔT_{DTC}, can be easily controlled by V_{in} over a linear range, and thus no significant circuit-level design effort is required.

The detailed implementation of the double-edge VCDU is shown in Fig. 15. Two SDUs are clocked at the rising and falling edges of the reference signal, $\Phi_{in,ref}$, and produce two signals with propagation delay T_{SDU} relative to the rising and falling edges of $\Phi_{in,ref}$. These two signals are then used to toggle the two TFFs such that the XOR of their Q-outputs produce signal Φ_r with the same period of $\Phi_{in,ref}$. The signal Φ_s is equal to the input reference clock $\Phi_{in,ref}$ with the same propagation delay as those circuits that appear in the signal path defined from $\Phi_{in,ref}$ to Φ_r.

Fig. 16(a) shows the transient response of the double-edge VCDU with input bias conditions (V_{in}) ranging across the voltage supply from 0 V to 1.2 V. As is evident, for the each input voltage, V_{in}, the time-difference between the rising edges of the reference clock, $\Phi_{in,ref}$, and the output of the double-edge VCDU, Φ_s, is equal to the time-difference between the falling edges of $\Phi_{in,ref}$ and Φ_s. In order to verify the linearity of the propose double-edge VCDU, we performed a transistor-level Spectre simulation. The results sre shown in Fig. 16(b), where the linearity error is defined as the largest deviation from the linear behavior over the ideal response in

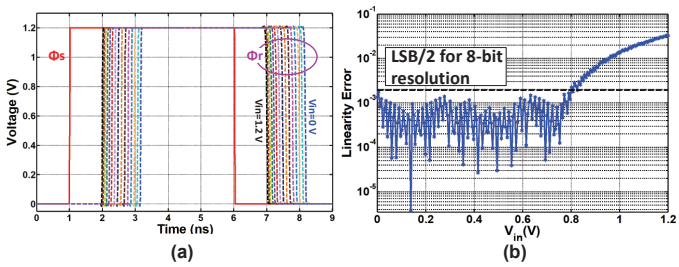

Fig. 16. Transistor-level simulation results of the double-edge VCDU: (a) transient response at different voltage input voltages and (b) linearity error. The relative linearity error is defined as the largest deviation from the ideal behavior over the full scale linear range of the input voltage. Note that $\Phi_s = \Phi_{in,ref}$.

percent [25]. Simulation results indicate that the linear range for both rising and falling edges is below the 8-bit resolution for a full-scale range from 0 to 0.8 V.

III. TM LDI-Based Resonator

To achieve a BP$\Delta\Sigma$TDC with a narrow 3-dB bandwidth and deep notch frequency (equivalently, one with a high Q-factor), the second-order TM LDI-based resonator shown in Fig. 17 will be used. Part (a) of this figure shows the z-domain block diagram of the proposed LDI-based resonator with input-output transfer function

$$T(z) = \frac{z^{-1}}{1+z^{-2}} \tag{16}$$

and (b) illustrates the corresponding block diagram using TLatches. This particular arrangement was selected based on the half-period delay that can be realized by the TLatch. As is evident from Fig. 17(a), six TLatches can be used to implement the resonator structure: two in the feedforward path and four in the feedback path. However, due to manufacturing processing errors, temperature and supply voltage variations, one of the half-period delay elements in the feedback loop will be replaced by the adaptive delay element. One additional advantage of using the adaptive delay element in the feedback path is that it is capable of handling a wide range of sampling clock frequencies. This is because the adaptive delay tracks the phase alignment between its input TM signal and the reference clock so that the total loop delay in the feedback path is nearly equal to two clock-period delays (i.e., z^{-2}). While process errors can also affect the delay in the feedforward path of the LDI resonator involving TLatch_1 and TLatch_2, this error will be accommodated by the DTC in the feedback loop of the BP$\Delta\Sigma$TDC - more on this later in section IV. It is also important to note that TLatch_2 performs a subtraction role in addition to including a half-period unit delay in the feedforward signal path.

The circuit-level implementation of the proposed second-order TM LDI-based resonator is shown in Fig. 18(a). The feed-forward path consists of a half-period delay unit and one input port to the TM subtractor to realize the numerator portion of the resonator transfer function (Eqn. (16)). The denominator term $(1+z^{-2})$ is achieved by the application of three half-period delay units and another port of the subtractor circuit

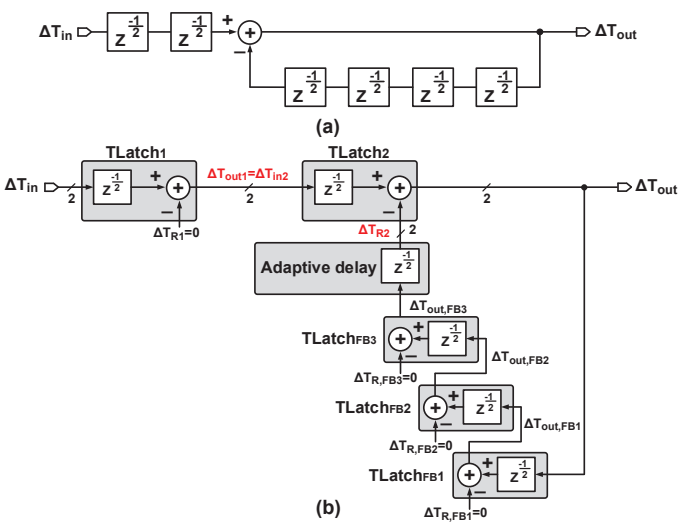

Fig. 17. (a) z-domain LDI-based resonator consisting of two half-period delay elements in the feedforward path and four half-period delay elements in the feedback path, (b) the block diagram of the proposed TM LDI-based resonator constructed with multiple TLatches.

of Fig. 11 - which includes another TLatch and the adaptive delay element for another half-period delay.

The timing diagram of the proposed TM LDI-based resonator is illustrated in Fig. 18(b). Starting from the first two cycles corresponding to the time index $[n-1]$ and $[n]$, the output is assumed to equal $\Delta T_{in}[n-1]$ and $\Delta T_{in}[n]$, respectively. During the $[n+1]$-th cycle, $\Delta T_{in}[n-1]$ appears at the output of (TLatch_{FB3}) in the feedback path. The time-difference between the two rising edges of the output of TLatch_{FB3} (i.e., $\Phi_{out,ref,FB3}$ and $\Phi_{out,sig,FB3}$) is then extracted by a phase-frequency detector (PFD) and aligned with the reference clock $\Phi_{in,ref}$. However, over one period of the reference clock $\Phi_{in,ref}$, the feedback signal produces a negative time-difference, meaning that the rising edge of $\Phi_{out,ref}$ leads the rising edge of $\Phi_{out,sig}$. This negative TM instance will appear at the output of TLatch_{FB3} during the $[n+4]$-th time instance and sets the Φ_{neg} signal to "1" T_{SDU} seconds after the next rising edge of clock reference. This, in turn, flips the subtractor into its adder mode. As a result, the desired transfer function is achieved at the output of the TM LDI-based resonator (ΔT_{out}).

The circuit prototype of the TM LDI-based resonator was designed in a 130 nm IBM standard CMOS process with a 1.2 V supply voltage. The proposed resonator operates over a wide input range (ΔT_{in}) from 0 to 3.5ns under different sampling frequencies from 4 MHz to 43 MHz. The lower limit of the sampling frequency is set by the capacitor current leakage in the SDU of the TLatches during their holding phase. Conversely, the upper limit is due to the charging time constant established by the SDU capacitors. In this design, a compromise between the current leakage and bandwidth limitation lead to the SDU capacitors being set to 600 fF.

To verify the performance of the resonator, a step response with a constant input time-difference of 1 ns was applied to the input of the resonator (i.e., ΔT_{in}=1ns) and the corresponding output TM signal was captured and analyzed using an FFT.

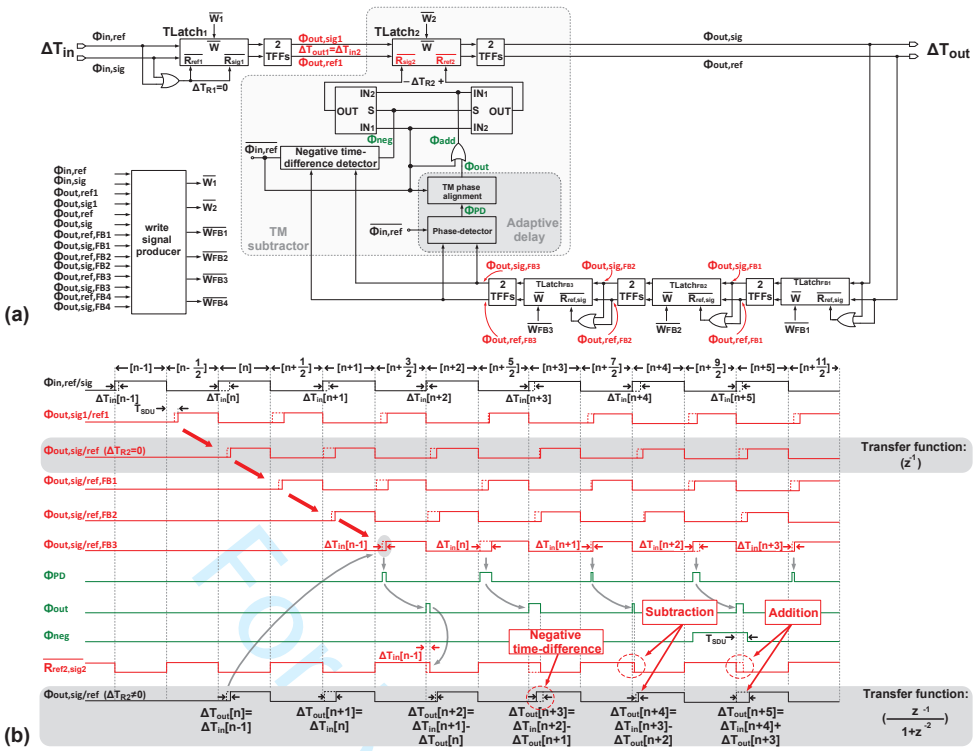

Fig. 18. TM LDI-based resonator with negative TM signal detect circuitry: (a) circuit schematic, (b) timing diagram. $\Phi_{out,sig/ref,FB1-3}$ in the timing diagram represents the signals $\Phi_{out,sig,FB1-3}$ and $\Phi_{out,ref,FB1-3}$, respectively.

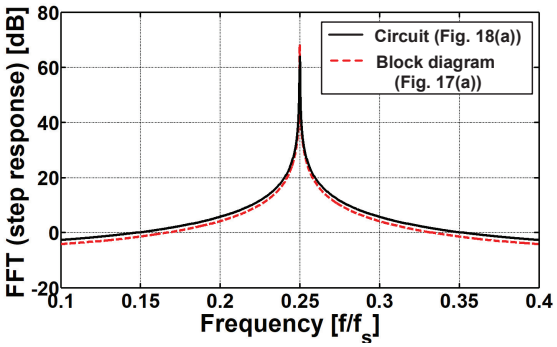

Fig. 19. Simulation results of the step response of the circuit-level implementation in Fig. 18(a).

The results are shown in Fig. 19 for both the transistor-level circuit implementation and the block-level system description shown in Fig. 17(a).

As is clearly evident, the resonance peak of the TM LDI-based resonator and system-level simulation are very similar; occurring at the desired frequency of $f_s/4$. In addition, one sees that the 3-dB bandwidth of either response is quite small. Detail analysis reveals a Q-factor is seen to be greater than 10.

IV. Second-Order BPΔΣTDC Circuit Implementation And Simulation Details

Fig. 20 shows a closed-loop architecture with feed-forward compensation of the proposed BPΔΣTDC. This TDC utilizes

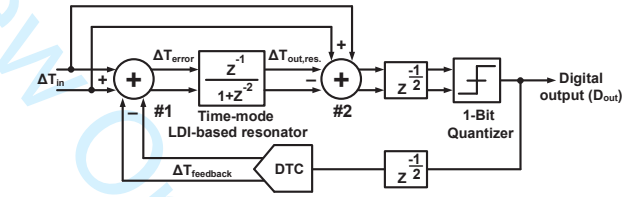

Fig. 20. Block diagram of the essential components in the proposed BPΔΣTDC.

a TM LDI-based resonator with transfer function $\frac{z^{-1}}{1+z^{-2}}$ whose poles are located at $\pm f_s/4$. The TM signals at the output of the resonator is subtracted (subtractor #2) from the input TM samples and passed through a 1-bit quantizer to obtain the digital output. The quantized signal is then converted back to the TM signals by a one-bit DTC and fedback to the first subtractor (subtractor #1).

The overall design of the prototype second-order BPΔΣTDC circuit is shown in Fig. 21. The feed-forward path of the TDC consists of a modified TM LDI-based resonator where a second input port of $TLatch_1$ (read ports) is provided to allow for the subtraction of a feedback TM signal, another TLatch acting as a second subtractor ($TLatch_3$) and a quantizer (DFF) clocked at f_s. The feedback path consists of a half-period delay DTC. In addition, control signals are generated by the Write Signal Producer block shown at the top of the diagram. This block provides the write signals for all TLatches in the appropriate time sequence.

In this work, several architecture and circuit techniques are

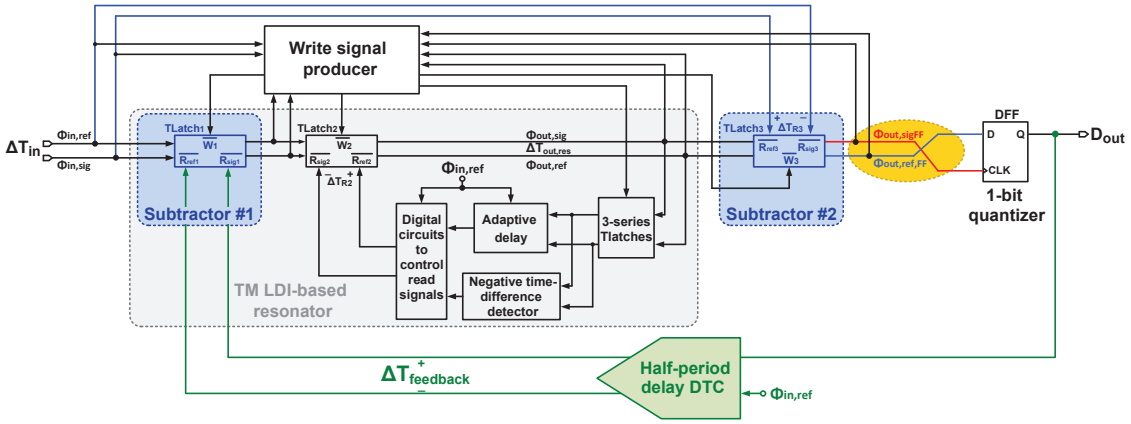

Fig. 21. Top-level schematic of the proposed BP ΔΣ TDC. TFFs in the output of $TLatch_1$ and $TLatch_2$ are not shown for simplicity.

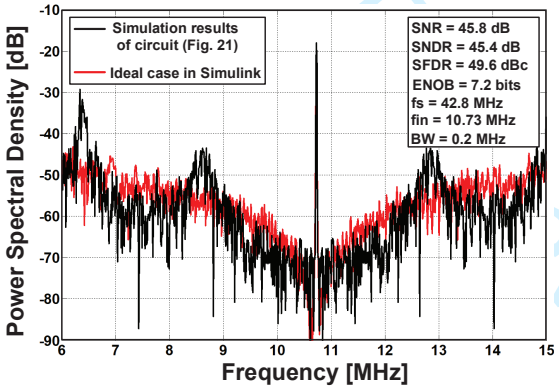

Fig. 22. Simulated PSD of the transistor-level circuit of BPΔΣTDC and Simulink system-level BPΔΣ modulator.

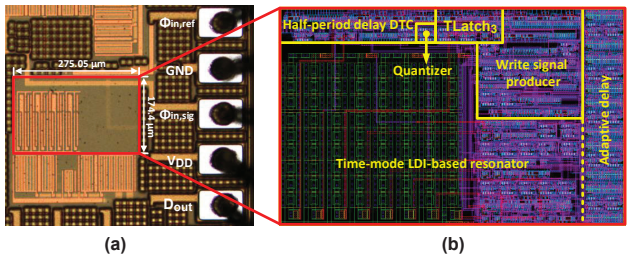

Fig. 23. (a) Die photograph, (b) TDC core layout.

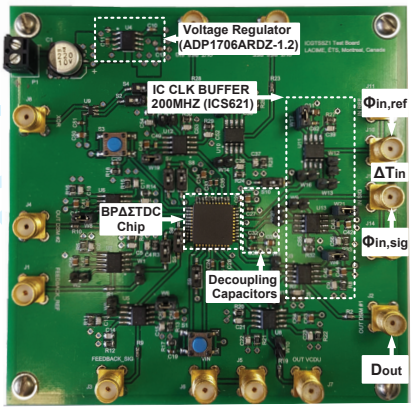

Fig. 24. Photograph of the customized board to test the TDC circuit.

employed to achieve the desired SNDR with minimum silicon area and power. Firstly, $TLatch_1$ used as a half-period delay unit inside the LDI resonator is modified to enable the LDI resonator to act on the time-difference between the input signal ΔT_{in} and the feedback TM signal $\Delta T_{feedback}$; thus, no extra TLatch is necessary at the front-end. Secondly, a direct feed-forward compensation path is incorporated to increase the SNDR of the modulator. By using this direct feed-forward path, the TM resonator's output swing can be reduced, as it only needs to process the quantization noise error and is free from the input TM signals [26], [27]. To implement this technique in the time-domain, $TLatch_3$ is included at the output of the resonator to subtract the input TM signal, ΔT_{in}, from the output of the resonator, $\Delta T_{out,res}$. This TLatch uses the same circuit topology as that shown in Fig. 3(a). Intentionally, ΔT_{in} and $\Delta T_{out,res}$ are connected to the read and input ports of $TLatch_3$, respectively. Thirdly, to maintain negative feedback around the loop involving the LDI resonator and the 1-bit quantizer (DFF), signals $\Phi_{out,sig,FF}$ and $\Phi_{out,ref,FF}$ are connected to the CLK and D inputs of the DFF, respectively. Fourthly, a DTC with a half-period delay is employed in the feedback path. This block converts the output 1-bit digital signal from the quantizer to a corresponding time-difference signal to be fedback to input subtractor. The half period-delay is necessary to ensure that a full two-period delay is achieved around the loop as depicted in Fig. 20.

Fig. 22 shows the simulated power spectral densities (PSD) of the BPΔΣTDC and the ideal BPΔΣ modulator. The output spectrum in Fig. 22 shows the desired second-order noise shaping at 10.73 MHz IF. The input TM signal is a 1 ns_{pp}, 10.73 MHZ sinusoidal tone, and the simulated SNDR, SNR, and SFDR are 45.4 dB, 45.8 dB, and 49.6 dBc, respectively, while operating with 1.2 V voltage supply.

V. Experimental Results

The proposed BPΔΣTDC was fabricated in 130 nm IBM CMOS technology. Fig. 23 shows the chip micrograph and

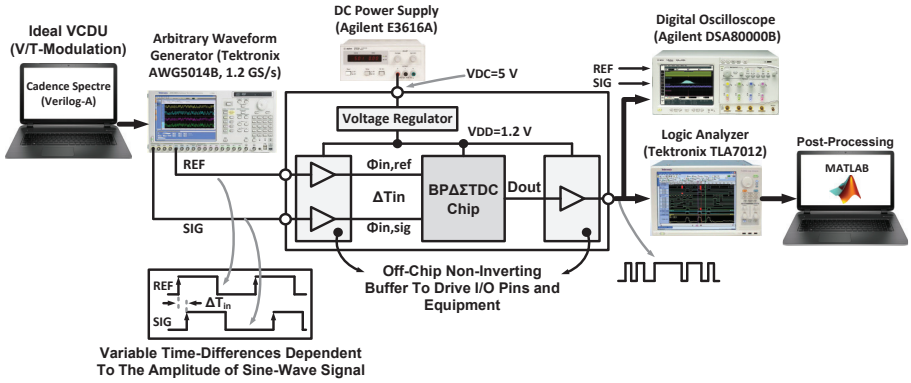

Fig. 25. Block diagram of the measurement setup.

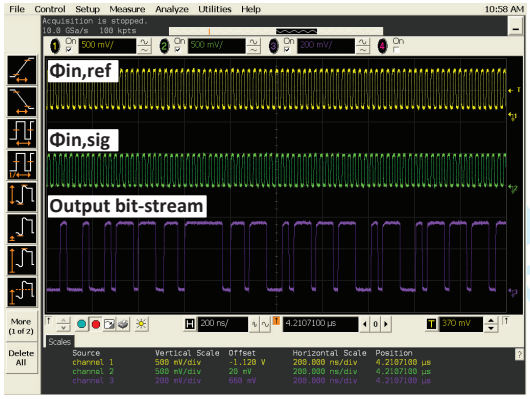

Fig. 26. Experimental time-domain waveforms of the input signals ($\Phi_{in,ref}$ and $\Phi_{in,sig}$) at sampling frequency 42.8 MHz and output bit-stream (D_{out}).

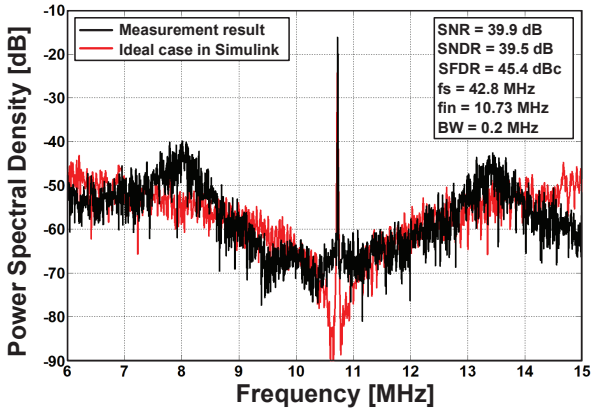

Fig. 27. Measured output spectrum of the BPΔΣTDC with a 10.73 MHz input signal and 42.8 MHz sampling frequency. Each of the output spectrum are averaged to reduce the variance of the PSD.

layout of the proposed TDC, which occupies the core size of 0.048 mm^2 (275.1 μm × 174.4 μm). The prototype chip is assembled in a 44-pin CQFP and mounted on a custom ten-layer PCB as shown in Fig. 24. Apart from the TDC chip marked with a white box, the test board included some features such as SMA connections to the input/output signals, non-inverting clock drivers (IDT ICS621) and a voltage regulator (Analog Devices ADP1706ARDZ-1.2). Bias voltages were derived from this reference voltage using resistor divider circuits, together with some 100 nF capacitors to suppressed any AC power-supply-related ripples. To reduce digital noise coupling into the power supplies network, the digital voltage supply lines were intentionally placed some distance away from the analog power lines. In addition, all power nets were decoupled with additional 100 nF capacitors. The other components seen on the PCB seen in Fig. 24 are not related to this TDC test and are used for other purposes.

A block diagram of the measurement setup used to characterize the prototype BPΔΣTDC is depicted in Fig. 25. The input TM signals ($\Phi_{in,ref}$ and $\Phi_{in,sig}$) were synthesized using an arbitrary waveform generator model Tektronix AWG5014B. The data loaded into the AWG5014B was created using Spectre by simulating an ideal VCDU with a conversion gain of 1 ns/V. The digital input to the VCDU was driven by a 1.2 V amplitude square wave operating at a frequency of 42.8 MHz. The voltage controlled input port was driven by a 1 V amplitude 10.73 MHz sine wave. The output phase-modulated voltage signal from the VCDU was then sampled at a rate of 42.8 Ms/s, then loaded into the AWG5014B to drive the PCB test setup. The digital output bit-stream, D_{out}, was captured by a logic analyzer (Tektronix TLA7012) and processed in MATLAB to extract the relevant parameters. In addition, digital oscilloscope (Agilent DSA80000B) was used to monitor the input signals of the TDC to ensure a stable constant sources (i.e., digital signals with variable time-differences and duty cycle of 50%). Fig. 26 shows a small portion of the input TM signals as seen on the scope, operating at 42.8 MHz frequency, as well as the output bit-stream of TDC. In the plot, the yellow and green traces are $\Phi_{in,ref}$ and $\Phi_{in,sig}$, respectively, and the output bit-stream signal D_{out} is displayed with a violet trace. As is evident, the input and output digital signals are operating at the expected data rate of 42.8 MHz with good rise and fall times.

The measured output PSD pre-processed with a Hanning window is shown in Fig. 27. The output spectrum shows a 20 dB/dec bandpass noise shaping characteristic corresponding to the behavior of a second-order BPΔΣTDC. The TDC achieved an SNR of 39.9 dB and an SNDR of 39.5 dB over a 0.2 MHz signal BW, resulting in an effective number of bits (ENOB) of 6.3 bits. This ENOB value is in good agreement with

TABLE I
PERFORMANCE SUMMARY OF THE PROPOSED BPΔΣTDC.

Specification	Measurement	Simulink
Technology	130-nm IBM CMOS	-
Order	Second	Second
Sampling frequency (f_s)	42.8 MHz	42.8 MHz
IF signal frequency (f_{in})	10.73 MHz	10.73 MHz
Signal bandwidth (f_{BW})	0.2 MHz	0.2 MHz
Input range (T_{range})	0-3.5 ns	-
Peak SNDR	39.5 dB	48.9 dB
Peak SNR	39.9 dB	48.9 dB
SFDR	45.4 dBc	61.5 dBc
ENOB	6.3 bits	7.8 bits
Supply voltage (V_{DD})	1.2 V	1.2 V
Power consumption	4.9 mW	-
BPΔΣTDC area	0.048 mm^2	-
Total chip area	1.0 mm × 1.0 mm	-

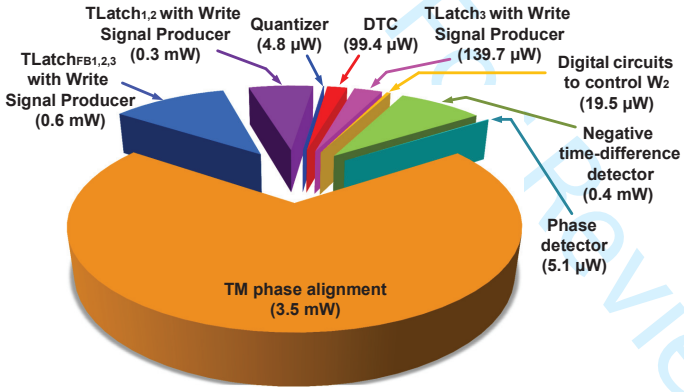

Fig. 28. Power breakdown of the prototype TDC.

7-bit circuit-level simulation prediction that corresponds to a 42 dB peak-SNDR. Table I shows a comparison between the measured performance of the prototype BPΔΣTDC and system-level design in MATLAB/Simulink. As is evident, the bandwidth of the measured prototype is the same as that predicted by simulation (in other words, the pole-zero positioning is correct). The measured signal-to-noise ratio performance metrics differ from the Simulink simulations results by about 10 dB. This we attribute to the additional noise sources related to the IC and PCB implementation which are not modeled in Simulink.

The TDC consumes a total power of 4.9 mW from the 1.2 V supply voltage at maximum sampling frequency of 42.8 MHz. Fig. 28 shows the breakdown in power consumption. The first two series TLatches (TLatch$_{1,2}$) consumes 6% of total power which includes the core of the TLatch and digital circuits to produce their write signals. TLacth,$_{FB1,2,3}$ and TLatch$_3$ as well as their Write Signal Producers consume 11% and 3%, respectively. The negative time-difference detector consumes 8%, and digital circuits shown in Fig. 18(a) (two multiplexers and a digital OR gate) and phase detector consume power less than 1%. Due to complexity of TM phase alignment in time shifting of Φ_{PD} signal, this circuit consumes 69% of the total power. While the power consumption on the VCDU-based DTC and quantizer are only 2% and <1%,

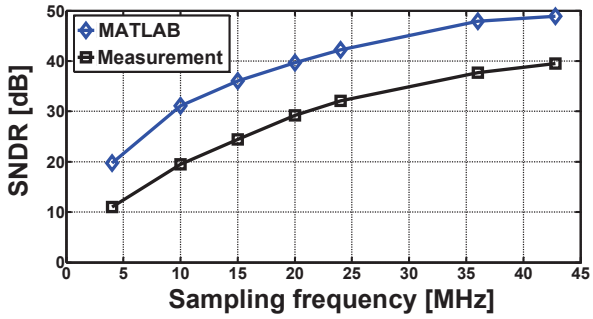

Fig. 29. MATLAB and Measured SNDR for different sampling frequency ($f_{in} = f_s/4$) with BW=0.2 MHz.

respectively. It should be noted that the power consumption of the BPΔΣTDC can be reduced further using innovative circuit design solutions now that the circuits proposed in this work have been validated. This is the subject of future work.

In order to verify the capability of the BPΔΣTDC over a wide range of reference clock frequencies, the above setup was utilized. The measured SNDR value versus the sampling frequency with a 0.2 MHz bandwidth and $f_{in} = f_s/4$ is shown in Fig. 29. When the sampling frequency is greater than 36 MHz, the SNDR is still greater than 37 dB, thanks to TM phase alignment and synchronization technique. Further decreasing the sampling frequency degrades the SNDR due to reduced the OSR.

VI. CONCLUSION

In this paper, we have successfully implemented the very first prototype of a BPΔΣTDC with second-order noise shaping with a peak SNDR of 39.5 dB over a 0.2 MHz bandwidth centered around 10.7 MHz. The key building blocks of the proposed TDC include a TM LDI-based resonator, an all-digital DTC, a TM subtractor circuit capable of subtracting negative time-difference values and an adaptive delay circuit that can compensate for process variations. The adaptive delay circuit enabled the sampling frequency to be adjusted from 4 MHz to 42.8 MHz with a notch frequency equal to one-quater of the sampling clock. The performance of the BPΔΣTDC was best at the highest sampling rate of 42.8 MHz. To conclude, this paper has demonstrate a BPΔΣTDC which is compact, efficient, and accurate that can be easily adopted into a new CMOS technologies under low supply voltage conditions. It is believed this work can be applied to the design of high-order BPΔΣTDC with a MASH structure.

REFERENCES

[1] I. Vornicu and R. Carmona-Galan and A. Rodriguez-Vazquez, "Arrayable Voltage-Controlled Ring-Oscillator for Direct Time-of-Flight Image Sensors," *IEEE Trans. on Circuits and Systems I: Regular Papers*, vol. 64, no. 11, pp. 2821–2834, Nov 2017.
[2] K. Nose, M. Kajita, and M. Mizuno, "A 1-ps Resolution Jitter-Measurement Macro Using Interpolated Jitter Oversampling," *IEEE J. of Solid-State Circuits*, vol. 41, no. 12, pp. 2911–2920, Dec 2006.
[3] H. Chen, Y. Zhang, and D. D. U. Li, "A Low Nonlinearity, Missing-Code Free Time-to-Digital Converter Based on 28-nm FPGAs With Embedded Bin-Width Calibrations," *IEEE Trans. on Instrumentation and Measurement*, vol. 66, no. 7, pp. 1912–1921, July 2017.

[4] R. Avivi and M. Kerner and E. Shumaker and G. L. Puma and T. Sela and L. Sofer and G. Horovitz, "Adaptive Spur Cancellation Technique in All-Digital Phase-Locked Loops," *IEEE Trans. on Circuits and Syst. II: Express Briefs*, vol. 64, no. 11, pp. 1292–1296, Nov 2017.

[5] S. Naraghi, M. Courcy, and M. P. Flynn, "A 9-bit, 14 μW and 0.06 mm^2 Pulse Position Modulation ADC in 90 nm Digital CMOS," *IEEE J. of Solid-State Circuits*, vol. 45, no. 9, pp. 1870–1880, Sept 2010.

[6] J. Daniels, W. Dehaene, M. S. J. Steyaert, and A. Wiesbauer, "A/D Conversion Using Asynchronous Delta-Sigma Modulation and Time-to-Digital Conversion," *IEEE Trans. on Circuits and Syst. I: Regular Papers*, vol. 57, no. 9, pp. 2404–2412, Sept 2010.

[7] S. Ziabakhsh and G. Gagnon and G. W. Roberts, "The Peak-SNR Performances of Voltage-Mode versus Time-Mode Circuits: the PMOS-NMOS Stack Use Case," *IEEE Transactions on Circuits and Systems II: Express Briefs*, pp. 1–5, 2018.

[8] K. Kim, Y. H. Kim, W. Yu, and S. Cho, "A 7 bit, 3.75 ps Resolution Two-Step Time-to-Digital Converter in 65 nm CMOS Using Pulse-Train Time Amplifier," *IEEE J. of Solid-State Circuits*, vol. 48, no. 4, pp. 1009–1017, April 2013.

[9] J. P. Jansson, A. Mantyniemi, and J. Kostamovaara, "Synchronization in a Multilevel CMOS Time-to-Digital Converter," *IEEE Trans. on Circuits and Syst. I: Regular Papers*, vol. 56, no. 8, pp. 1622–1634, Aug 2009.

[10] P. Chen, S.-L. Liu, and J. Wu, "A CMOS Pulse-Shrinking Delay Element For Time Interval Measurement," *IEEE Trans. on Circuits and Syst. II: Analog and Digital Signal Processing*, vol. 47, no. 9, pp. 954–958, Sep 2000.

[11] P. Lu, A. Liscidini, and P. Andreani, "A 3.6 mW, 90 nm CMOS Gated-Vernier Time-to-Digital Converter With an Equivalent Resolution of 3.2 ps," *IEEE J. of Solid-State Circuits*, vol. 47, no. 7, pp. 1626–1635, July 2012.

[12] L. Vercesi, A. Liscidini, and R. Castello, "Two-Dimensions Vernier Time-to-Digital Converter," *IEEE J. of Solid-State Circuits*, vol. 45, no. 8, pp. 1504–1512, Aug 2010.

[13] J. Yu and F. F. Dai, "A 3-Dimensional Vernier Ring Time-to-Digital Converter in 0.13 μm CMOS," in *IEEE Custom Integrated Circuits Conf. 2010*, September 2010, pp. 1–4.

[14] G. W. Roberts and M. Ali-Bakhshian, "A Brief Introduction to Time-to-Digital and Digital-to-Time Converters," *IEEE Trans. on Circuits and Syst. II: Express Briefs*, vol. 57, no. 3, pp. 153–157, March 2010.

[15] J. Yu, F. F. Dai, and R. C. Jaeger, "A 12-Bit Vernier Ring Time-to-Digital Converter in 0.13 μm CMOS Technology," *IEEE J. of Solid-State Circuits*, vol. 45, no. 4, pp. 830–842, April 2010.

[16] B. Young, S. Kwon, A. Elshazly, and P. K. Hanumolu, "A 2.4 ps Resolution 2.1 mW Second-Order Noise-Shaped Time-to-Digital Converter With 3.2 ns Range in 1MHz Bandwidth," in *IEEE Custom Integrated Circuits Conf. 2010*, Sept 2010, pp. 1–4.

[17] M. Gande, N. Maghari, T. Oh, and U. K. Moon, "A 71dB Dynamic Range Third-Order $\Delta\Sigma$ TDC Using Charge-Pump," in *2012 Symposium on VLSI Circuits (VLSIC)*, June 2012, pp. 168–169.

[18] M. Straayer and M. Perrott, "A Multi-Path Gated Ring Oscillator TDC With First-Order Noise Shaping," *IEEE J. of Solid-State Circuits,*, vol. 44, no. 4, pp. 1089–1098, April 2009.

[19] W. Yu, K. Kim, and S. Cho, "A 0.22 ps_{rms} Integrated Noise 15 MHz Bandwidth Fourth-Order Delta-Sigma Time-to-Digital Converter Using Time-Domain Error-Feedback Filter," *IEEE J. of Solid-State Circuits*, vol. 50, no. 5, pp. 1251–1262, May 2015.

[20] A. Elshazly, S. Rao, B. Young, and P. K. Hanumolu, "A Noise-Shaping Time-to-Digital Converter Using Switched-Ring Oscillators-Analysis, Design, and Measurement Techniques," *IEEE J. of Solid-State Circuits*, vol. 49, no. 5, pp. 1184–1197, May 2014.

[21] M. Ali-Bakhshian and G. Roberts, "A Digital Implementation of a Dual-Path Time-to-Time Integrator," *IEEE Trans. on Circuits and Syst. I: Regular Papers,*, vol. 59, no. 11, pp. 2578–2591, Nov 2012.

[22] S. Ziabakhsh and G. Gagnon and G. W. Roberts, "A Time-Mode LDI-Based Resonator for a Band-Pass $\Delta\Sigma$ TDC," in *2017 IEEE 60th Int. Midwest Symposium on Circuits and Systems (MWSCAS)*, Aug 2017, pp. 1296–1299.

[23] M. Abdelfattah and G. W. Roberts, "All-Digital Time-Mode Direct-Form All-Pole Biquadratic Filter Realization," *IEEE Trans. on Circuits and Systems II: Express Briefs*, vol. 64, no. 11, pp. 1262–1266, Nov 2017.

[24] C. Taillefer and G. Roberts, "Delta-Sigma A/D Conversion Via Time-Mode Signal Processing," *IEEE Trans. on Circuits and Syst. I: Regular Papers,*, vol. 56, no. 9, pp. 1908–1920, Sept 2009.

[25] S. Ziabakhsh, G. Gagnon, and G. Roberts, "Wide Linear Range Voltage-Controlled Delay Unit For Time-Mode Signal Processing," in *IEEE Int. Symp. on Circuits and Systems (ISCAS)*, May 2015, pp. 1826–1829.

[26] X. Haurie and G. W. Roberts, "A Multiplier-Free Structure for 1-Bit High-Order Digital Delta-Digma Modulators," in *38th Midwest Symposium on Circuits and Systems. Proceedings*, vol. 2, Aug 1995, pp. 889–892 vol.2.

[27] I. Lee and G. Han and Y. Chae, "A 2 mW, 50 dB DR, 10 MHz BW 5 $times$ Interleaved Bandpass Delta-Sigma Modulator at 50 MHz IF," *IEEE Trans. on Circuits and Syst. I: Regular Papers*, vol. 62, no. 1, pp. 80–89, Jan 2015.

Soheyl Ziabakhsh (S'13) received the M.Sc. degree in electrical engineering from the University of Guilan, Iran in 2009. He is currently working toward his Ph.D. degree in the Department of Electrical Engineering at École de technologie supérieure (É TS), Montreal, Canada. His main research interests include high-speed time-domain data converters and low-power analog/mixed-signal circuit design.

Ghyslain Gagnon (M'08) received the Ph.D. degree in electrical engineering from Carleton University, Canada in 2008. He is now an Associate Professor at École de technologie supérieure, Montreal, Canada. He is an executive committee member of ReSMiQ and Director of research laboratory LACIME, a group of 13 Professors and nearly 100 highly-dedicated students and researchers in microelectronics, digital signal processing and wireless communications. Highly inclined towards research partnerships with industry, his research aims at mixed-signal CMOS IC design, digital signal processing and machine learning with various applications, from media art to building energy management.

Gordon W. Roberts (S'85-M'85-SM'02-F'04) received the B.A.Sc. degree in electrical engineering from the University of Waterloo, Waterloo, ON, Canada, in 1983, and the M.A.Sc. and Ph.D. degrees in electrical engineering from the University of Toronto, Toronto, ON, in 1986 and 1989, respectively.

He is currently a Full Professor with McGill University, Montreal, QC, Canada, where he is also the James McGill Chair in Electrical and Computer Engineering. He has co-authored seven textbooks related to analog IC design and mixed-signal test. He has authored numerous papers in scientific journals and conferences, and has contributed chapters to various industrially focused textbooks. He is named on 14 patents, with 4 pending.

Dr. Roberts held many administration roles within various conference organizations such as the International Test Conference, the Custom Integrated Circuit Conference, the Design Automation Conference, and the International Symposium on Circuits and Systems. He was the 2009 and 2013 General Chair of the International Test Conference. He was the recipient of numerous department, faculty, and university awards for teaching test and electronics to undergraduates and was also a recipient of several IEEE awards for his work on mixed-signal testing.