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A Design Methodology for Wideband Current-Reuse Receiver Front-Ends Aimed at Low-Power Applications

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Abstract: This work gives a design perspective on low-power and wideband RF-to-Baseband current-reuse receivers (CRR). The proposed CRR architecture design shares a single supply and biasing current among both LNTA and baseband circuits to reduce power consumption. The work discusses topology selection and a suitable design procedure of the low noise transconductance amplifier (LNTA), down-conversion passive-mixer, active-inductor (AI) and TIA circuits. Layout considerations are also discussed. The receiver was simulated in 130 nm CMOS technology and occupies an active area of 0.025 mm^2. It achieves a wideband input matching of less than −10 dB from 0.8 GHz to 3.4 GHz. A conversion-gain of 39.5 dB, IIP3 of −28 dBm and a double-sideband (DSB) NF of 5.6 dB is simulated at a local-oscillator (LO) frequency of 2.4 GHz and an intermediate frequency (IF) of 10 MHz, while consuming 1.92 mA from a 1.2 V supply.

Keywords: current-reuse receiver; common gate; common source; low power; current sharing; low noise

Citation: Abbasi, A.; Nabki, F. A Design Methodology for Wideband Current-Reuse Receiver Front-Ends Aimed at Low-Power Applications. *Electronics* **2022**, *11*, 1493. https://doi.org/10.3390/electronics11091493

Academic Editors: João Paulo Pereira do Carmo, Subhanshu Gupta, Kunhee Cho and Anna Richelli

Received: 28 February 2022
Accepted: 2 May 2022
Published: 6 May 2022

1. Introduction

The fast growing Internet of Things (IoT) is creating smart environments that have the potential to significantly improve our quality of life. This includes IoT systems used in location tracking and positioning, such as vehicles or drones for navigation, home automation, in the health industry to monitor patients and in agriculture to optimize and control watering systems, etc. This requires IoT devices with low power consumption, which will translate into billions of IoT devices that will require significant aggregate power consumption to operate. Accordingly, reducing the power consumption in each IoT device by a fraction can lead to an important overall energy use reduction globally.

Notably, in a typical IoT module, the RF transceiver plays a significant role in defining the overall power consumption of a given system. This work thus aims at giving insights regarding how to reduce the power consumption of RF transceivers. There are several techniques to reduce the power consumption of RF transceivers, including current sharing of the baseband and RF front-end by stacking a transimpedance amplifier (TIA) on top of the low transconductance amplifier (LNTA) and mixer, which is very effective compared to the conventional technique that cascades the LNTA, mixer and TIA.

There have been a wide range of studies into current-reuse techniques for RF receivers, leading to the introduction of the current-reuse receiver (CRR) architecture. Conventionally, in such receivers, current-reuse is employed in the LNTA design to boost the transconductance by stacking both PMOS and NMOS transistors and sharing their current bias through a single supply [1]. Recently, the current-reuse technique has been applied to receiver design by stacking several blocks such as the LNTA, mixer and TIA and sharing the biasing current among all of these circuits. In this fashion, power consumption can be reduced significantly. In [2], a voltage-controlled oscillator (VCO), mixer and LNTA are stacked to share the biasing current from a single supply. This reduces the overall power consumption significantly, but the design suffers from a high noise figure (NF) and

VCO injection locking. Similarly, in [3], VCO and LNA are stacked, thus reducing the power consumption at the price of narrowing the bandwidth, potentially becoming prone to VCO injection locking as in [2]. A balun LNA, active mixer and hybrid baseband filter are stacked in [4] to form a current-reuse topology to reduce power consumption. However, the active-mixer consumes voltage headroom, which reduces linearity. Another approach is the function-reuse technique employed in [5], where a push–pull amplifier is used to function as both the LNTA and TIA. However, a poor linearity of -50 dBm due to the low supply voltage is reported. Moreover, this approach is suitable for sub-GHz applications only. In [6], a current-reuse receiver using an N-path passive mixer for input matching and an active mixer for down-conversion is used. This topology needs additional voltage headroom for its active mixer, increasing its supply voltage requirement. Moreover, it requires an additional circuit to combine the N paths, consuming additional power. Another approach introduces the $1/f$ noise-cancellation (NC) technique. However, it consume a high power of 8 mW [7]. Another alternative in [8] utilizes both input matching and a $1/f$ NC technique and reports a low NF of 1.94 dB at the cost of very narrow bandwidth. The same current-reuse receiver architecture is employed in [9] but utilizes a cross-coupled common-gate (CCCG) LNTA topology to enhance the operating bandwidth. However, both [8,9] suffer from the loading effect on the RF signal due to the sharing of the passive mixer input and receiver output nodes. A quadrature RF-to-BB current-reuse receiver is proposed in [10], which comprises the architecture from [8]. It reports a very high NF of 13.2 dB despite using a common-source LNTA topology with a low noise contribution and narrow bandwidth. In [11], the concept of an active-inductor (AI) was introduced, and this was used in our earlier works [12] to overcome the issues mentioned above.

In order to provide design insights into low-power CRR circuits, this work provides a design procedure, characterization and more depth into the design methodology behind the circuit proposed in our earlier work [12]. It includes the topology selection and design of the LNTA, down-conversion mixer and active-inductor (AI). The concept and design of the TIA is described as well. The paper provides all of the design steps and test benches required, along with the mathematical calculations necessary for the design. The paper is structured as follows. Section 2 overviews the design steps and test benches of the circuit implementation, Section 3 presents system integration considerations, Section 4 discusses circuit layout aspects, and Section 5 presents the post-layout simulation results of the resulting design and discusses them.

2. RF-to-BB Current-Reuse Receiver Front-End Circuit Level Design

Thanks to the CMOS scaling, which reduces the threshold voltage of the transistors, V_{TH}, and increases their frequency of operation (i.e., transition frequency ω_T or f_T), the stacking of several circuits sharing a single supply is possible. However, this introduces design challenges, which are discussed in [12]. The current-reuse receiver (CRR) block diagram proposed in [12] is shown in Figure 1. In this section, the detailed design steps, test benches and topology selections are discussed.

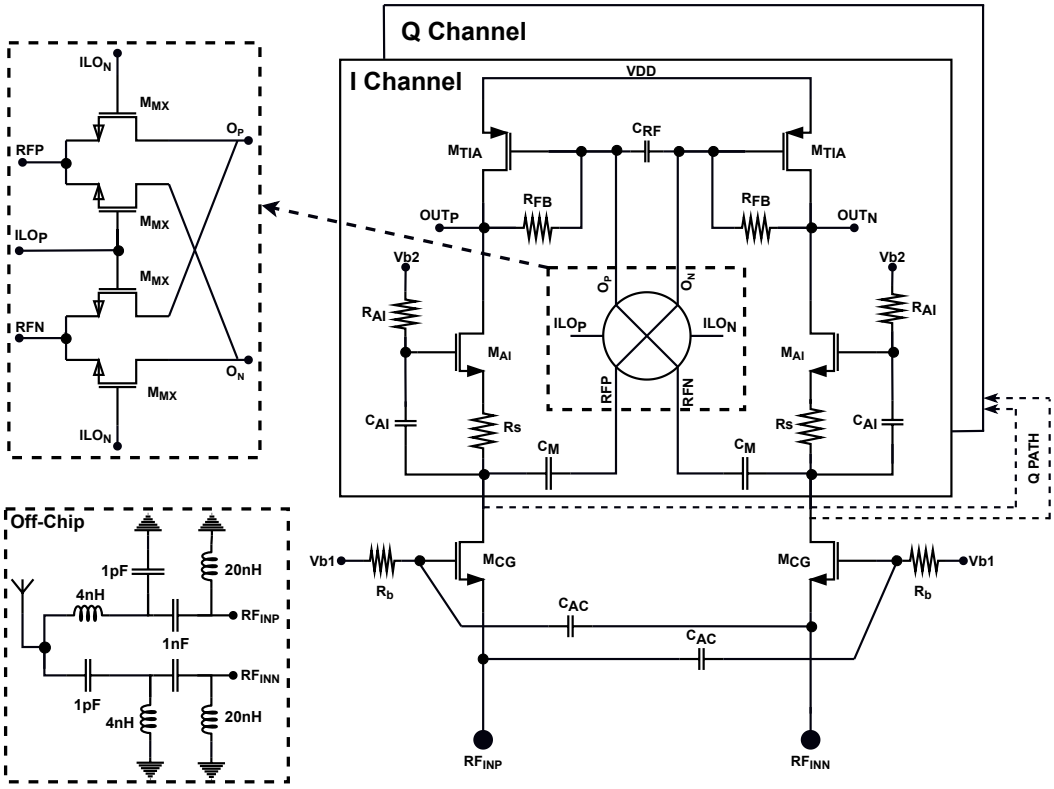

Figure 1. Block diagram of the proposed current-reuse receiver. Adapted with permission from Ref. [12]. Copyright 2022 Frederic Nabki.

2.1. Low Noise Transconductance Amplifier

In CRR front-ends, the LNTA plays a significant role in defining the overall performance of the CRR, such as its sensitivity, input matching and power consumption. There are two well-known LNTA topologies that can be employed: common-source (CS) and common-gate (CG). The common-source topology is suitable for very low-noise applications, where the noise-figure (NF) is given by [13]

$$NF_{CS} = 1 + g_m R_S \gamma \left(\frac{\omega_o}{\omega_T}\right)^2, \tag{1}$$

where g_m is the transconductance, R_S is the source impedance, γ is the channel effect, ω_o is the operating frequency, and ω_T is related to the maximum frequency at which that transistor can operate effectively (i.e., transition frequency). Equation (1) shows that a higher ω_T results in a very low NF in the CS LNTA topology. The NF in CG topology is given by

$$NF_{CG} = 1 + \frac{\gamma}{g_m R_s}. \tag{2}$$

It is undeniable that the CG topology achieves much higher NF (>3 dB) than the CS topology since the second term in Equation (1) is suppressed by ω_T when $\omega_T \gg \omega_o$. On the other hand, the CG topology is more suitable for wideband applications, while the CS topology results in narrow-band input impedance matching. The input impedance considering the CS LNTA is given by

$$Z_{CS} = s(L_g + L_s) + \frac{1}{s(C_{gs} \parallel C_{par})} + \omega_T L_s, \tag{3}$$

where L_g is a series gate inductor, L_s is an source-degeneration inductor, C_{gs} is the gate to source capacitance, and C_{par} is the parasitic capacitance considering the input of the LNTA, such as the pad and ESD cell capacitance. Equation (3) shows that the CS topology is

suitable for narrow-band applications. On the other hand, the input impedance considering the CG LNTA is calculated by $1/g_m$ which is a real impedance. Hence, the CG LNTA topology is very suitable for wideband applications as it can be readily matched to the antenna (e.g., 50 Ω). Thus, topology selection for the LNTA depends on the application requirements. The receiver in [12] requires a wideband operation to cover a wide range of frequencies for several wireless standards; hence, the CG topology is suitable for this goal at the cost of a higher NF compared with the CS topology.

The LNTA design begins with an optimization of g_m and f_T. Figure 2a shows a test bench utilized to optimize and characterize g_m and f_T. Less than half of the supply voltage is applied to the drain terminal, which is close to the voltage that is expected after the receiver integration. The simulation is performed by sweeping the biasing current (I_{ds}) while the width over length ratio (W/L) is maintained at constant value. To observe the channel-length effect, W and L are increased with a scaling coefficient from W/L to 5W/5L, resulting in the plots shown in Figure 2b,c. This shows that, by increasing the current for a given W/L, both g_m and f_T increase to a certain value until they flatten. The short channel effect can be reduced by increasing L. Thus, by increasing both W and L by the same scaling factor, g_m improves. However, f_T reduces due to the increase in gate-source and gate-drain capacitance. In the CG topology, f_T is not the main contributor in the NF equation, but it is preferred to maintain it to be at least 10 times higher than the operating frequency to avoid any non-idealities such as oscillations. In this case, a scaling factor of 2 (i.e., 2W/2L) is selected. To achieve the required g_m for input matching, both the width and the current need to increase. This can lead the circuit to consume high power. One approach to reduce the power consumption is to use the capacitive cross-coupling technique to boost the transconductance by a factor of 2. In this way, half of the current is required to achieve the required g_m. The LNTA requires a current path to ground, and this can be achieved using either a resistor or inductor. In [12], an inductor is used to reduce the voltage headroom requirement and the RF signal loss by resonating with the parasitic capacitance. Note that further device optimization will need to be performed after receiver integration.

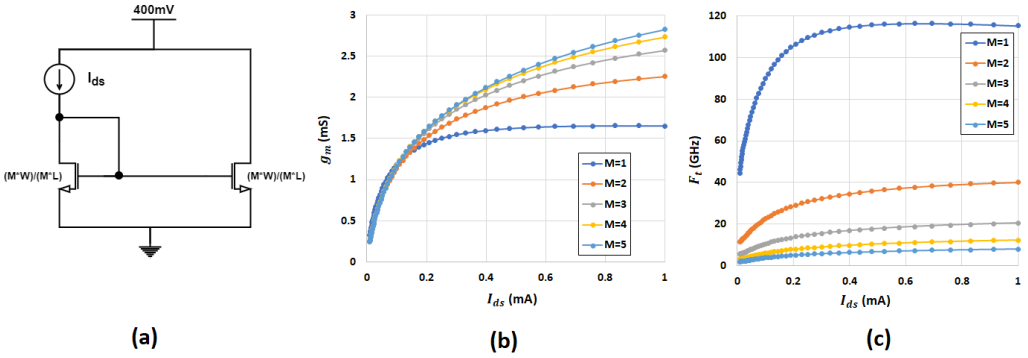

Figure 2. (**a**) Test bench to optimize and characterize g_m and f_T, (**b**) resulting g_m plots, and (**c**) resulting f_T plots.

A single-ended antenna input needs to be converted to a differential signal at the input of the receiver. Both single to differential and LC baluns can be used. An LC-balun achieves a lower NF than a differential balun at the cost of a narrower bandwidth, but its combination with a CG LNTA topology provides wide bandwidth. Moreover, an LC-balun is able to convert the antenna impedance to any impedance considering the LNTA by adjusting the L and C values. This gives more flexibility to the design and allows it to operate at higher g_m.

2.2. Down-Conversion Mixer

There are two choices of down-conversion mixers: active and passive. A passive mixer is preferred over an active mixer since active mixers require voltage headroom, which is not

desirable due to the resulting poor linearity performance. Moreover, low-frequency noise can be filtered out using an AC-coupling capacitor at the input of the passive mixer. Thus, in [12], a passive mixer is used to down-convert the RF signal to the IF. A double-balanced passive mixer, as shown in Figure 1, is used. To design the mixer switches and optimize the W/L ratio, where L is minimum, a test bench that models the receiver front-end is employed as shown in Figure 3. In this test bench, the LNA and TIA are ideal macro-models. A voltage controlled current source (VCCS) is used to convert the RF voltage to the RF current to perform as an LNTA. The LNTA output impedance is modeled by R and C. R_1, C_1 and an OpAmp model define the TIA macromodel. The design of the mixer switches is performed by sweeping the value of the W/L ratio and the gate voltage of the mixer switches concurrently in order to achieve the best NF and linearity. Figure 4 shows the NF and 1 dB compression point (P1dB) performance versus the W/L ratio and the gate voltage of the switches, VCM. The best integrated double side band noise figure (DSBNF), from 1 MHz to 10 MHz, is achieved at a VCM of 800 mV, while the P1dB at 600 mV is 1.4 dB higher than at a VCM of 800 mV. Very large mixer switches need to be avoided to minimize large parasitic capacitors at the input of the mixer that attenuate the RF signal and cause LO to RF leakage. Thus, a W/L ratio of 35 µm/130 nm is selected as a suitable trade-off value. Moreover, the gate voltage should be below the breakdown of the transistors when the LO signal switches high or low. Final optimization is needed after receiver integration.

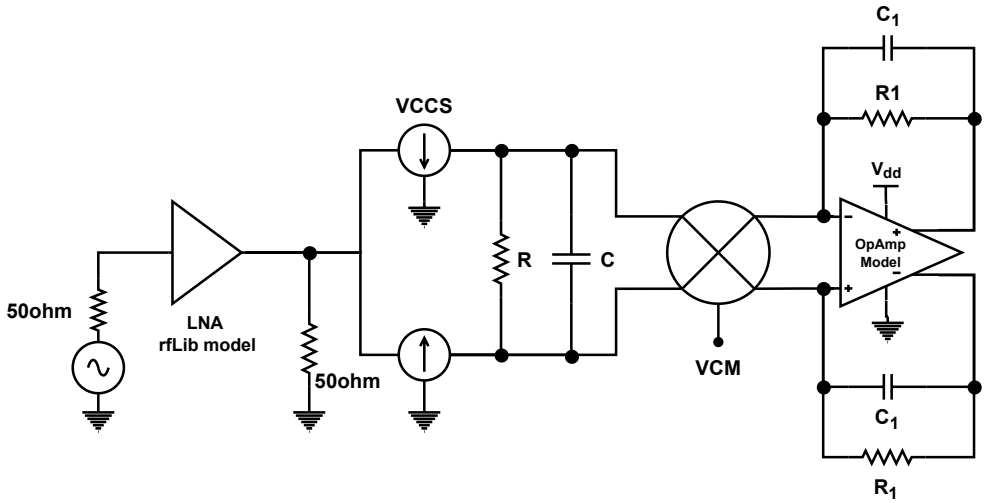

Figure 3. Test bench to design and optimize the down-conversion mixer switches.

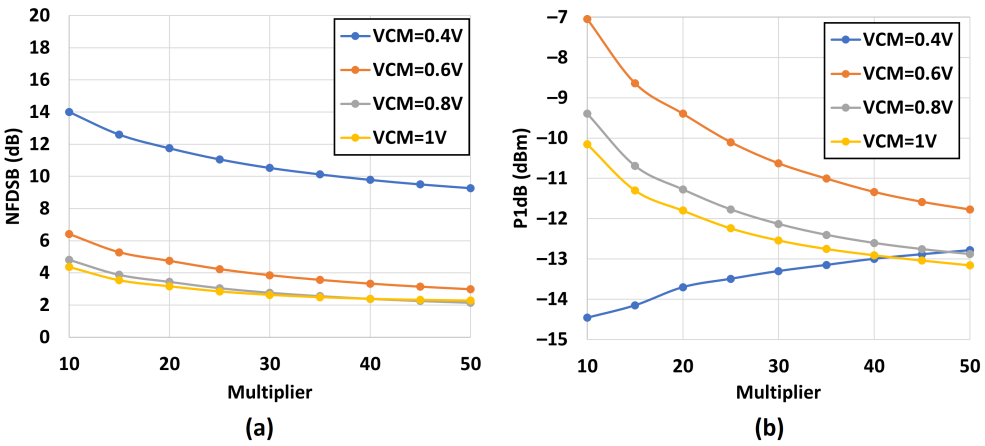

Figure 4. (**a**) The noise figure and (**b**) the 1 dB compression point versus the W/L ratio for different gate voltages of the input transistors.

2.3. Active Inductor and Noise Cancellation

In [8], the mixer input and receiver output share the same node, which causes RF signal losses. As a result, the design is not able to operate at very high frequency and is more suitable to sub-GHz applications. In our earlier works [12], the concept of an AI was introduced. In this design, cascoded devices are used to boost the output impedance, as shown in Figure 1 (M_{AI}). The impedance considering the AI circuit, Z_{AI}, by ignoring M_{NC} since it is in parallel, is summarized and given by

$$Z_{AI}(s) \cong \frac{g_{m,AI}R_S(R_{AI}C_{AI}s+1)+R_{AI}C_{AI}s}{g_{m,AI}R_SC_{AI}s+g_{m,AI}+C_{AI}s} || \frac{1}{sC_{par}}, \quad (4)$$

where C_{par} is the parasitic capacitance at the mixer input and is related to the technology node.

The impedance from the LNTA to the AI is very small at lower frequencies and increases at higher frequencies. This helps to isolate the RF signal from the output node. In this case, the mixer input connects to the LNTA output directly, where the majority of the RF signal flows through the mixer input due to the lower input impedance compared to that of the AI.

Figure 5a shows the test bench to design the AI circuit. The AI circuit includes M_{AI}, R_{AI} and C_{AI}. R_S is used to boost the impedance at higher frequencies. A small value is considered to avoid excessive voltage headroom usage. M_{TIA} and R_{FB} are used to model the TIA circuit. R_{AI} and C_{AI} should be optimized to define the cut-off frequency. The transconductance of M_{AI} defines the impedance of the AI at DC and low frequencies. A small signal, I_{AC}, is applied to the input of the AI circuit, and V_{AC}/I_{AC} is calculated to extract the input impedance of the AI circuit, Z_{AI}. Figure 5b illustrates the magnitude of Z_{AI} versus the frequency with and without R_S being considered. It is obvious that R_S helps to boost the AI input impedance at the cost of voltage headroom. Thus, there is a trade-off between the NF and linearity when the value of R_S is defined. The gate terminal of M_{AI} needs to be biased with a voltage, V_b, of 800 mV to keep it in saturation.

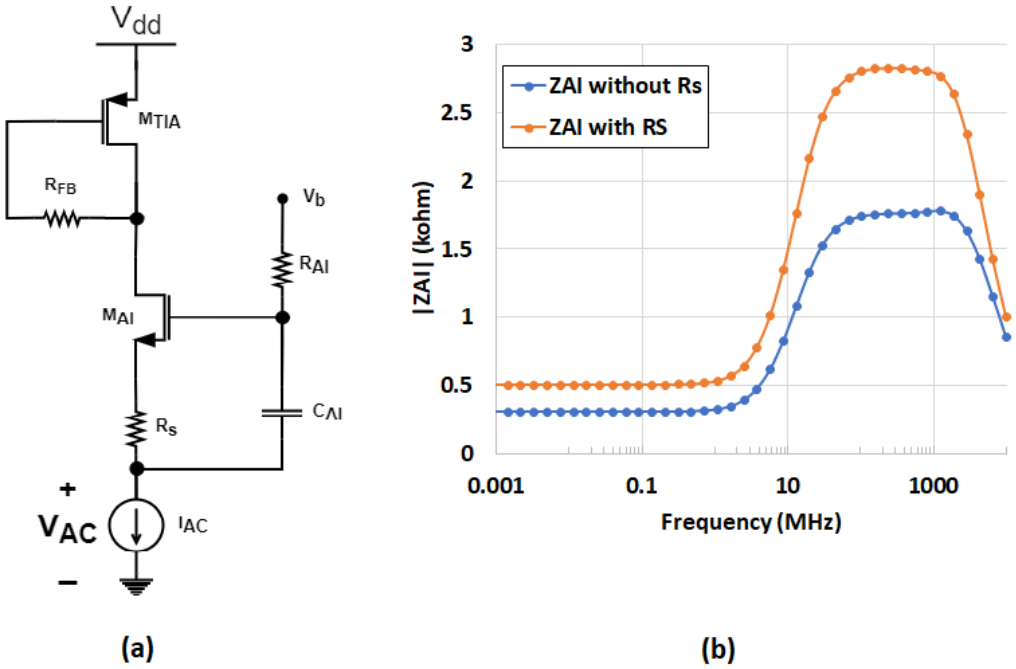

Figure 5. (**a**) Test bench to design the active inductor and (**b**) its impedance magnitude over frequency with and without R_S considered.

The magnitude of Z_{AI} is shown for different C_{AI} values in Figure 6. This illustrates that a higher C_{AI} value pushes the cutoff frequency of Z_{AI} to a lower frequency and increases

its magnitude at high frequency, while it remains constant at lower frequencies. A value for C_{AI} of 1 pF shows a good trade-off value between the frequency cutoff and maximal impedance magnitude. Another step in the design of the AI circuit is to select the best W/L ratio of M_{AI}. Figure 7 shows that increasing the W/L ratio of M_{AI} with the multiplier from 2 to 8 leads to a higher g_m and a lower Z_{AI} magnitude at lower frequencies. A W/L ratio of M×10 µm/260 nm, where M is equal to 4, is selected as a good trade-off between low-frequency and high-frequency impedance behavior.

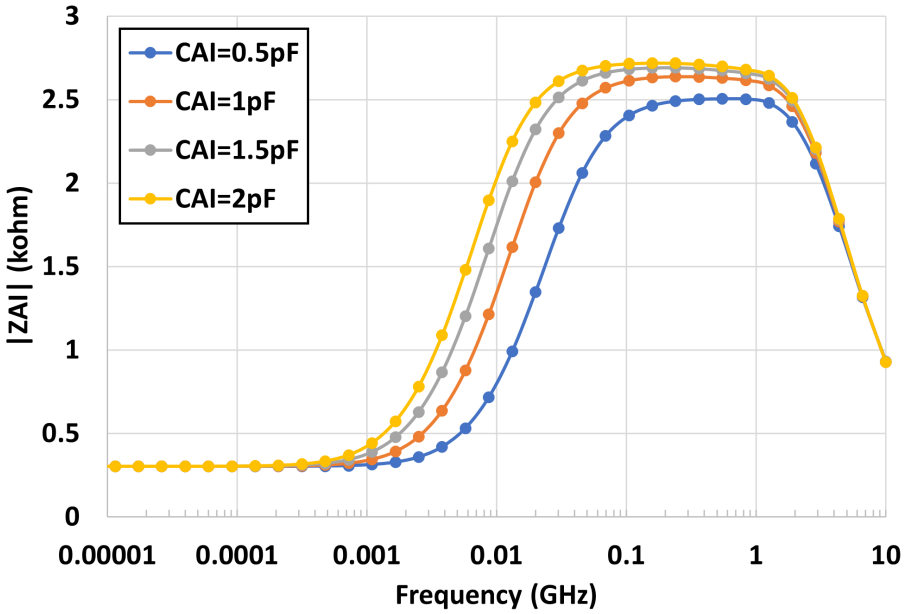

Figure 6. Magnitude of Z_{AI} for different values of C_{AI}.

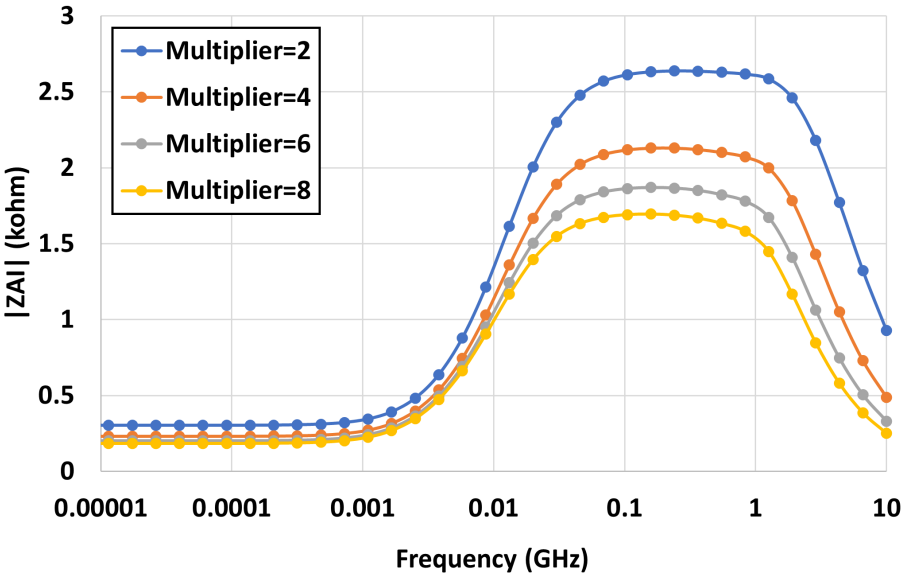

Figure 7. Magnitude of Z_{AI} for different W/L ratio multipliers of transistor M_{AI}. The unit W/L ratio is 10 µm/260 nm.

Final component value fine tuning can be performed after receiver integration.

2.4. Transimpedance Amplifier

The final step is to design the baseband (BB) circuit in the CRR front-end where the BB current needs to be converted to a BB voltage at the output. In [8,12], a TIA is

designed using a single transistor with a feedback resistor, R_{FB}, shown in Figure 1. A large channel-length value should be used to enhance the TIA output impedance. The impedance considering the TIA is defined by $1/g_m$ of M_{TIA}. The conversion gain is approximately calculated through the following relation:

$$Conv.Gain \cong \frac{2\sqrt{2}}{\pi} g_{m,eff} R_{FB}. \quad (5)$$

where $g_{m,eff}$ is $2 \times g_m$ of transistor M_{CG} thanks to the capacitive cross-coupling technique, which boosts the g_m by almost two times. R_{FB} should be large enough to achieve the required conversion gain. The output common-mode voltage can be slightly higher than half of the supply voltage in order to provide more voltage headroom for the AI and LNTA circuits. A value for C_{RF} of 1 pF is used to remove high-frequency components at the output of the mixer right before the TIA input.

After all of the aforementioned circuits are integrated within the CRR structure, an optimization needs to be performed by small adjustments to the component values in order to achieve the best possible performance.

3. System Integration

CRR Front-End

The design of each circuit part of the CRR has been discussed in Section 2, which covered the design choices, theoretical analysis, design flow and test benches. The sub-blocks need to be integrated as shown in Figure 1 to form the CRR front-end. This includes the LNTA with external LC-balun to convert RF voltage to current, a passive mixer to convert the RF signal to a baseband current, a TIA to convert the baseband current to a voltage at the output and finally the AI circuit to isolate the RF signal from the output in order to reduce the RF signal loss.

The TIA, AI and LNTA are cascoded to share a single supply of 1.2 V. The performance of the CRR front-end should be verified through simulations versus several design metrics such as biasing voltages to make sure the design is robust. This begins with the NF and CG performance versus the gate voltage biasing of the LNTA, as shown in Figure 8. This illustrates that a voltage bias of 365–375 mV achieves almost a constant conversion gain and NF performance. The performance starts to degrade at higher biasing voltages due to the resulting poor input matching, as shown in Figure 9 and voltage headroom limitation. The S_{11} starts degrading at biasing voltages above 380 mV since g_m increases due to the larger device current stemming from the increase in V_{GS}.

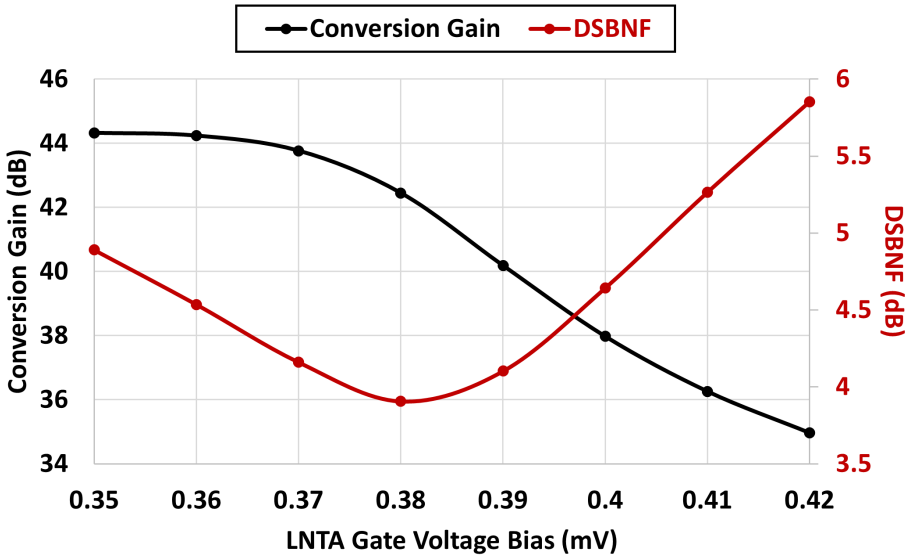

Figure 8. The NF and conversion gain versus the gate bias voltage of the LNTA.

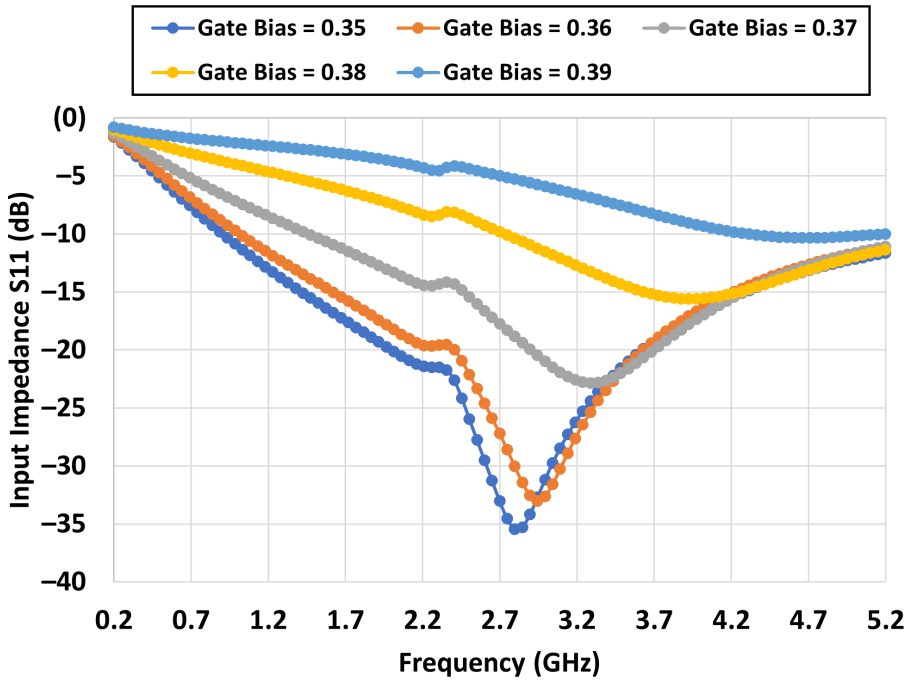

Figure 9. The input matching (S_{11}) versus frequency for several gate bias voltages of LNTA.

It is important to optimize the gate biasing voltage of the mixer switches. Figure 10 shows the NF and conversion gain of the CRR front-end versus the gate biasing of the mixer switches. It shows a flat conversion gain and NF performance versus a wide rage of biasing from 0.6 V to 0.9 V, which is beneficial to compensate for bias variations.

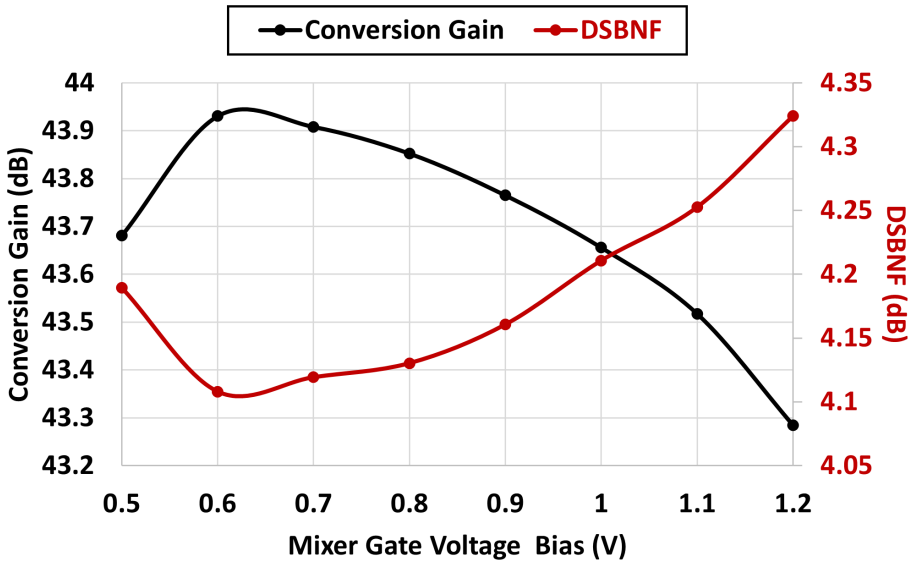

Figure 10. The NF and conversion gain versus the gate bias voltage of the mixer.

The performance of the CRR front-end needs to be verified across a wide supply voltage range since the current-reuse architecture depends on the available voltage headroom. Figure 11 shows the NF and conversion gain performance versus the supply voltage sweep from 1 V to 1.5 V. It shows a very stable performance versus the supply variations. The conversion gain changes by almost 3 dB from a supply going from 1.1 V to 1.3 V, and the NF is almost constant at 4.1 dB.

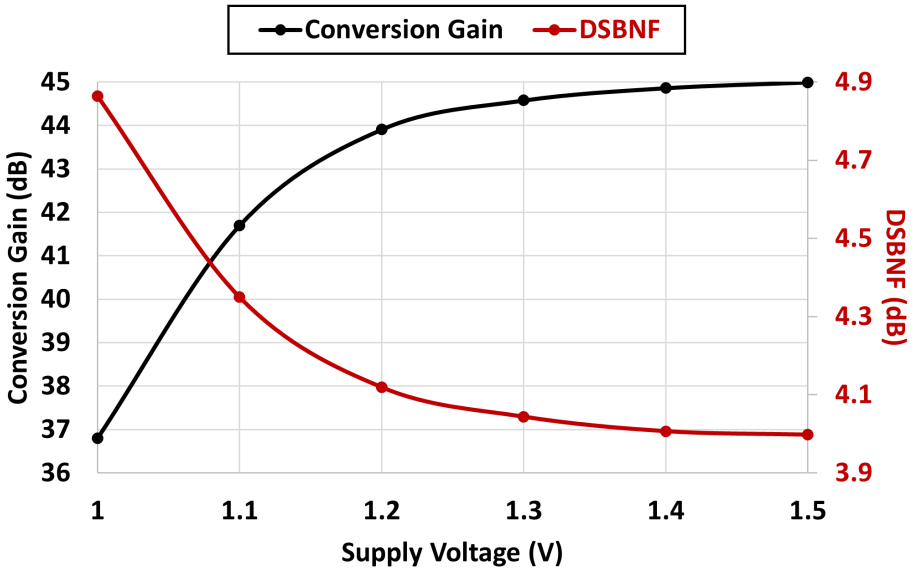

Figure 11. The NF and conversion gain versus supply variations.

Finally, the performance needs to be verified over the RF bandwidth from 1 GHz to 3.8 GHz in order to cover the wideband operation of the studied receiver. Figure 12 shows the NF and CG performance versus the LO frequency. It shows that the conversion gain reduces while NF increases versus the LO frequency sweep due to the losses of the parasitic capacitors after the LNTA.

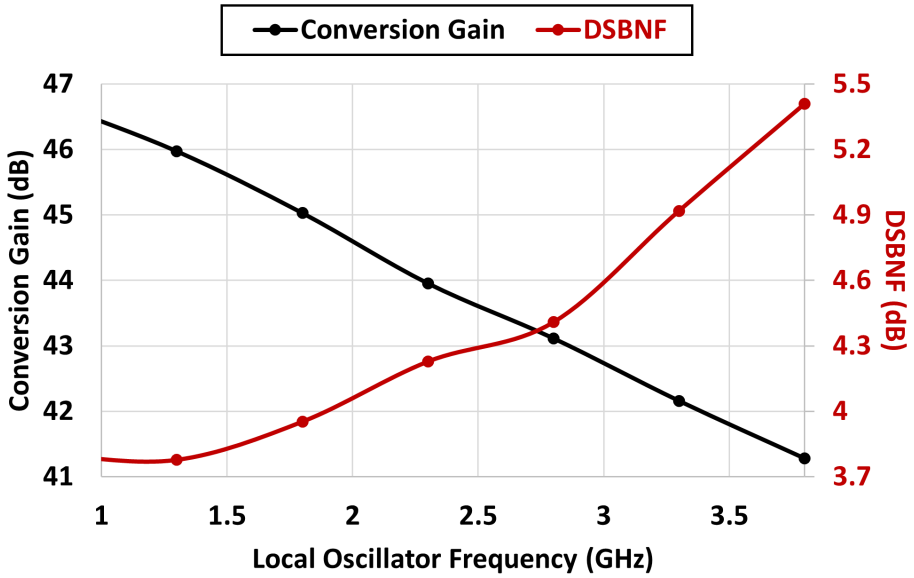

Figure 12. The NF and conversion gain versus the LO frequency.

The linearity performance of the CRR front-end is verified through post-layout simulations in Section 5.

4. Layout Considerations

Analog circuit design is always challenging since many design metrics need to be considered while designing a circuit. This can be more complex when designing RF circuits. It is always crucial to think of the impact of the layout on the performance during the schematic level design. Thanks to the evolution of process design kits (PDKs), many layout non-idealities such as gate resistance and terminal-to-terminal capacitance are modeled in the RF device models. However, the routing effects and substrate leakage are not modeled

at the schematic level. Hence, the layout considerations are discussed here in order to ensure the performance of the CRR front-end after post-layout simulations and ultimately after fabrication.

4.1. LNTA Layout

The LNTA is the first circuit in the receiver front-end that receives the weak signal. Routing to the LNTA input and output needs to have the minimum parasitic resistance to avoid the degradation of NF and S_{11} and to ensure a minimum parasitic capacitance. In this case, top metal layers are preferred to reduce metal resistance and substrate leakage, but it is preferred to reserve the topmost metal layer for supply and ground routing. It is very important to keep routing resistance and capacitance low where the RF signal path passes through in areas such as the capacitive cross-coupling, which is used to enhance the transconductance. In the LNTA layout, it is beneficial to maintain the layout symmetry but avoid using any conventional analog matching techniques since these increase the parasitic capacitance. The capacitive loading effect on the inductor may change the resonant frequency. In this case, a capacitor of 1 pF should be added to the schematic during the schematic design phase, which can be reduced after post-layout simulation is performed. Vias always have high resistance; hence, it is preferred to increase the number of vias to reduce the resistance. This can worsen with the scaling down of the CMOS node.

4.2. Mixer Layout

The mixer layout is also important as it is paramount to maintain the symmetry in the mixer layout to avoid any non-idealities related to the even-order harmonics. It is also important to keep the parasitics at the gate and the source of the switches equal to avoid LO-RF and LO-IF feed-through. This can be done by carefully drawing the input, output and LO routes. While routing the LO path, it is essential to isolate it with ground routing underneath the LO routing to avoid the substrate leakage of the high-power LO signal that may degrade the performance of the entire chip. In this case, the LO signal can be routed with metal five while it is shielded by metal four, which is connected to ground. While designing the mixer, it should not be made very large to avoid parasitic loading on the RF ports.

4.3. Baseband Circuits

Layout considerations are more relaxed when it comes to the BB circuits. Nonetheless, the routing and circuits after the mixer should keep both symmetry and ensure matching, while parasitic capacitances are not as critical to minimize. While sizing the BB transistors, a sufficient number of fingers and multipliers needs to be used to match the components appropriately. Two well-known layout techniques can be used to perform the matching of baseband circuits: common-centroid and inter-digitization. In this work, inter-digitization is used to create the layout of the AI and TIA circuits. In BB circuits, parasitic resistance is important. Thus, low-resistance metal with sufficient width should be used.

4.4. Floor Plan

The complete integration of the sub-circuits requires routing from the pads to the LNTA input. The parasitic capacitance needs to be minimized as much as possible to reduce RF signal losses. It is essential to use high metal layers to draw routing to the LNTA input. Sensitive nets can use several pads to reduce the effect of wire bonding. It is suggested to employ high metal layers while connecting the sub-circuits as well. High metal layers can be used to connect the LNTA output to the mixer input, while lower metals can connect the BB and AI circuit. To avoid RF signal loss, the parasitic capacitance at the LNTA output needs to be reduced, as indicated in (6).

5. Post-Layout Simulation Results and Discussion

The wideband and low-power RF-to-baseband CRR front-end was implemented with TSMC 130 nm CMOS technology. The layout is shown in Figure 13. The CRR front-end only occupies an active area of 0.025 mm^2. It consumes a very low current of 1.92 mA from a supply voltage of 1.2 V.

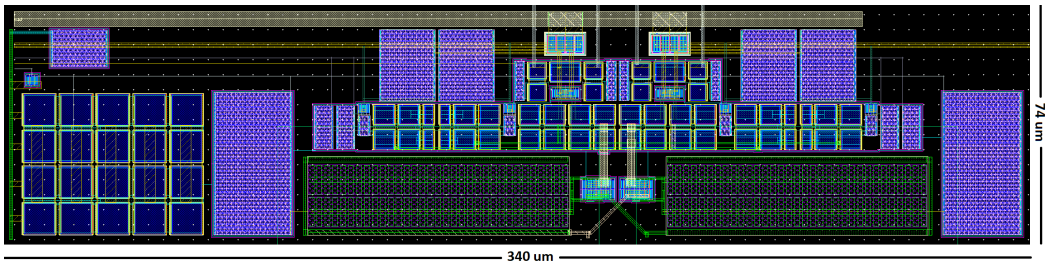

Figure 13. The layout of CRR front-end . Reprinted with permission from Ref. [12]. Copyright 2022, Frederic Nabki.

The NF and conversion gain are post-layout simulated versus the IF, while the LO frequency is constant at 2.4 GHz, as shown in Figure 14. At frequencies above 10 MHz, a flat NF of 4.5 dB is achieved, while an integrated DSB NF of 5.6 dB from 0.5 MHz to 20 MHz is attained. A high low-frequency noise contribution comes from the direct coupling of the LNTA flicker noise to the baseband due to the low impedance path through the AI circuit at low frequencies. The receiver exhibits a conversion gain of 39.5 dB over a wide IF 3dB-bandwidth of 40 MHz. Although the conversion gain drops at high IF, the NF remains below 5 dB at up to 100 MHz.

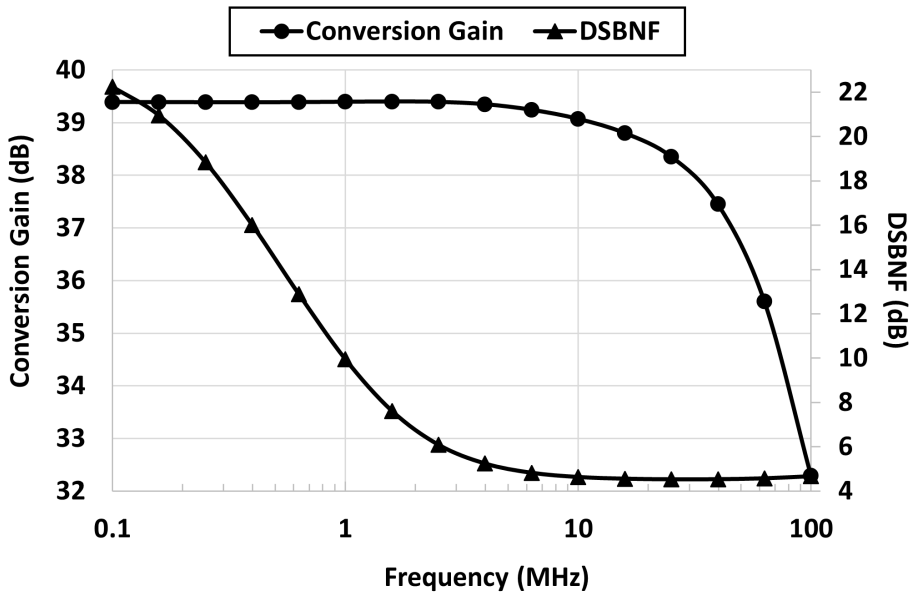

Figure 14. The post-layout simulated NF versus the IF.

The linearity performance is verified by applying two tones of 2.41 GHz and 2.411 GHz at the input. This is performed while the LO frequency remains at 2.4 GHz. This generates fundamental tones of 10 MHz and 11 MHz and third-order intermodulation products of 9 MHz and 12 MHz at the output. The output power of the fundamental tone and third-order intermodulation products versus the input power are shown in Figure 15. An IIP3 of −28 dBm is achieved.

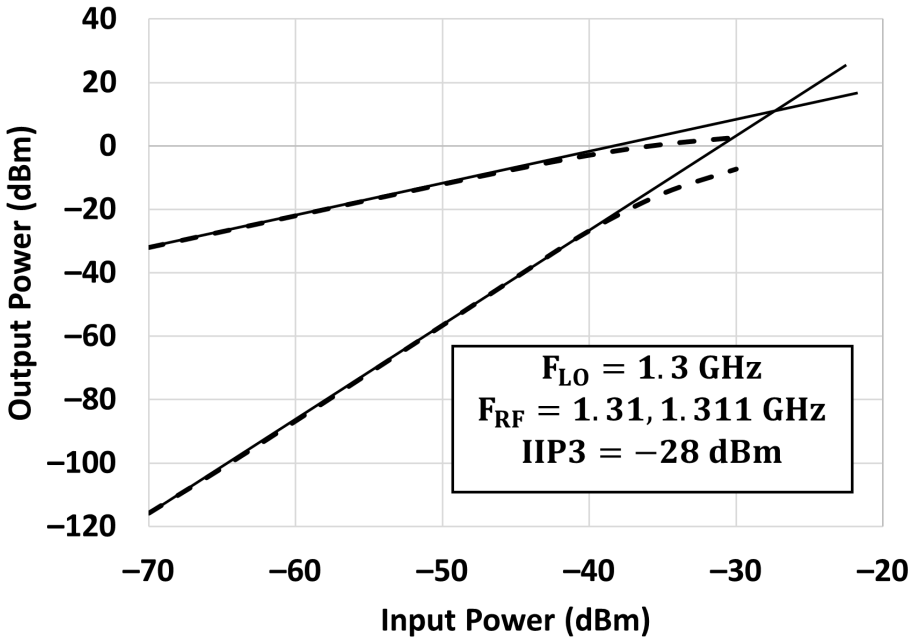

Figure 15. The post-layout simulated fundamental and third-order intermodulation products versus the input power.

The receiver performance is verified with an RF input signal varying from 0.75 GHz to 3.4 GHz while the IF remains constant at 10 MHz, as shown in Figure 16. The front-end exhibits an S_{11} of less than −10 dB over the entire RF range of interest. As the RF increases, the conversion gain reduces from 44.7 dB to 36 dB, and the DSB NF increases from 4.1 dB to 7.9 dB. On the other hand, the IIP3 result improves from −34.5 dBm to −25 dBm due to the conversion gain reduction.

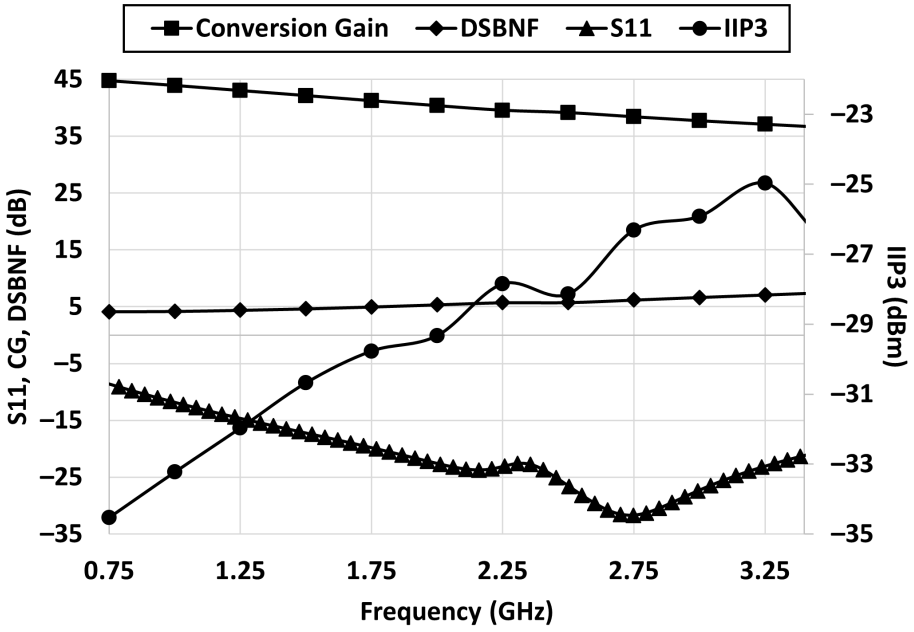

Figure 16. Receiver post-layout simulated performance versus the RF signal.

The design's capabilities and its overall performance are compared to prior works using the following figure of merit (FoM) used in [14] and given by

$$FoM = \frac{Gain[abs] \times (F_H - F_L)(GHz) \times IIP3[mW]}{(F-1) \times F_L(GHz) \times P_{dc}[mW]}, \quad (6)$$

where F_H and F_L are the highest and lowest RF operating frequencies, respectively, F is the noise factor, IIP3 is the in-band IIP3 performance in mW, and P_{dc} is the power consumption. The results are shown in Figure 17, where the FoM for the proposed design and other references is plotted versus the power consumption. The FoM compares well considering the power consumption.

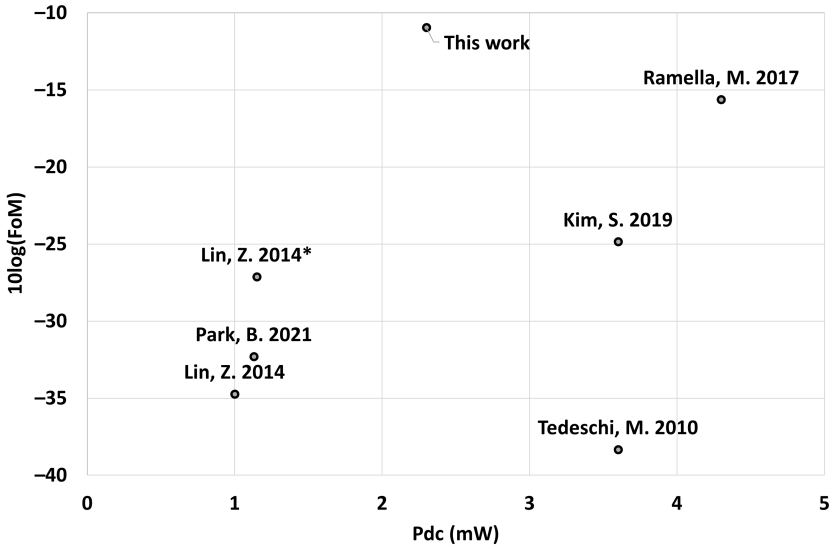

Figure 17. Comparison of the FoM to prior works versus the power consumption. Tedeschi, M. 2010 [2]. Lin, Z. 2014 [4]. Lin, Z. 2014* [5]. Kim, S. 2019 [8]. Ramella, M. 2017 [11]. Park, B. 2021 [10].

Table 1 compares and summarizes the performance of the proposed receiver simulated here from the circuit proposed in [12] with the latest literature. This work compares well in terms of bandwidth and NF considering its technology node and power consumption.

Table 1. Performance Summary and Comparison.

Parameters	This Work **	JSSC 2010 [2]	JSSC 2014 [4]	JSSC 2014 [5]	MWCL 2019 [8]	JSSC 2017 [11]	IEEE 2021 [10]
Application	IoT	ZigBee	ZigBee	ZigBee	IoT	Bluetooth	BLE
Process node	130 nm CMOS	90 nm CMOS	65 nm CMOS	65 nm CMOS	65 nm CMOS	28 nm CMOS	65 nm CMOS
Freq. (GHz)	0.8–3.4	2.4	2.4	0.433–0.96	0.91	2.4	2.4–2.48
S11 (dB)	<−10	<−10	<−10	<−10	<−10	<−10	<−10
Gain (dB)	39.5	75	57	50	40.7	43.4	42
NF (dB)	5.6	9	8.5	8.1	1.94	7.8	13.2
IIP3 (dBm)	−28 *	−12.5 ┼	−6 ┼	−20.5 ┼	−25.6 *	−20 *	−25 *
P_{DC}@V_{DD} (mW)	2.3@1.2	3.6@1.2	1@1.2	1.15@0.5	3.6@1.8	4.3@1.8	1.13@0.8
Active Area (mm^2)	0.025	0.35	0.3	0.2	0.559	0.4	0.85
FoM	−11	−38.3	−34.7	−27.1	−24.8	−15.6	−32.3

* In-band IIP3; ┼ Out-of-band IIP3; ** Post-layout simulation.

6. Conclusions

This work provided a design tutorial for the low-power and wideband RF-to-baseband CRR that was proposed in [12]. It discussed topology selection, design considerations and layout aspects for the LNTA, down-conversion mixer, AI circuit and TIA. The receiver is able to perform over the wide frequency band from 0.8 GHz to 3.4 GHz.

The proposed receiver in [12] was divided into four individual sub-circuits—LNTA, mixer, AI circuit and TIA—to be designed individually before integration. The design of each circuit was detailed through equations and simulations. Two well-known LNTA topologies, the CG and CS, were studied to make sure that the best topology was selected to provide wideband performance. The AI circuit in [12] enhances the RF performance and addresses the issues raised in the literature. The TIA design used a single transistor, and design constraints and metrics were studied. Then, the test bench models to design and simulate each sub-circuit were also included. Finally, post-layout simulation results after the integration were presented, outlining the potential of the receiver and the viable design procedure described in this paper.

Author Contributions: Conceptualization, A.A. and F.N.; methodology, A.A.; software, A.A.; validation, A.A.; formal analysis, A.A.; investigation, A.A.; resources, A.A.; data curation, A.A.; writing—original draft preparation, A.A.; writing—review and editing, A.A. and F.N.; visualization, A.A.; supervision, A.A. and F.N.; project administration, A.A.; funding acquisition, F.N. All authors have read and agreed to the published version of the manuscript.

Funding: Received funding from NSERC (Natural Sciences and Engineering Research Council of Canada) for this research work.

Acknowledgments: The author would like to thank CMC Microsystems for chip fabrication and for providing the EDA tool.

Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

P1dB	1 dB compression point
AI	Active inductor
BB	Baseband
CG	Common gate
CRR	Current-reuse receiver
CS	Common source
DUT	Design under test
DSB	Double side-band
ÉTS	École de technologie supérieure
FoM	Figure of merit
IF	Intermediate frequency
IoT	Internet of Things
LNTA	Low-noise transconductance amplifier
LO	Local oscillator
NF	Noise figure
DSBNF	Double side-band noise figure
PDK	Process design kit
RF	Radio frequency
TIA	Transimpedance amplifier
VCO	Voltage-controlled oscillator
VCCS	Voltage-controlled current source
V_{TH}	Voltage threshold

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