IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received 17 August 2022, accepted 31 August 2022, date of publication 8 September 2022, date of current version 16 September 2022.

Digital Object Identifier 10.1109/ACCESS.2022.3205110

RESEARCH ARTICLE

A Wideband Low-Power RF-to-BB Current-Reuse Receiver Using an Active Inductor and 1/*f* Noise-Cancellation for L-Band Applications

ARASH ABBASI, AMIR HOSSEIN MOSHREFI, (Graduate Student Member, IEEE), AND FREDERIC NABKI, (Member, IEEE)
Department of Electrical Engineering, École de Technologie Supérieure (ÉTS), Montreal, QC H3C 1K3, Canada
Corresponding author: Arash Abbasi (arash.abbasi.1@ens.etsmtl.ca)

This work was supported by the Natural Sciences and Engineering Research Council of Canada (NSERC).

ABSTRACT A low-power and wideband RF-to-baseband (BB) current-reuse receiver (CRR) front-end utilizing both a $1/f$ noise cancellation (NC) technique and an active inductor (AI) is proposed tuned to operate from 1 GHz to 1.7 GHz for L-Band applications, including those that require high modulation bandwidths. The CRR front-end employs a single supply and shares the bias current of the low noise transconductance amplifier (LNTA) with the BB circuits to reduce the power consumption. To minimize the losses of the radio frequency (RF) signal right before down-conversion, a high impedance AI circuit isolates the mixer input from the CRR output node. The $1/f$ NC circuit suppresses the low frequency noise of the LNTA that leaks to the output. A common-gate LNTA with g_m-boosting, along with a single-to-differential LC-balun are used to enhance the input matching, conversion gain and noise figure (NF). The proposed receiver is fabricated in a TSMC 130 nm CMOS process and occupies an active area of 0.54mm^2. The input matching (S_{11}) is below -10 dB from 1 GHz to 1.7 GHz. At a local-oscilator (LO) frequency of 1.3 GHz, intermediate-frequency (IF) of 10 MHz and default current settings, the CRR achieves a conversion gain of 41.5 dB, a double-sideband (DSB) NF of 6.5 dB, and an IIP3 of -28.2 dBm while consuming 1.66 mA from a 1.2 V supply.

INDEX TERMS Current-reuse receiver (CRR), cross-coupled common-gate low noise transconductance amplifier (LNTA), wideband, low-power, wide modulation bandwidth, L-Band.

I. INTRODUCTION

The internet of things (IoT) aims to connect trillions of devices for various applications. Today, both academia and industry are investigating how to employ the IoT to manage, locate, monitor, identify and track within different sectors such as automotive, agriculture, manufacturing, education, smart buildings, military and others. IoT applications operate in different frequency bands. One of the important bands is the L-Band that includes several applications and wireless standards such as various global navigation satellite systems (GNSS), cellular communication, aircraft surveillance, digital video/audio broadcasting, etc. [1], [2], [3], [4], [5], [6], [7]. For instance, among the various features of the IoT, location tracking is important, and can be used in different applications such as vehicles for navigation, health for patient tracking, military for soldier localization, shipping to track goods, etc [4].

As the L-Band includes several wireless standards and applications within the $1-2$ GHz band, a wideband RF front-end that covers a wide frequency range is suitable as it mitigates the need of multiple RF front-ends. In addition, a wide modulation bandwidth is required in the front-end to not limit the receiver bandwidth to address the requirements of different wireless standards.

However, while wideband RF front-ends are attractive, as they provide system agility and compactness, reducing the power consumption of the RF front-end while maintaining performance metrics such as linearity and noise figure (NF) is a challenge. Various methods and techniques have been

The associate editor coordinating the review of this manuscript and approving it for publication was Sungyong Jung.

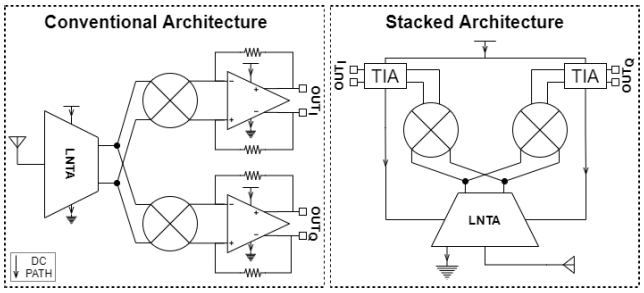

FIGURE 1. Conventional and stacked receiver front-end architectures.

studied to address this challenge. Among them, a widespread method to reduce power consumption is current-reuse. Usually, current-reuse has been employed within individual blocks such as the low noise transconductance amplifier (LNTA) [8]. In [9], a current-reuse power-optimized LNTA was used in a conventional cascaded receiver architecture. It reports good 1-dB compression out-of-band linearity, but a poor in-band 1-dB compression of −56 dBm is achieved at a maximum gain setting of 61 dB. Another approach [10] employed a current-reuse baseband amplifier in a mixer-first receiver architecture. It achieves very good performance consuming a low-power of 0.38 mW. However, the receiver architecture is not suitable for wideband modulations as it reports a very low baseband bandwidth of 2 MHz that is not suitable for wider modulation bandwidth applications. In [11], a quadrature low noise amplifier (LNA) and active-type poly-phase filter (PPF) were used to reduce power consumption. However, the receiver has a narrow RF bandwidth due to the common-source LNA topology, and high NF because of the quadrature technique used in the LNA. In [12], alternatively, an inverter-based LNA with an LC-balun and passive PPF are used to generate the quadrature signal before the down conversion. This reduces the LO dynamic power for Bluetooth low-energy (BLE), but using an LC-balun and passive PPF is not suitable for wideband applications. In addition, a phase-locked loop (PLL) free receiver architecture is proposed in [13] at the cost of a high NF.

Recently, current sharing of RF and BB blocks using a single supply voltage has been actively studied. Conventionally, receiver front-ends cascade circuits to receive and amplify a weak RF signal with a LNTA, down-convert it to BB through a mixer and finally convert the current signal to a voltage signal using a transimpedance amplifier (TIA), as shown in Fig. 1. On the other hand, by scaling down the CMOS technology node where the voltage threshold is reduced and transition frequency (f_T) is increased, stacked architectures that reduce power consumption by sharing the current of the RF circuits with the BB circuits are now possible.

Although the stacked architecture reduces power consumption significantly, it has shortcomings. In [14], LNTA, mixer and voltage-controlled oscillator (VCO) blocks are stacked to share a single supply, reducing the power consumption. However, the front-end suffers from VCO injection locking and a high NF of 9 dB. In addition, the common-source LNTA used limits the RF bandwidth, which is not suitable to cover wide RF bandwidth with a single receiver module. Another approach with cascoded LNTA, active mixer and BB filter was proposed in [15]. It still suffers from high NF. Moreover, the use of an active mixer reduces the linearity and increases voltage headroom requirements. A function-reuse RF front-end is an interesting method which employs a push-pull amplifier to function as both LNTA and TIA. However, it reported poor P_{1dB} of −50 dBm due to the low supply voltage [16]. This approach is only suitable for sub-GHz applications. A current-reuse architecture using an N-path passive mixer for input matching is another sub-GHz alternative which reports good NF performance [17]. However, one of its bottlenecks is the use of an active mixer for down-conversion that requires a higher supply voltage. It also suffers LO to RF leakage due to the N-path passive mixer used for input matching. Moreover, it requires additional circuits to combine the N paths at the output which increases the overall power consumption. In [18], a $1/f$ noise-cancellation (NC) technique and linearity enhancement method is used, but its power consumption is high at 8 mW. A current-reuse receiver (CRR) proposed in [19] employed input matching and a $1/f$ noise reduction technique that results in a low NF of 1.94 dB at the cost of limited RF bandwidth. Moreover, both [19] and [20] suffer from losses of the RF signal due to the sharing of the BB output and passive mixer input. To overcome this issue, our earlier work in [21], applied the concept of an active inductor (AI) from [22], [23] to isolate the mixer input from the BB output, thus reducing the losses of the RF signal before the down conversion. This allows the receiver to maintain its performance at higher frequencies even in a relatively large 130 nm CMOS process. However, it still suffers from a high NF at low IF due to the direct injection of the low frequency noise of the LNTA into the BB.

This work is the continuation and extension of our earlier published conference paper in [21] that presented simulation results. Notably, this work improves the circuit architecture of our prior work with a 1/f noise cancellation technique and an integrated on-chip input inductor. In [21], a high quality off-chip input inductor model was used in simulation, while in this work, this inductor is integrated on-chip. Importantly, measurement results are now presented, thus experimentally validating our prior work, along with the aforementioned improvements.

Accordingly, this work proposes a quadrature (I/Q) low-power and wideband RF-to-BB CRR front-end uniquely employing both an AI and $1/f$ NC technique in order to overcome the aforementioned issues. It utilizes a wideband LNTA stage to convert the RF voltage to an RF current, a current driven passive mixer to down-convert the RF signal to an IF signal, and a TIA to convert the IF current to an IF voltage using a single transistor. The proposed CRR front-end achieves good NF and linearity performance along with low power consumption. The paper is structured as follows. Section II provides a receiver architecture overview, Section III details the different circuits required in

the design, and Section IV presents the measurement results and discusses them.

II. RECEIVER OVERVIEW

Through the scaling down of CMOS technology nodes, the implementation of high frequency circuits is readily possible with reduced trade-offs thanks to the reduced parasitic. However, the fabrication cost increases sharply for smaller technology nodes. Thus, in order to implement such circuits in cost efficient CMOS such as 130 nm CMOS technology, design techniques are required to maintain the performance of the design. For instance, in [19], while a very low NF is reported, the RF bandwidth is limited. This is due to the fact that the input of the down-conversion mixer is shared with the receiver output node causing loading from the following stage and output circuit. Ultimately, this degrades the performance of the receiver at higher frequencies and limits it to sub-GHz applications. To mitigate this issue, this work uniquely applies both an AI and $1/f$ NC technique from [21], [22], [23] to the CRR front-end.

The block diagram of the proposed CRR front-end is shown in Fig 2. It includes an LNTA to convert the RF voltage to a current. Transistors M_{CG}, inductor L_R and cross-coupled capacitors C_{AC} form the LNTA circuit. The LNTA sets the receiver sensitivity, linearity and input impedance matching. Thus, it is designed to attain the required performance metrics, and it defines the overall current consumption. The CRR employs a passive mixer shown on the top left of the figure, and includes transistors M_{MX} that do not consume DC current. As previously mentioned, the CRR uses both an AI and $1/f$ NC circuit in order to improve the receiver sensitivity. These are implemented by M_{AI}, R_{AI}, C_{AI}, M_{NC} and R_S. The single supply current divides equally between the TIA blocks, each formed by a single transistor, M_{TIA}, and feedback resistor, R_{FB}. The TIA feeds the LNTA and AI current. Moreover, the receiver employs a quadrature (I/Q) architecture using a 25% LO duty-cycle and single LNTA. In this way, the power consumption is significantly reduced by the reuse of the supply current. Details pertaining to each circuit composing the CRR front-end are discussed in the next section.

III. CIRCUIT DESIGN

A. LNTA WITH LC-BALUN MATCHING NETWORK

The LNTA plays an important role for input matching and receiver sensitivity. Two well-known typologies can be used to provide input matching: the common-source and the common-gate. In [19], the common-source topology along with a $1/f$ NC technique is employed. Although the noise performance is very good, it has a narrow-band response, and is sensitive to package parasitics and non-idealities related to the printed circuit board (PCB). In this work, a common-gate topology is used instead, and provides wideband input matching at the cost of a higher NF. In Fig. 2, M_{CG} forms the common-gate topology which is differentially applied in this design. The gate terminal of M_{CG} connects to a bias

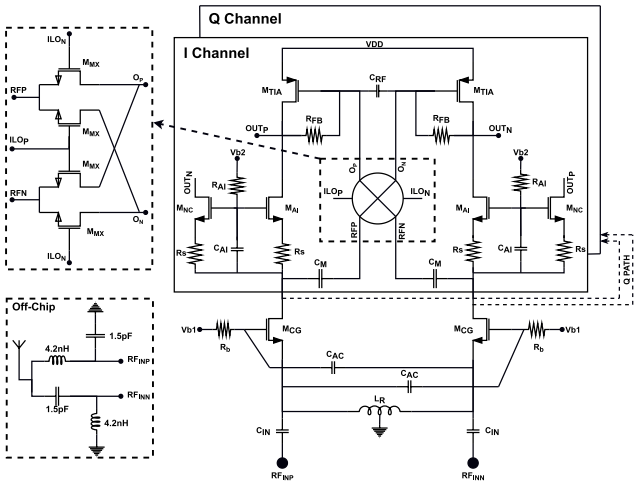

FIGURE 2. Block diagram of the proposed CRR front-end.

voltage, V_{b1}. Center tap inductor L_R provides the DC current path to the ground and resonates with parasitic capacitors at the input to reduce input losses. C_{IN} is an AC-coupling capacitor. To reduce the power consumption and NF of the LNTA, cross-coupled capacitors C_{AC} are used to boost the transconductance of M_{CG} by approximately a factor of two, yielding an effective transconductance of $g_{meff} = 2 \times g_m$. This assumes that the short channel effect is negligible for the input transistors. Moreover, this increased transconductance helps achieve the required input impedance, $1/g_{meff}$, and a better NF with less current. The noise factor of the LNTA is calculated by using the following:

$$F \cong 1 + \frac{\gamma}{4\alpha} \cdot \frac{1}{R_S g_m} + \frac{R_{Balun}}{R_S}, \tag{1}$$

where α and γ are the bias-dependent noise parameters and R_S is the source resistance. The balun losses can be modeled by series resistor R_{Balun}. γ/α is reduced by increasing the channel-length slightly while maintaining the transition frequency, f_T, at least ten times higher than the frequency of operation.

Earlier works used a 1:1 balun to convert the single ended signal to a differential one [22], [24], [25]. To perform input matching, the LNTA input impedance should be designed to $R_S = 1/2g_m$. This degrades the NF by increasing the second term in equation (1) by two times. The noise factor is then given by

$$F \cong 1 + \frac{\gamma}{2\alpha} + \frac{R_{Balun}}{R_S}. \tag{2}$$

In this work, a 2:1 LC-balun, shown at the bottom left of Fig. 2, is used to convert the single ended input signal to a differential one at the input of the LNTA. It can convert the 50 Ω antenna impedance to any impedance required (in this work 25 Ω) on the differential side by choosing proper inductor and capacitor values. This gives the advantage to design the LNTA with higher $g_{m,eff}$ (in this work $2 \times g_{m,eff}$) to achieve lower NF while maintaining the input matching

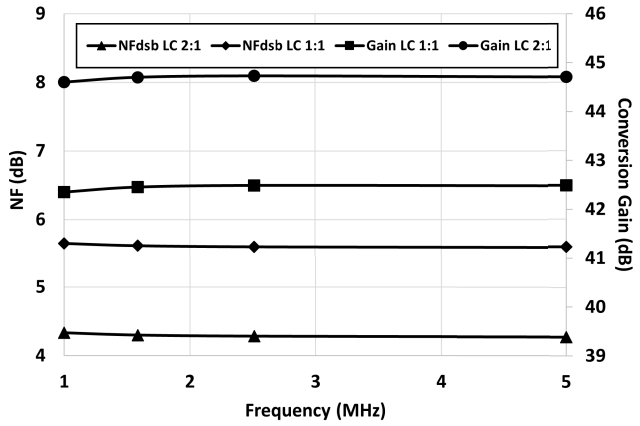

FIGURE 3. Simulated conversion-gain and DSB NF of the CRR using a 1:1 LC-balun or a 2:1 LC-balun.

performance. In this way, the LNTA noise is given by

$$F \cong 1 + \frac{\gamma}{4\alpha} + \frac{R_{Balun}}{R_S}. \quad (3)$$

In this fashion, the good input matching is maintained and the second term in (3) is halved in comparison to (2) that involves a 1:1 balun. An W/L of $50\mu/140n$ is chosen for M_{CG} to achieve the best NF and g_m/g_{ds} performance, where g_{ds} is the admittance of M_{CG}.

To outline the benefit of the matching technique proposed, the simulated NF and conversion-gain of the CRR is compared using a 1:1 or a 2:1 LC-balun employing $g_{m,eff}$ and almost $2 \times g_{m,eff}$, respectively. The results are shown in Fig. 3, outlining that the conversion-gain is improved by about 2.5 dB and the NF is reduced by more than 1 dB.

The LNTA and LC-Balun were tuned to the L-band in this work, but this tuning could have been applied to other bands such as the 2.4 GHz ISM band (e.g., Bluetooth Low Energy) or the 900 MHz ISM band (e.g., Zigbee).

B. ACTIVE INDUCTOR AND 1/f NOISE-CANCELLATION TECHNIQUE

Conventionally, a cascode circuit is used to boost the output impedance and enhance isolation. Fig. 4(a) shows the conventional CRR using a cascode circuit after the LNTA. The input of the down-conversion mixer and receiver output share the same node, causing RF signal attenuation from both parasitic capacitors and the large loading of the next stage at the output. This limits the operating frequency of the circuit. Moreover, it renders the architecture impractical for modern applications if designed in a large technology node such as 130 nm CMOS. To overcome this issue, this work proposes an AI in Fig. 4(b) using M_{AI}, C_{AI} and R_{AI}. The impedance looking into the AI circuit, Z_{AI}, is low at DC but keeps increasing with frequency [23]. In this way, the AI circuit isolates the mixer input from the output node at higher frequencies, while the DC current passes through the AI circuit. To boost the impedance further, R_S is added to the source of M_{AI}. The impedance looking into the AI circuit, Z_{AI}, by ignoring M_{NC} since it is in parallel is given by

$$Z_{AI}(s) \cong \frac{g_{m,AI}R_S(R_{AI}C_{AI}s + 1) + R_{AI}C_{AI}s}{g_{m,AI}R_SC_{AI}s + g_{m,AI} + C_{AI}s} \,||\, \frac{1}{sC_{par}}, \quad (4)$$

where C_{par} is the parasitic capacitance at the mixer input. The C_{par} depends on the technology node. Fig. 5 shows the mathematical model of the magnitude of Z_{AI} versus the frequency using (4) for different parasitic capacitance values and compares it with simulation results. To model this, a $g_{m,AI}$ of 3.5 S, C_{AI} of 1 pF, R_{AI} of 50 kΩ and R_S of 200 Ω are used. Two scenarios are considered for C_{par}. Firstly, C_{par} is ignored, showing that Z_{AI} increases linearly with frequency. Then, C_{par} values of 30 fF are considered to compare with the simulation results. This shows that as a result of increasing the parasitic capacitor at the input of the AI circuit, Z_{AI} reduces faster at higher frequencies and limits the operating frequency of the AI.

The AI circuit injects noise into the LNTA output at RF as well as at low frequencies at BB. The noise factor considering the AI circuit is then given by

$$F \cong 1 + \frac{\gamma}{4\alpha} + \frac{R_{Balun}}{R_S} + 4R_S\left(\gamma g_{m,AI} + \frac{1}{R_{AI}}\right)\left(1 + \frac{R_{Balun}}{2R_S}\right) + K_1\frac{V^2_{fk\_LNA}}{4kTR_S} + K_2\frac{V^2_{fk\_AI}}{4kTR_S}. \quad (5)$$

Another problem of the conventional CRR shown in Fig. 4(a) is the direct coupling of the LNTA $1/f$ noise to the output. This also can affect the structure with the AI since the AI circuit is not blocking the low frequency components. To overcome this issue, M_{NC}, added in Fig. 4(b), creates a low frequency path to the output with the opposite polarity. This makes the $1/f$ noise common-mode for the next stage such that it can be rejected with a differential architecture ($K_1 \sim 0$). The $1/f$ noise of the AI circuit is still contributing to the output. The source-degeneration resistor, R_s, helps reduce the $1/f$ noise of M_{NC} and M_{AI} as well as boost Z_{AI}. In (5), $g_{m,AI}$ is replaced with $g_{m,AI}/(1 + g_{m,AI}R_s)$ where R_s is a degeneration resistor and $K_2 \ll 1$. The simulation results of the CRR front-end with the NC circuit activated or deactivated is shown in Fig. 6. As can be seen, while the thermal noise remains the same, the $1/f$ noise is suppressed by the NC circuit. This allows the CRR front-end to operate at low IF in a direct-conversion architecture.

The straightforward way to design the NC circuit is to half the W/L ratio of M_{AI} and double the value of R_S in the AI circuit. Then, the same device values can be used in the NC circuit [22].

C. PASSIVE DOWN-CONVERSION MIXER

A conventional current driven double-balanced passive mixer is employed to convert the RF current to the BB current, as shown in Fig. 2. It operates with a 25% duty cycle LO signal to enhance both NF and conversion gain [26]. The clock generation circuit is shown in Fig. 7 [27]. The AC-coupling capacitors, C_M, separate the DC biasing of the mixer. Moreover, this blocks the low frequency noise of the LNTA. The

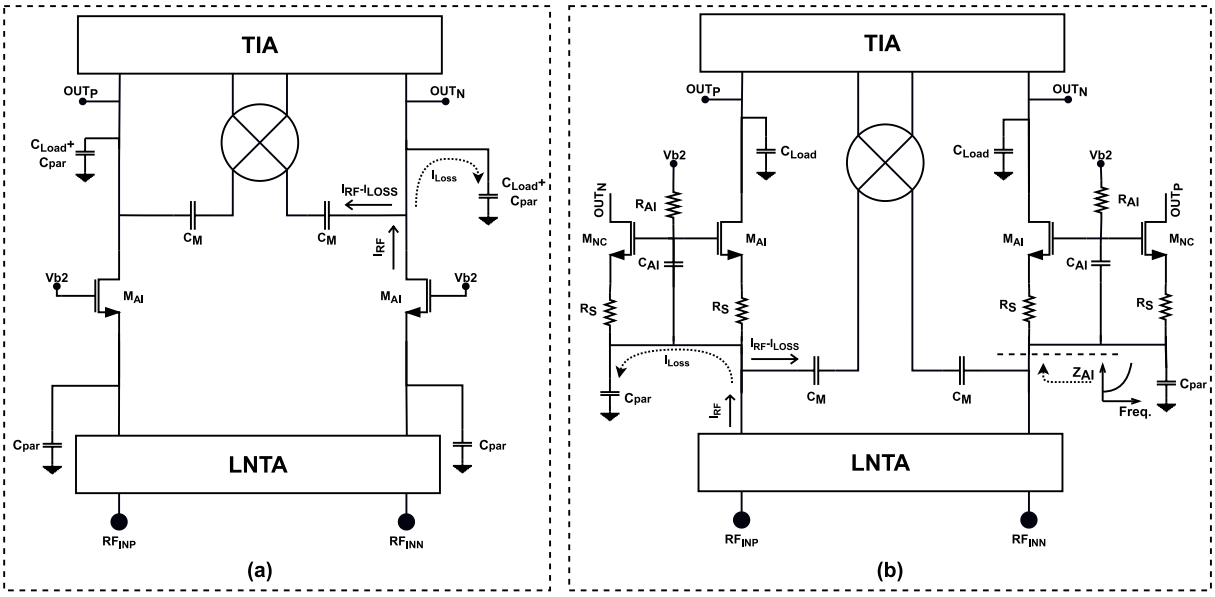

FIGURE 4. (a) Convectional CRR with cascoded transistor. (b) Proposed architecture introducing an AI and 1/*f* NC technique.

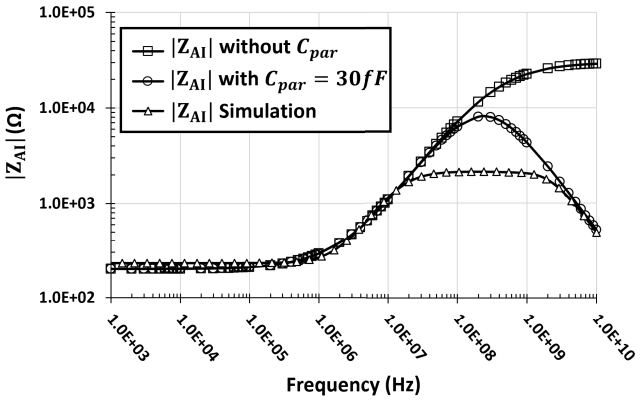

FIGURE 5. Mathematical model, with and without C_{par}, and simulation of the magnitude of Z_{AI} versus frequency.

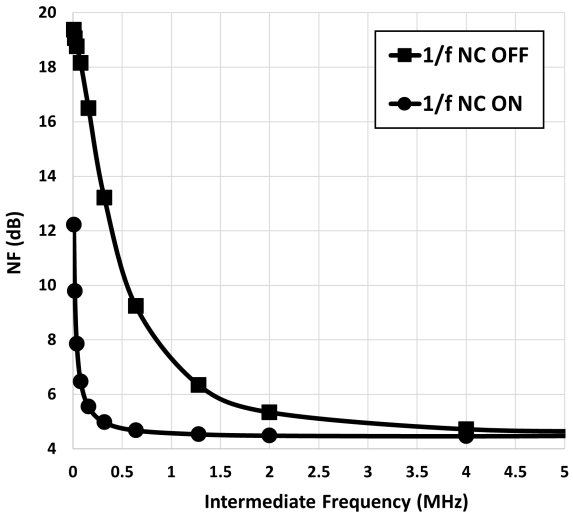

FIGURE 6. The simulated NF with the NC circuit activated or deactivated.

source and drain biasing of the mixer switches is provided by the TIA to be half of the supply (600 mV). The gate bias voltage of the mixer switches is chosen to ensure that the LO signals are able to toggle the switches properly, while maintaining the V_{GS} and V_{GD} values in the safe operating region to avoid breakdown.

D. TRANSIMPEDANCE AMPLIFIER

The BB current generated by the down-conversion mixer is converted to a BB voltage using a TIA at the output node. The TIA circuit is formed by M_{TIA} and feedback resistors, R_{FB}. M_{TIA} needs to provide sufficient g_m to maintain the impedance low enough at the output of the mixer in order to keep the voltage swing at that node small, and thus avoid a degradation of the linearity. To enhance the output impedance and reduce the short-channel effect, a large channel length of 500 nm is used for M_{TIA}.

Overall, the conversion gain of the proposed receiver is approximately calculated as

$$Gain_{CRR} \cong \frac{2\sqrt{2}}{\pi} g_{m,eff} R_{FB} \tag{6}$$

E. OUTPUT BUFFER

An output buffer is required to allow for measurement of the CRR using off-chip laboratory equipment such as a spectrum analyzer, high-speed oscilloscope or any similar instrument with a 50 Ω input impedance. This output buffer ensures that the output impedance of the CRR is well matched to the impedance of the testing equipment. For this purpose, a fully differential current-mode logic (CML) circuit is used and shown in Fig. 8. The gain of the CML circuit is designed

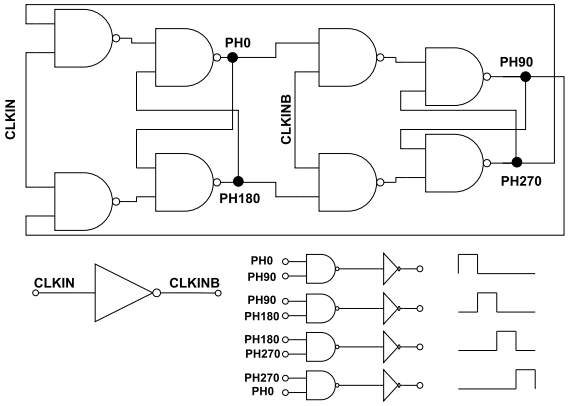

FIGURE 7. Schematic of the clock generation circuit generating 25% duty cycle phases.

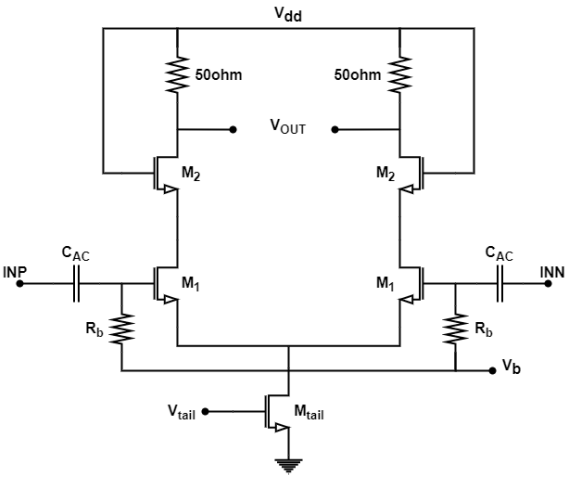

FIGURE 8. Output buffer circuit used in the measurements.

to be of 0 dB and is given by

$$Gain_{CML} = g_{m1} \cdot R_L, \tag{7}$$

where R_L is the output load. This load is chosen to be 50 Ω in order to avoid a very high value for $g_{m,M1}$ that would results in high current and large W/L ratio, reducing the bandwidth of the buffer. A 2:1 balun can be used off-chip at the output to convert the 100 Ω differential output to a single ended 50 Ω output. Cascode transistors, M_2, are used to enhance the bandwidth of the CML circuit. The input of the CML circuit is AC-coupled to separate its biasing voltage with that of the CRR front-end. The cascode transistors are directly biased with the supply voltage.

Both the CML and CRR front-end each utilize a 1.2 V supply. The CML circuit consumes a high current of 40 mA to maintain high linearity and low NF performance for testing proposes.

IV. EXPERIMENTAL RESULTS AND DISCUSSION

The low-power and wideband RF-to-BB current-reuse receiver front-end was fabricated in TSMC 130 nm CMOS technology. Both CRR front-end and CML output buffer were implemented on-chip and the die micrograph is shown in

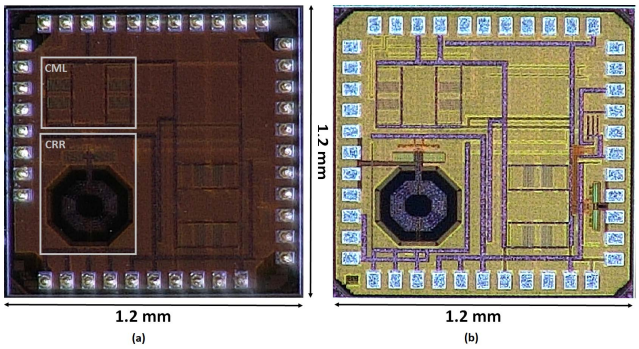

FIGURE 9. Die micrograph of the fabricated die (a) fully covered with metal fill (Chip1), and (b) with reduced metal fill on the sensitive nodes (Chip2). Note that the circuitry on the right half of the dies is not related to this work.

Fig. 9. The design was fabricated under two conditions, one is covered with metal fill at sensitive nodes (Chip1), shown in Fig. 9(a), and another reduced the metal fill on sensitive RF nodes and blocks (Chip2), shown in Fig. 9(b). Metal fill reduction was done manually through an iterative process to make sure the metal fill is optimized on the sensitive paths. The CRR front-end occupies an active area of 0.54mm^2, excluding the output buffer and bond pads. It consumes 1.66 mA from the 1.2 V supply. Both chips were measured under the same biasing conditions, PCB and test setup.

The diagram and picture of the measurement setup is shown in Fig 10. The CRR front-end and output buffer supply and ground are separated on the PCB. The chip is packaged into a QFN48 package, and is connected to the PCB with an RF socket (SG-MLF-7006). To extract the actual performance of the CRR front-end, the non-idealities due to the socket, cables and external baluns should be taken into account. To this end, the S-parameter characteristics of the cables and baluns are extracted using a 4-port vector network analyzer (VNA), Rohde and Schwarz ZVB 8. The socket losses are provided by the manufacturers' datasheet. The single-ended input from the signal generator (Agilent N5182a MXG) is converted to a differential input using an external LC-balun shown at the bottom left of Fig. 2. A second signal generator(Agilent N5182a MXG) provides the clock signal for the mixer switches. The differential output of the output buffer is converted to a single-ended signal using a 2:1 balun (TRS2-32-75+) and this signal drives the measurement equipment.

The Y-factor method using a noise source is employed to measure the NF performance. Fig. 11 illustrates the measured and simulated double side-band (DSB) NF versus the IF while the LO frequency is at 1.3 GHz. A flat measured NF of 7.5 dB is achieved using Chip1 and is close to the simulation results above an IF of 1 MHz.The measured and simulated NF of Chip2 with reduced metal fill lowers by about 1 dB to 6.5 dB above an IF of 1 MHz. The $1/f$ NF is slightly increased for both simulation and measurement at low frequencies due to the AC-coupling between the CRR front-end and the output buffer circuit. This effect is not important as

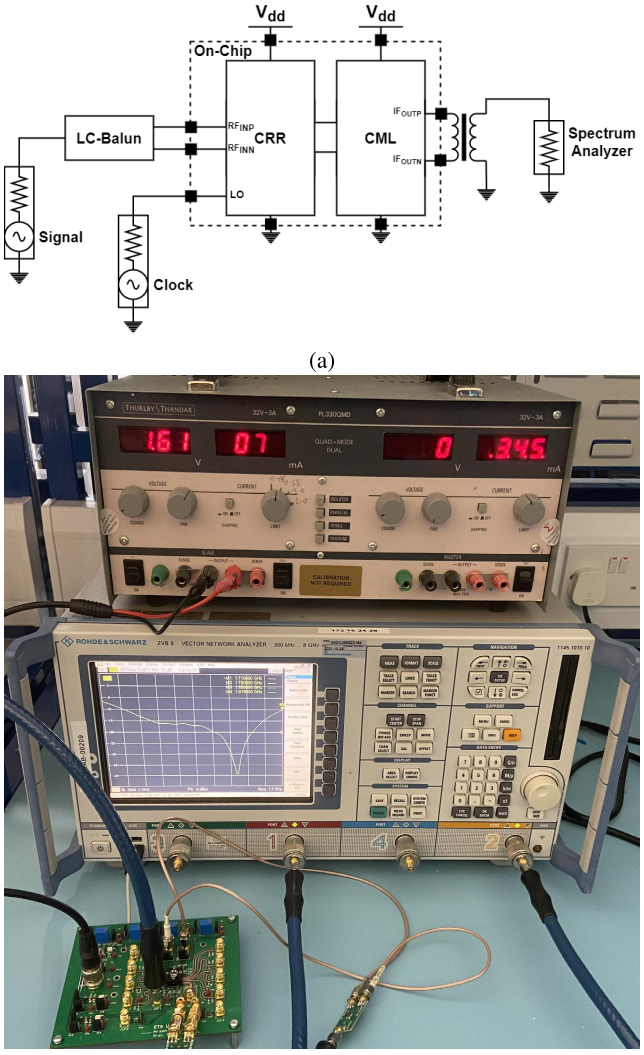

FIGURE 10. (a) Diagram and (b) picture of the measurement setup.

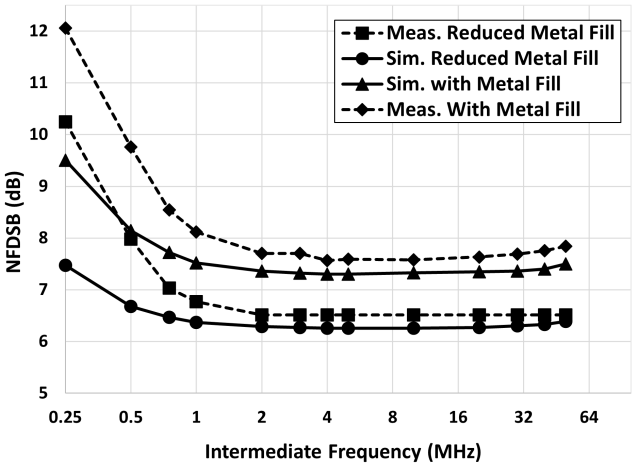

FIGURE 11. The simulated and measured NF versus the IF.

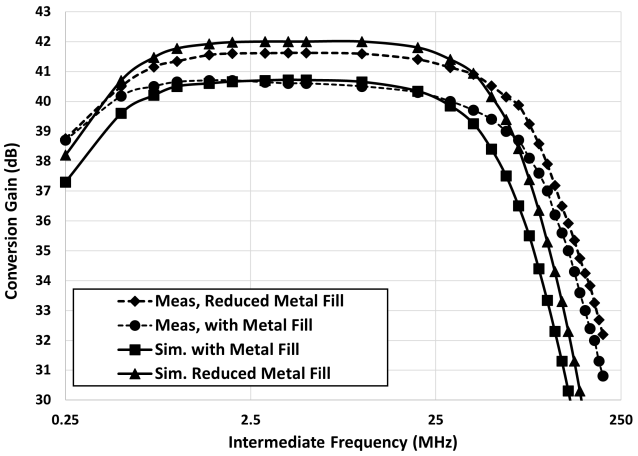

FIGURE 12. The simulated and measured conversion gain versus the IF.

the buffer would not be required in a receiver implementation including the BB circuits. The measured 1/*f* noise corner frequency is very close to the simulation results. This shows the 1/*f* NC circuit operates well.

The measured and simulated conversion gain versus the IF is shown in Fig. 12 while an LO frequency of 1.3 GHz is used. The circuit achieves a flat conversion gain of 40.5 dB with Chip1. The figure also shows using Chip2 the impact of the metal fill effect on the conversion gain simulation and measurement results due to the parasitic loading. The conversion gain of 41.5 dB of Chip2 represents a 1 dB improvement over Chip1. A wide IF bandwidth of 90 MHz is achieved. The conversion gain results are reduced at low frequency due to the AC-coupling at the input of the output buffer, but again this would not be an issue in an implementation of the receiver without the buffer.

A two-tone test with 1.31 GHz and 1.311 GHz input signals is performed to measure the in-band IIP3 performance of the CRR front-end. An LO frequency of 1.3 GHz is applied to the mixer switches. This generates two tones at 10 MHz and 11 MHz at the IF, along with third-order intermodulation products at 9 MHz and 12 MHz that appear above the noise floor by increasing the input power. Fig. 13 shows the output power of the fundamental tone and third-order intermodulation product versus an input power sweep where an in-band IIP3 of −28.2 dBm is achieved for both Chip1 and Chip2. There may be a few dB uncertainty in the IIP3 results since the CML circuit might limit the linearity. To confirm this, under the same biasing condition and test scenario, the CML voltage was increased by 0.2 V. This improved the IIP3 result of Chip1 to −26.5 dBm and Chip2 to −27.5 dBm.

The in-band IIP3 performance is verified across the IF by using a two-tone RF signal (1 MHz offset between tones) and an LO frequency that remains constant at 1.3 G. The input tones are swept and the IIP3 extracted for multiple IF values. The result is shown in Fig. 14. It illustrates that the in-band IIP3 performance of Chip1 increases from −28.2 dBm to −25.2 dBm by increasing the IF from 3 MHz to 95 MHz. The IIP3 performance of Chip2 increases from −29 dBm to −26.5 dBm by increasing the IF from 3 MHz to 95 MHz.

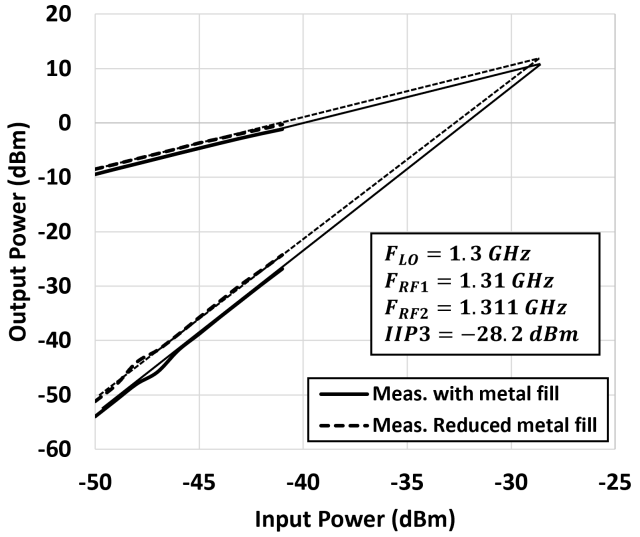

FIGURE 13. Measured fundamental and third-order intermodulation products versus the input power sweep. The resulting in-band IIP3 is shown.

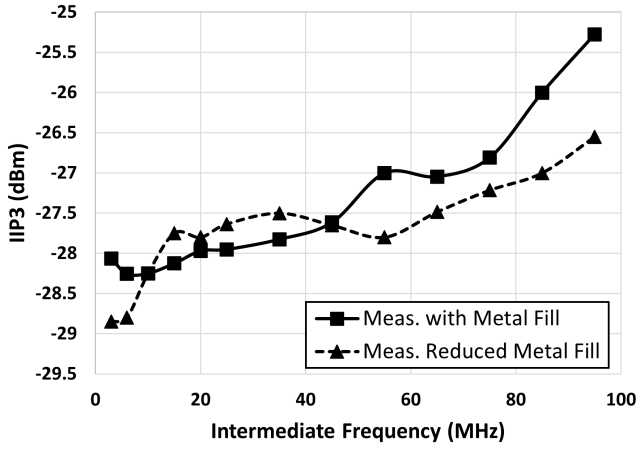

FIGURE 14. Measured in-band IIP3 performance versus the IF.

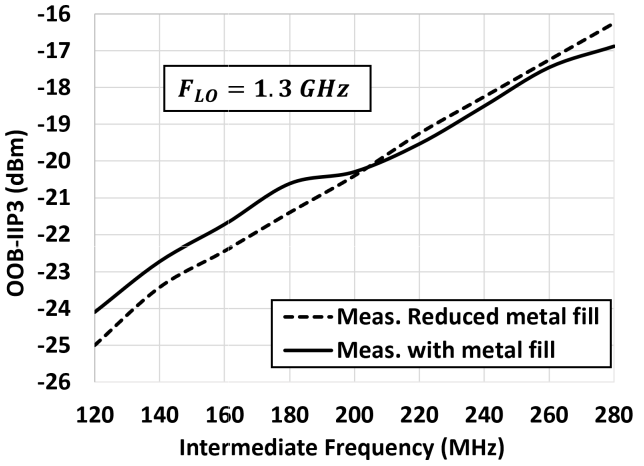

FIGURE 15. Measured OOB IIP3 performance versus the IF.

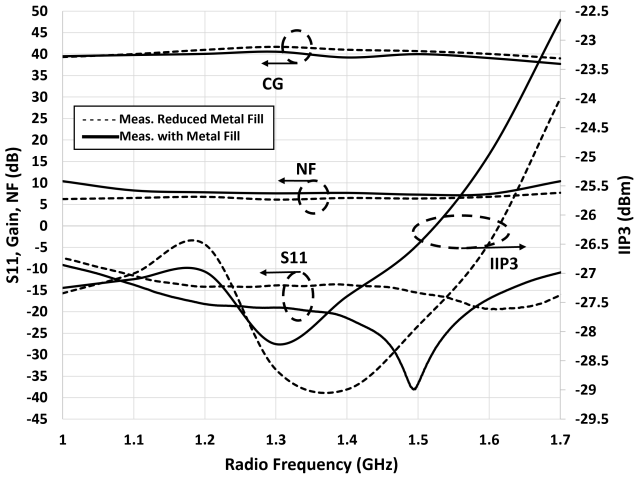

FIGURE 16. Measured receiver performance versus the RF input signal frequency.

The out-of-band (OOB) IIP3 performance is verified across the IF by using a two-tone RF signal (1 MHz offset between tones) and an LO frequency that remains constant at 1.3 GHz. The input tones are swept and the IIP3 extracted for multiple IF values. The result is shown in Fig. 15. It illustrates that the OOB IIP3 performance of Chip1 increases from −24.1 dBm to −16.9 dBm by increasing the IF from 120 MHz to 280 MHz. The OOB IIP3 performance of Chip2 increases from −25 dBm to −16.2 dBm by increasing the IF from 120 MHz to 280 MHz.

Fig. 16 shows the receiver performance across the RF range from 1 GHz to 1.7 GHz while the IF remains constant at 10 MHz. It shows the S_{11} remains below −10 dB over the entire RF range with Chip1. The S_{11} of Chip2 moved slightly to higher frequencies due to the parasitic capacitor reduction on the input nets. Both conversion gain and NF of Chip1 remain almost constant at 40.5 dB and 7.5 dB, respectively. The conversion gain and NF of Chip2 also remain almost constant at 41.5 dB and 6.5 dB, respectively. The NF of Chip2 remains constant at the RF band edge while it degrades slightly for Chip1. The IIP3 result of Chip1 improves for the frequencies above 1.3 GHz from −28.2 dBm to −22.5 dBm due to the RF signal losses at higher frequencies and reduced conversion gain. The IIP3 result of Chip2 follows the same trend and it improves for the frequencies above 1.3 GHz from −29 dBm to −24 dBm.

The performance comparison and summary of the proposed receiver with the recent literature is reported in Table 1. Note that the majority of the other designs in the table are implemented in smaller CMOS technology nodes ranging from 28 nm to 90 nm and have relatively narrow baseband bandwidths (i.e., modulation bandwidth), providing inherent advantages. This work compares well in terms of bandwidth and NF considering its technology node and power consumption. It supports a significantly wider baseband bandwidth of 90 MHz and a wide RF band of operation from 1 GHz to 1.7 GHz (i.e., in the L-band). Its area, considering the technology node utilized, also compares well with the other

TABLE 1. Performance summary and comparison.

Parameters	This Work	This Work★	TMTT 2020 [11]	JSSC 2014 [15]	JSSC 2014 [16]	MWCL 2019 [19]	JSSC 2017 [22]	IEEE 2021 [24]	JSSC 2021 [9]	JSSC 2021 [10]	JSSC 2018 [13]	TMTT 2019 [12]
Application	IoT	IoT	IoT	ZigBee	ZigBee	IoT	Bluetooth	BLE	IoT	IoT	ZigBee	BLE
Process node	130nm CMOS	130nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS	28nm CMOS	65nm CMOS	28nm CMOS	28nm CMOS	65nm CMOS	130nm CMOS
$F_{RF-High}$ (GHz)	1.7	1.7	2.48	3.55	0.96	0.92	2.8	2.48	2.9	2.8	2.48	2.48
F_{RF-Low} (GHz)	1	1	2.4	2.25	0.433	0.9	2	2.4	2.2	1.8	2.4	2.4
BB Bandwidth (MHz)	90	90	2	2	2	20	1.5	2	2	2	2	2
S11 (dB)	<-10	<-10	<-10	<-10	<-10	<-10	<-10	<-10	<-10	<-10	<-10	<-10
Gain (dB)	40.5	41.5	49.5	57	50	40.7	43.4	42	61	45	57.8	42
NF (dB)	7.5	6.5	8.2	8.5	8.1	1.94	7.8	13.2	5.5	6	15.7	7.2
In-Band IIP3 (dBm)	-28.2	-28.2	–25.75	-53	-45	-25.6	-20	-25	-46	-13	-18.5	-17
OOB IIP3 (dBm)	-24.1_-16.9	-25_-16.2	N/A	-6	-20.5	N/A	6	N/A	-7.5	5	N/A	N/A
$P_{DC}@V_{DD}$ (mW)	2@1.2	2@1.2	2.16@1.2	1@1.2	1.15@0.5	3.6@1.8	4.3@1.8	1.13@0.8	0.37@0.7	0.38@0.8	1.78@1	1.7@1.2
Active Area (mm^2)	0.54	0.54	1.16	0.3	0.2	0.559	0.4	0.85	0.5	0.2	0.45	0.7

★ This work with reduced metal fill in the vicinity of sensitive RF nodes.

works. Moreover, its projected low-cost of implementation is well suited to IoT applications, while supporting large modulation bandwidths for applications such as GNSS.

Very good performance is achieved in [10], but the receiver architecture is not suitable for wide bandwidth applications due to the sharp frequency response having a 2 MHz bandwidth at the LO frequency. Many of the other receiver architectures are not able to achieve wideband RF matching due to the LNTA topology, making them unsuitable for wideband wireless standards. Note that in some of the references, instead of in-band IIP3, only the 1-dB compression point (P1dB) is reported and it is assumed that in-band IIP3 is 10 dB higher than P1dB.

V. CONCLUSION

A low-power and wideband RF-to-BB CRR front-end was fabricated in TSMC 130 nm CMOS technology. The design was fabricated under two conditions: one is covered with metal fill at sensitive nodes (Chip1), and another has reduced metal fill on the sensitive RF nodes and blocks (Chip2). The results show almost 1 dB improvement in conversion gain and NF when the metal fill is reduced on the sensitive RF nodes and blocks. It uniquely incorporated an AI and NC circuit to the conventional CRR front-end architecture to enhance the NF performance and RF bandwidth of the receiver. The current sharing of the LNTA, AI and TIA reduced the power consumption significantly. In addition, a cross-coupled technique with a common-gate topology in the LNTA reduces the power consumption further while maintaining the receiver performance. The LNTA uses the LC-Balun to convert the single ended 50 Ω input from the antenna to a differential port with slightly lower impedance in order to allow for the LNTA to be designed with a higher transconductance, thus improving the NF and conversion gain performance.

The proposed wideband receiver front-end can be used for L-band frequency ranging from 1 GHz to 1.7 GHz. This can simplify multi-band receiver modules and lower their integration cost and overall power consumption. For instance, this receiver can be used to support the various global navigation satellite systems. In this work, the LNTA and LC-Balun were tuned to the L-band, but the design could be re-tuned to other applications.

Fundamentally, the proposed CRR front-end architecture allows relatively large CMOS technology nodes to extend their performance capabilities to higher RF operating frequencies at low-power and good NF, which can significantly reduce the implementation cost of wideband RF receivers.

ACKNOWLEDGMENT

The author would like to thank CMC Microsystems for enabling chip fabrication and providing access to the EDA tools. Also, the authors thank Sequans Communications and its supportive team in both hardware platform and RFIC departments for providing laboratory equipment and technical support during the measurements.

REFERENCES

[1] P. Marks, T. Lavender, S. Wongsaroj, and T. Hogg, "Global momentum and economic impact of the 1.4/1.5 GHz band for IMT," *GSMA Spectr.*, Feb. 2015. [Online]. Available: https://www.gsma.com/spectrum/wp-content/uploads/2015/03/Global-momentum-and-economic-impact-of-the-1.4-1.5-GHz-band-L-band-for-IMT-October-2015.pdf

[2] A. J. J. Abularach, R. C. Rodriguez, M. P. C. de Almeida, L. da Silva Mello, G. Neto, and F. Giacomini, "Coexistence of aeronautical mobile telemetry and IMT systems in the 1300–1518 MHz band," in *Proc. Int. Workshop Telecommun. (IWT)*, Jun. 2015, pp. 1–5.

[3] R. Beresik, M. Sotak, F. Nebus, and J. Puttera, "Satellite communication system's detection," *Przegląd Elektrotechniczny*, vol. 87, pp. 249–254, 2011.
[4] L. Zhang, J. Liu, and H. Jiang, "Energy-efficient location tracking with smartphones for IoT," in *Proc. IEEE Sensors*, Oct. 2012, pp. 1–4.
[5] J. T. Penttinen, *The Telecommunications Handbook: Engineering Guidelines for Fixed, Mobile and Satellite Systems*. Hoboken, NJ, USA: Wiley, 2015.
[6] D. Chen, W. Pan, P. Jiang, J. Jin, T. Mo, and J. Zhou, "Reconfigurable dual-channel multiband RF receiver for GPS/Galileo/BD-2 systems," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 11, pp. 3491–3501, Nov. 2012.
[7] S. Li, J. Li, X. Gu, H. Wang, C. Li, J. Wu, and M. Tang, "Reconfigurable all-band RF CMOS transceiver for GPS/GLONASS/Galileo/Beidou with digitally assisted calibration," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 23, no. 9, pp. 1814–1827, Sep. 2015.
[8] N. Shams, A. Abbasi, and F. Nabki, "A 3.5 to 7 GHz wideband differential LNA with GM enhancement for 5G applications," in *Proc. 18th IEEE Int. New Circuits Syst. Conf. (NEWCAS)*, Jun. 2020, pp. 230–233.
[9] B. J. Thijssen, E. A. M. Klumperink, P. Quinlan, and B. Nauta, "2.4-GHz highly selective IoT receiver front end with power optimized LNTA, frequency divider, and baseband analog FIR filter," *IEEE J. Solid-State Circuits*, vol. 56, no. 7, pp. 2007–2017, Jul. 2021.
[10] V. K. Purushothaman, E. A. M. Klumperink, R. Plompen, and B. Nauta, "Low-power high-linearity mixer-first receiver using implicit capacitive stacking with 3× voltage gain," *IEEE J. Solid-State Circuits*, vol. 57, no. 1, pp. 245–259, Jan. 2022.
[11] B. Park and K. Kwon, "2.4-GHz Bluetooth low energy receiver employing new quadrature low-noise amplifier for low-power low-voltage IoT applications," *IEEE Trans. Microw. Theory Techn.*, vol. 69, no. 3, pp. 1887–1895, Mar. 2021.
[12] M. Silva-Pereira, J. T. de Sousa, J. C. Freire, and J. C. Vaz, "A 1.7-mw −92-dbm sensitivity low-if receiver in 0.13-μm CMOS for Bluetooth LE applications," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 1, pp. 332–346, Oct. 2018.
[13] K. Wang, L. Qiu, J. Koo, R. Ruby, and B. Otis, "Design of 1.8-mW PLL-free 2.4-GHz receiver utilizing temperature-compensated FBAR resonator," *IEEE J. Solid-State Circuits*, vol. 53, no. 6, pp. 1628–1639, Jun. 2018.
[14] M. Tedeschi, A. Liscidini, and R. Castello, "Low-power quadrature receivers for ZigBee (IEEE 802.15.4) applications," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1710–1719, Sep. 2010.
[15] Z. Lin, P.-I. Mak, and R. P. Martins, "A 2.4 GHz ZigBee receiver exploiting an RF-to-BB-current-reuse blixer + hybrid filter topology in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 49, no. 6, pp. 1333–1344, Jun. 2014.
[16] Z. Lin, P.-I. Mak, and R. P. Martins, "A sub-GHz multi-ISM-band ZigBee receiver using function-reuse and gain-boosted N-path techniques for IoT applications," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 2990–3004, Dec. 2014.
[17] F. Lin, P.-I. Mak, and R. P. Martins, "An RF-to-BB-current-reuse wideband receiver with parallel N-path active/passive mixers and a single-MOS pole-zero LPF," *IEEE J. Solid-State Circuits*, vol. 49, no. 11, pp. 2547–2559, Nov. 2014.
[18] D. Ghosh and R. Gharpurey, "A power-efficient receiver architecture employing bias-current-shared RF and baseband with merged supply voltage domains and 1/*f* noise reduction," *IEEE J. Solid-State Circuits*, vol. 47, no. 2, pp. 381–391, Feb. 2012.
[19] S. Kim and K. Kwon, "A low-power RF-to-bb-current-reuse receiver employing simultaneous noise and input matching and 1/*f* noise reduction for iot applications," *IEEE Microw. Wireless Compon. Lett.*, vol. 29, no. 9, pp. 614–616, Jun. 2019.
[20] A. Abbasi, N. Shams, A. P. Kakhki, and F. Nabki, "A low-power wideband receiver front-end for NB-IoT applications," in *Proc. 18th IEEE Int. New Circuits Syst. Conf. (NEWCAS)*, Jun. 2020, pp. 50–53.
[21] A. Abbasi, N. Shams, and F. Nabki, "A 0.8–3.4 GHz, low-power and low-noise RF-to-BB-current-reuse receiver front-end for wideband local and wide-area IoT applications," in *Proc. 27th IEEE Int. Conf. Electron., Circuits Syst. (ICECS)*, Nov. 2020, pp. 1–4.
[22] M. Ramella, I. Fabiano, D. Manstretta, and R. Castello, "A SAW-less 2.4-GHz receiver front-end with 2.4-mA battery current for SoC coexistence," *IEEE J. Solid-State Circuits*, vol. 52, no. 9, pp. 2292–2305, Sep. 2017.
[23] B. Razavi, "The active inductor [a circuit for all seasons]," *IEEE Solid State Circuits Mag.*, vol. 12, no. 2, pp. 7–11, Jun. 2020.
[24] B. Park and K. Kwon, "2.4 GHz BLE receiver with power-efficient quadrature RF-to-baseband-current-reuse architecture for low-power IoT applications," *IEEE Access*, vol. 9, pp. 62734–62744, 2021.
[25] C. J. Jeong, Y. Sun, S. K. Han, and S. G. Lee, "A 2.2 mW, 40 dB automatic gain controllable low noise amplifier for fm receiver," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 2, pp. 600–606, Feb. 2015.
[26] B. Razavi, *RF Microelectronics: Pearson New International Edition*. London, U.K.: Pearson Education, 2013.
[27] N. Shams and F. Nabki, "Analysis and comparison of low-power 6-GHz N-path-filter-based harmonic selection RF receiver front-end architectures," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 30, no. 3, pp. 253–266, Mar. 2022.

ARASH ABBASI received the B.Sc. degree in electrical engineering from Islamic Azad University, in 2011 and the M.Sc. degree in electronic engineering from University Putra Malaysia, in 2015, where he worked on radio frequency integrated circuits (RFIC). After that, he was working for four consecutive years at Symmid Corporation as a Senior Analog Designer. He joined the Institute for Microelectronics, in February 2019, where he was working as a Project Assistant, with a focus on the characterization and modeling of noise in Si technology. He is currently working on his Ph.D. thesis at École de Technologie Supérieure while he is working as a Senior RFIC Design Engineer at Sequans Communications. His research interest is analog RFIC design specifically developing low-power and wideband receiver front-ends.

AMIR HOSSEIN MOSHREFI (Graduate Student Member, IEEE) received the B.Sc. and M.Sc. degrees in electrical engineering from the Amirkabir University of Technology, Iran, in 2012 and 2014, respectively, and the Ph.D. degree in electronics (circuit and system) from the Nano-Electronics Center of Excellence, University of Tehran, Iran, in 2021. He is currently pursuing the Ph.D. degree with the École de Technologie Supérieure (ETS), Canada. He was a Lecturer with the University of Tehran, in 2017 for two years. He was a Visiting Researcher with the Institute for Microelectronics, TU-Wien, Austria, about the compact modeling of bias temperature instabilities (BTI) for reliability of integrated digital circuits, in 2019.

FREDERIC NABKI (Member, IEEE) received the B.Eng. degree (Hons.) in electrical engineering and the Ph.D. degree in electrical engineering from McGill University, Montreal, QC, Canada, in 2003 and 2010, respectively.

In 2008, he joined the Université du Queébec à Montreéal (UQAM), Montreal, where he was an Associate Professor in microelectronics engineering. In 2016, he joined the École de Technologie Supérieure (ETS), Montreal, where is currently a Full Professor with the Department of Electrical Engineering. He jointly manages the Microtechnology and Microsystems Laboratory of ETS. He has authored two book chapters and over 150 publications. He holds 37 issued patents on applications related to MEMS, ICs, and CMOS/MEMS monolithic integration. His research interests include microelectromechanical systems (MEMS) and RF/analog microelectronics, specifically focusing on the creation of next-generation MEMS processes using advanced materials, the integration of MEMS devices with CMOS systems, the modeling of MEMS devices, and the design of CMOS phase-locked loops, ultra-wideband transceivers, and MEMS interface circuits.

Dr. Nabki is currently a member of the Quebec Order of Engineers. He served as the Secretary and Treasurer for the Montreal Section of the IEEE. He was a recipient of the Governor General of Canadas Academic Bronze Medal, the IEEE Canada J. J. Archambault Eastern Canada Medal, the UQAM Faculty of Science Early Career Research Award, and the ETS Board of Directors Research Excellence Prize. He holds or has held financial support from the Microsystems Strategic Alliance of Quebec, the Quebec Fund for Research in Nature and Technology, the Natural Sciences and Engineering Research Council of Canada, and the Canada Foundation for Innovation.