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A Comparison of Off-Chip Differential and LC Input Matching Baluns in a Wideband and Low-Power RF-to-BB Current-Reuse Receiver Front-End

Arash Abbasi * and Frederic Nabki

École de Technologie Supérieure (ÉTS), Montreal, QC H3C1K3, Canada
* Correspondence: arash.abbasi.1@ens.etsmtl.ca

Abstract: A wideband and low-power RF-to-baseband (BB) current-reuse receiver (CRR) front-end is proposed, and its performance is verified using two matching networks, one with an LC balun and on-chip biasing inductor, CRR1, and another with a differential balun and without on-chip biasing inductor, CRR2, requiring less area. The transimpedance amplifier (TIA) and low-noise transconductance amplifier (LNTA) share the bias current from a single supply to reduce power consumption. It employs both an active-inductor (AI) and a $1/f$ noise-cancellation technique to improve the NF and RF bandwidth performance. A passive mixer is utilized for RF to BB conversion, which does not require any DC power and voltage headroom. Both CRR1 and CRR2 are fabricated in TSMC 130 nm CMOS technology on a single die and packaged using a QFN48. CRR1 occupies an active area of 0.54 mm^2. From 1 to 1.7 GHz, it achieves a conversion gain of 41.5 dB, a double-sideband (DSB) NF of 6.5 dB, S_{11} <-10 dB, and an IIP3 of -28.2 dBm, while the local-oscillator (LO) frequency is at 1.3 GHz. CRR2 occupies an active area of 0.025 mm^2. From 0.2 to 1 GHz, it achieves an average conversion gain of 37 dB, an average DSB NF of 8 dB, and an IIP3 of -21.5 dBm while the LO frequency is at 0.7 GHz. Both CRR1 and CRR2 consume 1.66 mA from a 1.2 V supply voltage.

Keywords: LC balun; differential balun; current-reuse receiver (CRR); cross-coupled common-gate (CCCG) low-noise transconductance amplifier (LNTA); wideband; low-power; matching network

Citation: Abbasi, A.; Nabki, F. A Comparison of Off-Chip Differential and LC Input Matching Baluns in a Wideband and Low-Power RF-to-BB Current-Reuse Receiver Front-End. *Electronics* **2022**, *11*, 3527. https://doi.org/10.3390/electronics11213527

Academic Editors: João Paulo Pereira do Carmo, Manuel Fernando Silva and Graça Minas

Received: 22 September 2022
Accepted: 27 October 2022
Published: 29 October 2022

1. Introduction

Growth in the Internet of Things (IoT) market led both academia and industry to invest on developing low-power and wideband transceivers to cover a wide RF spectrum and several wireless standards with minimum power consumption. One of the challenges is to design a receiver front-end that can cover several RF bands by minor modifications on the input matching network. In this way, design times, costs, and verification times can be reduced. However, designing a receiver front-end with low-power consumption and wideband RF coverage is an added challenge.

A well-known method to design low-power circuits is the current-reuse technique, which is conventionally used to design low-noise transconductance amplifiers (LNTAs) [1]. In [2], a push–pull LNTA is used in a cascaded receiver to reduce the power consumption. However, it reports a poor 1 dB compression point (P1dB) of -56 dBm. A stacked baseband amplifier is employed in a mixer first receiver architecture in [3] that achieves very low power consumption. However, it has limited bandwidths due to the mixer's first architecture that makes it unsuitable for wideband modulation schemes. A quadrature low-noise amplifier (LNA) followed by poly-phase filter (PPF) is employed in [4] to improve power efficiencies. However, it suffers form a narrow RF bandwidth due to the common-source LNA topology. Another approach in [5], employs a current-reuse LNA followed by an on-chip LC-balun and a passive PPF to reduce the dynamic power consumption in the LO signal path. However, the combination of the on-chip LC balun followed by PPF limits the bandwidth, which is not suitable for wideband applications. In [6], a free phase-locked loop (PLL) receiver

architecture is proposed, but the reported NF of 15.7 dB is very high. Recently, thanks to the scaling down in CMOS technology, where the voltage threshold (V_{TH}) reduced and the transition frequency (f_T) increased, the current-reuse technique is employed to design a receiver front-end by stacking different blocks and to share the bias current from a single supply to reduce the overall power consumption in comparison to the conventional approach in which circuits are cascaded with separate supply currents, as shown in Figure 1.

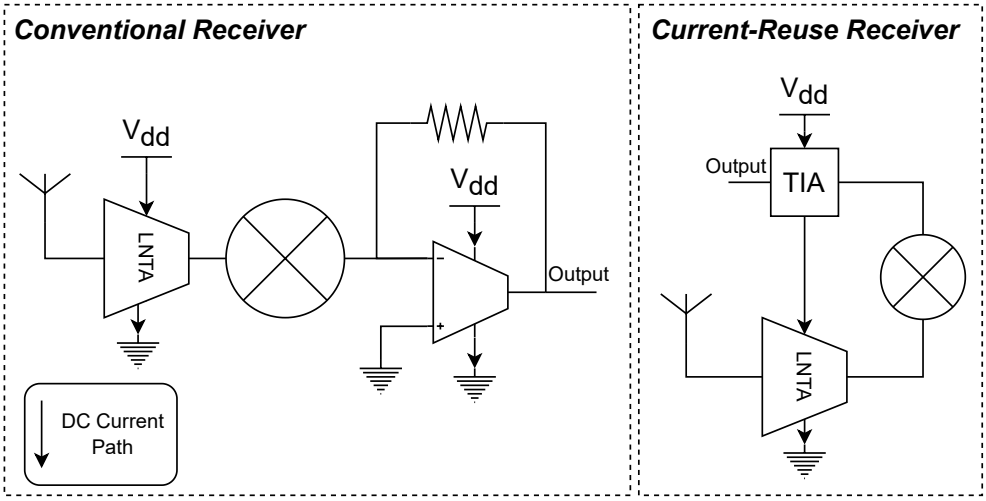

Figure 1. Conventional (**left**) and current-reuse (**right**) receiver architectures.

A wide range of studies has been performed on designing low-power receivers using the current-reuse technique. The low-noise amplifier (LNA), down-conversion mixer, and voltage-controlled oscillator (VCO) are stacked in [7] to share a single supply and bias current, which achieve very low power consumption. However, the reported NF of 10 dB is high. Moreover, it may suffer injection locking of the VCO. In [8], the LNTA, active mixer, and baseband (BB) filter are cascoded. Its choice of an active mixer increases the voltage's headroom requirement to achieve high linearity. In [9], a function-reuse method is employed where a push–pull amplifier functions as both the LNTA and TIA. However, a low supply voltage results in a poor P1dB performance of −50 dBm. Moreover, the circuit is mainly suitable for sub-GHz applications due to the limited RF bandwidth. An N-path current-reuse receiver is another alternative that is also suitable for sub-GHz applications [10]. One of the issues in N-path receivers is the requirement for additional circuitry to combine the N paths that require additional power consumption and area. Moreover, the active mixer used requires more voltage headroom. A $1/f$ noise-cancellation (NC) technique and linearity enhancement method is utilized by [11], but it consumes a relatively high 8 mW. A current-reuse technique is used in [12] by sharing the VCO current with the LNA and PA. Moreover, a function-reuse mixer is employed that reduces the overall power consumption. However, the stacking of the VCO on the LNA and PA may cause problems with VCO locking. Another approach is to employ a method of simultaneous input matching and a $1/f$ NC technique that results in a very low NF of 1.94 dB [13] at the cost of very limited RF bandwidth. Both current-reuse receiver (CRR) circuits proposed in [13,14] share the output node with the down-conversion mixer input, which causes loading and a loss of the RF signal. In our earlier works [15–18], the concept of an active-inductor (AI) and a $1/f$ NC technique was introduced to overcome the problems mentioned above. The AI circuit helps isolate the output node from the mixer input. In addition, the $1/f$ NC technique pushes the $1/f$ noise corner below 1 MHz.

This work mainly employs the quadrature (I/Q) low-power and wideband RF-to-BB CRR front-end proposed in [17] to assess its functionality with different matching circuits over a wide frequency range. It evaluates the performance of the LNTA using both a differential balun without an on-chip biasing inductor and an LC balun with an on-chip

biasing inductor. The RF-to-BB CRR employs both an AI and $1/f$ NC to improve the gain and NF performance by isolating the RF signal from the output node and removing the common-mode low frequency noise. It utilizes a wideband cross-coupled common-gate (CCCG) topology to convert the RF voltage to an RF current, and a 25% down-conversion passive mixer is used to convert the RF current to a BB current without consuming the DC current. Finally, it converts the BB current to the BB voltage using a TIA circuit that shares the DC current with the LNTA to reduce power consumption.

This study shows that the proposed CRR is well-suited for different matching circuits over a wide RF range and discusses both input matching methods and their impact on performance. Notably, a structure with a differential balun and without an on-chip biasing inductor is studied, having a reduced area in comparison to what was proposed in [17].

The paper is structured as follows. Section 2 overviews the receiver front-end architecture and provides a detailed description of the front-end circuitry, and Section 3 presents the measurement results. This is followed by a conclusion.

2. RF-to-BB-Current-Reuse Receiver Front-End Circuit-Level Considerations

Scaling down the CMOS technology node improves the frequency of operation and reduces the V_{TH} of the transistors. This allows for the stacking of circuits to share the bias current using a single supply. This introduces several design challenges to maintain the overall performance, which was studied in our earlier work [17]. In reality, designing a receiver front-end requires time and cost. It would be very efficient to design a receiver front-end that can be used for several frequency bands with minor adjustment in the input matching network. Moreover, a receiver compatible with different matching networks helps reuse the receiver for applications having different requirements.

The block diagram of the circuit proposed in [17], CRR1, and the block diagram of the proposed circuit in this work, CRR2, are shown in Figure 2. CRR2 does not include an internal biasing inductor for the DC current path and uses an external differential balun. Both circuits include the LNTA, which mainly defines the receiver performance, the down-conversion passive mixer to reduce the DC power consumption, and the voltage headroom required; the AI and $1/f$ NC circuits that are used to improve the NF performance; and the TIA that converts the BB current to the BB voltage at the output. The TIA shares the current with the LNTA to reduce the power consumption.

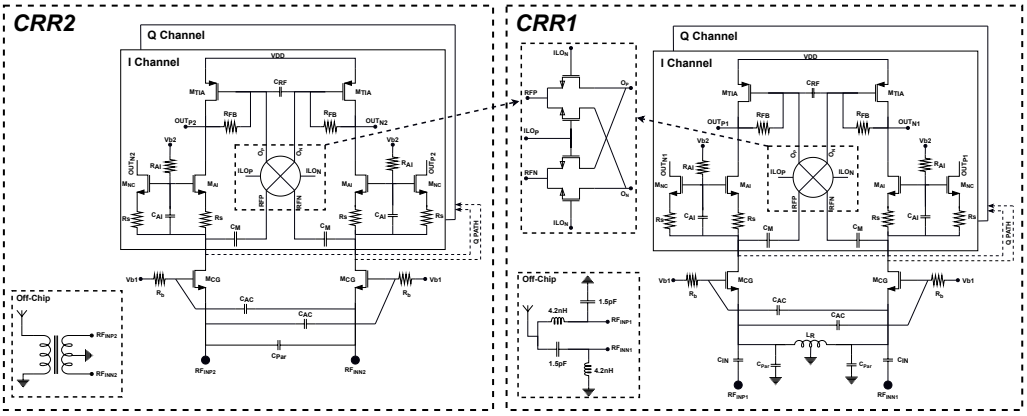

Figure 2. CRR1 proposed in [17] (**right**) and CRR2 proposed in this work (**left**).

2.1. LNTA Design with Differential Balun and LC Balun Input-Matching Network

The LNTA is the first stage in the receiver front-end which defines the sensitivity and amplifies the weak input signal before down-conversion. There are two well-know topologies to design the LNTA circuit: the common-gate (CG) and the common-source (CS). In [13], a common-source topology was used, which results a very low NF at the cost of narrow bandwidth. However, the CS topology is very sensitive to non-idealities such as wire-bonding, reducing the design robustness of the LNTA. On the other hand,

the CG topology is well-known for its design robustness and wideband operation, but it has a higher NF. It provides input matching via $1/g_m$ that can be achieved by optimizing the current and the W/L ratio [19]. However, the CG topology requires high currents to achieve the required g_m. To overcome this issue, a cross-coupled technique is employed to boost the effective g_m by two times without consuming extra DC currents. This results in achieving the required input matching, NF, and gain. Moreover, this cross-coupling avoids using large transistors to achieve the required g_m, which results in less parasitics that reduce the RF signal losses and improve NF. In this work, a CCCG LNTA is used with wideband input matching and allows for higher robustness at the cost of higher NF.

In Figure 2, the CCCG LNTA is formed by M_{CG} and the cross-coupled connection of C_{AC}. The NF is given by the following:

$$F \cong 1 + \frac{\gamma}{4\alpha} \cdot \frac{1}{R_S g_m} + \frac{R_{Balun}}{R_S}, \tag{1}$$

where α and γ are the bias-dependent noise parameters, and R_S is the source resistance. The balun losses can be modeled by series resistor R_{Balun}. γ/α is reduced by increasing the channel-length slightly but it maintains an f_T that is at least ten times higher than the frequency of operation.

To perform input matching using a 1:1 differential balun, $R_S = 1/2g_m$ is designed for it. Then, the second term in (1) increases by two times. The noise factor is then given by the following.

$$F \cong 1 + \frac{\gamma}{2\alpha} + \frac{R_{Balun}}{R_S}. \tag{2}$$

Compared to the differential balun, the LC balun converts the 50 Ω antenna impedance to the required impedance (in this work, 25 Ω) on the differential side. In this way, the LNTA can be designed with a higher g_m while maintaining the input matching performance and reducing the NF. In this way, the LNTA noise is given by the following.

$$F \cong 1 + \frac{\gamma}{4\alpha} + \frac{R_{Balun}}{R_S}. \tag{3}$$

The LNTA with a differential balun can be designed with a 25 Ω input impedance but at the cost of poor input matching.

In this work, the LNTA is designed using an LC balun and a differential balun at its input in CRR1 and CRR2, respectively.

The single-ended antenna input needs to be converted to a differential signal at the input of the LNTA. CRR1 employs an off-chip LC balun to convert the single-ended signal to a differential one. Moreover, an on-chip inductor, L_R, is used to provide the DC current path and resonates with large parasitic capacitors, C_{Par}, at the input of the LNTA. L_R helps reduce RF signal losses and allows the receiver to operate at higher frequencies, as will be later shown in the measurements. Although the LC balun is well-known for its narrow band operation, its combination with the CG LNTA topology provides wideband input impedance matching [15]. Alternatively in CRR2, an off-chip single to differential balun is utilized. The balun provides the DC current path that removes the need for the on-chip inductor that requires a significant die area. However, it suffers from high RF signal losses due to the parasitic capacitances that did not resonate as in CRR1, reducing its operating frequency range capabilities.

The LC balun and LNTA in CRR1 are tuned to operate from 1 GHz to 1.7 GHz. CRR2 is designed over a similar frequency range to compare with CRR1, but its input matching strategy will nonetheless reduce its operating frequency range.

2.2. Active-Inductor and 1/f Noise-Cancellation Technique

Conventionally, CRRs use cascode devices to boost the output impedance and isolate the I/Q paths [13,15]. However, they suffer from RF signal losses due to the sharing of

the mixer input with the output node that has large capacitive loading. Moreover, the $1/f$ noise from the LNTA is directly coupled to the output via the cascode transistor, despite the conventional receiver architecture that uses an AC-coupling capacitor before the mixer to remove low frequency components. To overcome the issues mentioned above, our earlier works [14,16,17] proposed the AI and $1/f$ NC circuits.

The AI circuit helps isolate the passive mixer input from the output node to avoid RF losses due to the loading of the output node, which helps improve the NF and gains at higher frequencies even in a relatively large technology node, such as 130 nm CMOS.

Figure 3a shows the conventional AI proposed in [20]. The AI is formed by M_{AI}, R_{AI}, and C_{AI}. The impedance looking into the AI circuit is small at low frequencies to pass the DC current while it kept increasing and moving towards high frequencies. The impedance with respect to the circuit shown in Figure 3a is given by the following:

$$Z_{AI}(s) \cong \frac{R_{AI}C_{AI}s+1}{g_{m,AI}+C_{AI}s} || \frac{1}{sC_{par}}, \tag{4}$$

where C_{par} is the parasitic capacitance at the mixer input. C_{par} is dependant on the technology node.

A small resistor, R_S, is added to boost the impedance looking into the AI circuit at the cost of voltage headroom, as shown in Figure 3b. The impedance looking into the AI circuit Z_{AI} is then calculated by the following.

$$Z_{AI}(s) \cong \frac{g_{m,AI}R_S(R_{AI}C_{AI}s+1)+R_{AI}C_{AI}s}{g_{m,AI}R_SC_{AI}s+g_{m,AI}+C_{AI}s} || \frac{1}{sC_{par}}, \tag{5}$$

Appendix A derives (5). The mathematical model of $|Z_{AI}|$ from (5) with a C_{par} value of 30 fF is plotted versus the frequency along with simulation results in Figure 4, where g_m is of 3.5 mS, C_{AI} is of 1 pF, R_{AI} is of 30 kΩ, and R_S is of 200 Ω. For high values of g_m, the low frequency impedance in (5) is equal to R_S if channel-length modulation is ignored.

As mentioned previously, the LNTA $1/f$ noise is directly coupled into the CRR output since the AI circuit does not block low frequencies. To suppress the resulting low frequency noise, a $1/f$ NC circuit is used. M_{NC} provides the signal path to the output with the opposite sign to cancel the low frequency noise and push the $1/f$ corner to a lower frequency.

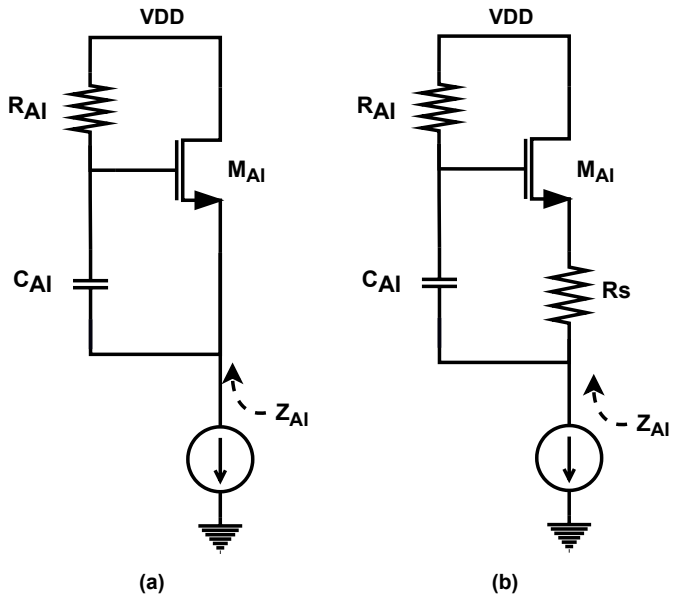

Figure 3. (**a**) Conventional and (**b**) active-inductor with R_s.

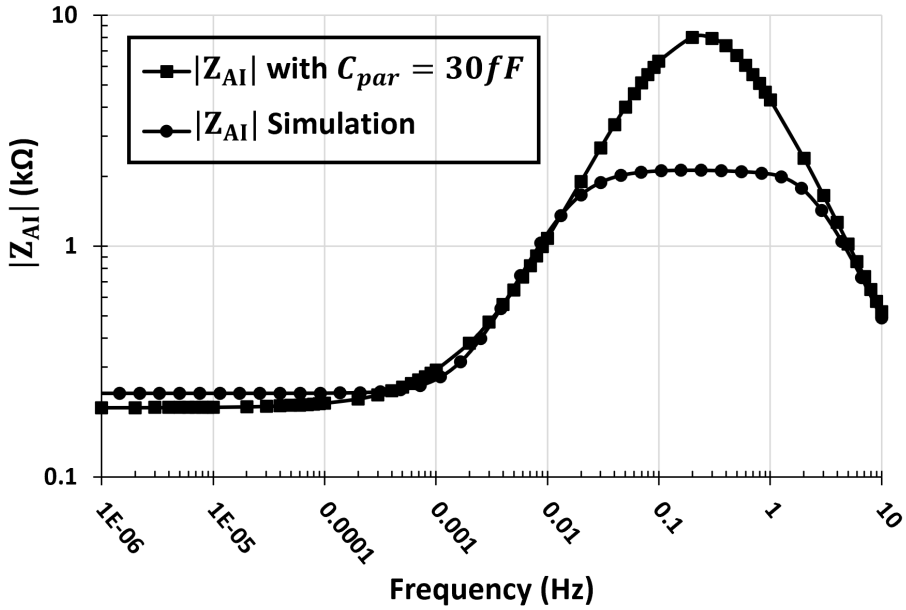

Figure 4. Mathematical model of Z_{AI} looking into the active-inductor with R_S included and C_{par} of 30 fF along with circuit simulation results.

2.3. Passive Mixer

The RF current from the LNTA needs to be down converted to the BB current before the TIA and BB circuits. To this end, both active and passive mixer structures can be employed. Usually, the passive mixer is preferred over the active mixer since the active mixer suffers from both a voltage headroom issue and a direct coupling of low frequency noise.

Accordingly, a 25% double balanced passive mixer is employed to down convert the RF current from the LNTA to a BB current without DC power consumption and no voltage headroom limitation. The mixer should have an input impedance that is much smaller than that of the LNTA output impedance in order to ensure lower NF and higher gain. Moreover, a low input impedance reduces the voltage gain at the input of the mixer, which improves linearity. Thus, it is important to optimise switch sizes in a way that achieves low input impedance, while maintaining a sufficiently small parasitic capacitance to avoid RF signal losses. The gate of the mixer switches need to be biased such that the LO signal switches on and off the mixer completely. The voltage bias of the source and drain terminal of the mixer switches is provided by the TIA. The rail-to-rail voltage of the LO signal should not exceed the transistor breakdown, and a voltage that is similar to the supply or lower is preferred.

2.4. Transimpedance Amplifier

The TIA is formed by a single transistor, M_{TIA}, and feedback resistor, R_{FB}. It converts the BB current to the BB voltage at the output. A large channel-length is preferred for M_{TIA} to enhance the output impedance. The simplified equation of the conversion gain is given by the following:

$$gain \cong \frac{2\sqrt{2}}{\pi} g_{m,eff} R_{FB}, \tag{6}$$

where $g_{m,eff}$ is two-times the transconductance of transistor M_{CG}.

3. Experimental Results and Discussions

The wideband and low-power current-reuse receiver front-end was fabricated in a TSMC 130 nm CMOS process, and the die micrograph is shown in Figure 5, occupying a total area of 1.2 mm × 1.2 mm. The on-chip current-mode logic (CML) buffer provides output matching to measure the performance of the CRR using a spectrum analyzer (Agilent N9020A), as shown in Figure 6. The CML buffer needs to consume a high power of 48 mW so that the CRR performance is maintained, notably its linearity. The current bias

needs to be adjusted to achieve a transconductance for M_1 that yields a 0 dB gain given by $g_{m1} \times 50\,\Omega$. The required transconductance can be reduced by half if the output impedance is doubled. This helps reduce the effect of parasitic capacitors and increases the bandwidth of the CML buffer. In this way, to match the 100 Ω output impedance of the CML buffer with the spectrum analyzer, a 2:1 differential to single-ended balun is required and losses need to be taken into account during measurements. In addition, the cascode transistor, M_2, enhances the output impedance and reduces the miller effect to increase the bandwidth. The large AC-coupling capacitor, C_{AC}, is used to separate the CML buffer biasing from the CRR's output voltage. Both CRR and CML buffers utilize a 1.2 V supply.

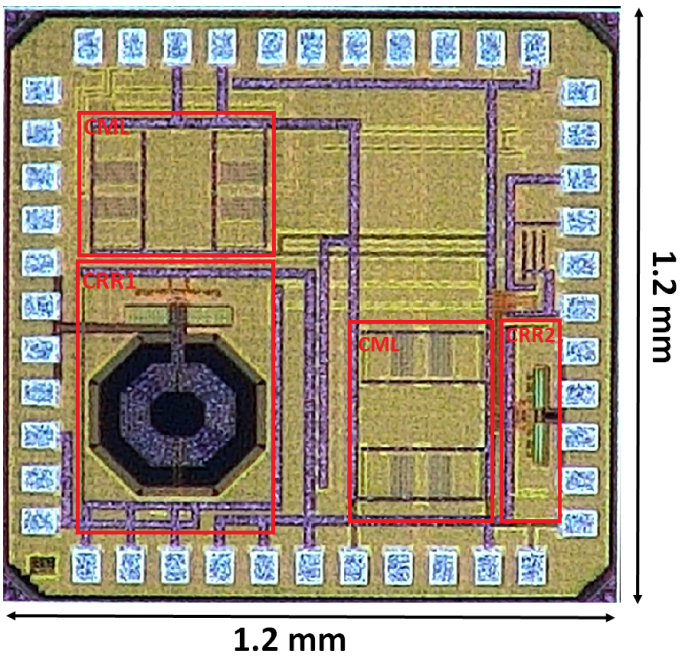

Figure 5. Die micrograph.

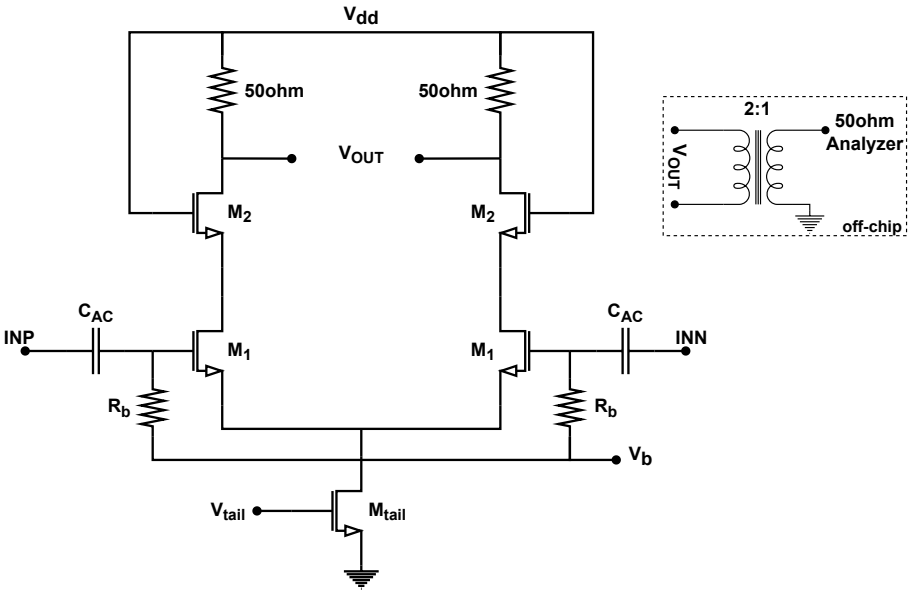

Figure 6. The CML buffer circuit used to drive the measurement equipment in a matched state.

As previously discussed, the performance of the circuit is characterized using two different input matching networks: (i) a differential balun (TCM1-63AX-2+) and (ii) a

custom-designed LC balun. This outlines the robustness of the circuit, along with its operation over a wide RF band with the two input matching methods utilized.

For this purpose, as shown in Figure 2, two CRR topologies were implemented in this work: one with an on-chip inductor, CRR1, which occupies an active area of 0.54 mm^2 and is measured using an LC balun at its input, and the other without an on-chip inductor, CRR2, that occupies a much smaller active area of 0.025 mm^2 and is measured with a differential balun at its input. These active areas exclude the CML buffer and bond pads. Both CRR1 and CRR2 consume 1.66 mA from the 1.2 V supply. This identical current biasing is selected to provide a representative comparison of both presented circuits.

The chip is packaged in a QFN48, and it is connected to the PCB using a socket (SG-MLF-7006). Non-idealities related to the cable, socket, and external output balun are carefully considered. To this end, the S-parameter characteristics of the cables and baluns are extracted using a four-port vector network analyzer (VNA) (Rohde and Schwarz ZVB-8). The socket losses are provided by the manufacturers' datasheet. Two signal generators (Agilent N5182a MXG) were used to generate the input signal and the clock signal for the down-conversion mixer switches. For the measurement, the differential output of the CML buffer is converted to a single-ended output to the spectrum analyzer using an external 2:1 balun. Figure 7 shows the measurement setup using a VNA to measure the S_{11} performance of CRR1 and CRR2. The power supply shows that both CRR1 and CRR2 consume 3 mA together while their CML buffers powered down.

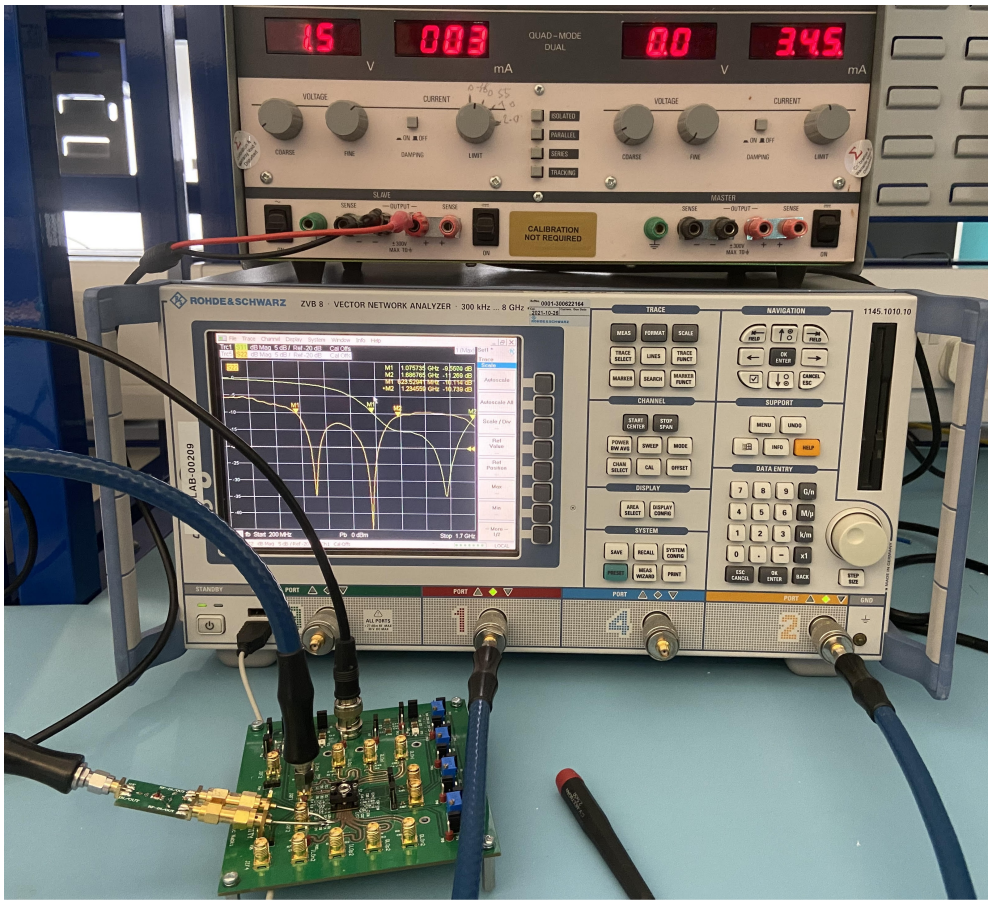

Figure 7. Measurement setup using a VNA to evaluate the S_{11} performance of CRR1 and CRR2. The voltage shown on the power supply is applied to the LDO on the PCB that in turn provides the 1.2 V supply to the chip.

There are several methods to measure the NF performance of the receiver. In this work, the Y-factor method, which utilizes a noise source, is employed with high accuracy. The NF performance of CRR1 and CRR2 is measured across the RF input and is shown in Figure 8.

The NF remains below 8 dB over the RF from 1 to 1.7 GHz in CRR1. However, the NF is increasing from 6 to 10.5 dB with the RF proceeding from 0.2 to 1 GHz in CRR2. This is thanks to the on-chip inductor used in CRR1 that resonates with C_{Par} at the frequency of operation, which reduces RF signal losses and allows CRR1 to maintain its NF performance at higher frequencies. However, this comes at the cost of a larger chip area for CRR1 due to its on-chip inductor. The performance of both CRR1 and CRR2 is verified across the IF while the LO frequency is constant at 1.3 GHz and 0.7 GHz, respectively, and the results are shown in Figure 9. The low frequency noise is suppressed and the $1/f$ corner noise is pushed to a low frequency of less than 1 MHz thanks to the $1/f$ NC circuit.

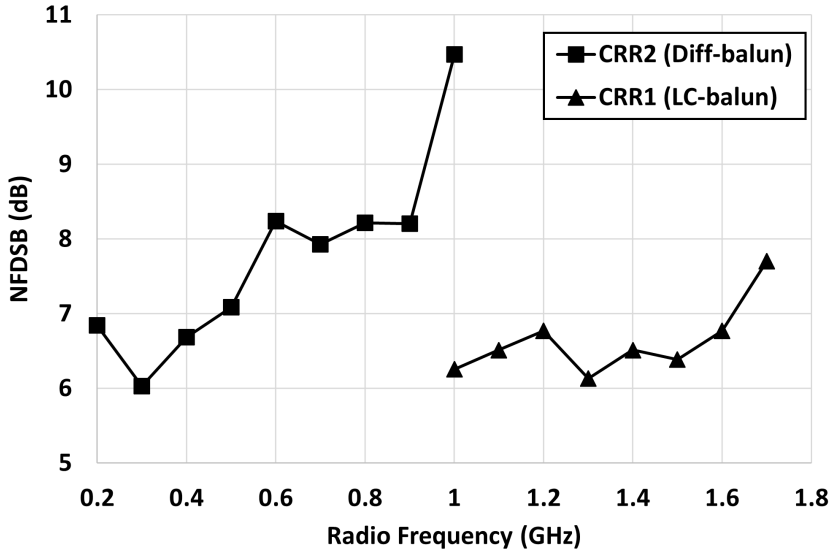

Figure 8. The NF performance CRR1 and CRR2 versus the RF input.

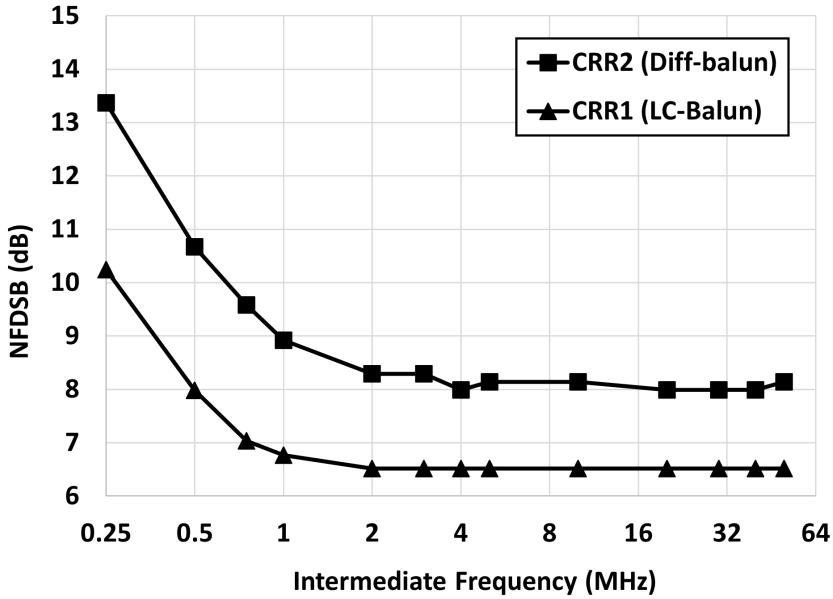

Figure 9. The NF performance of CRR1 and CRR2 versus the IF.

A low-power RF signal with a 5 MHz frequency spacing from the LO frequency is applied to the input to calculate the conversion gain from the output signal power at BB (in dBm) minus the power of the input signal at RF. The measured conversion-gain performances versus the RF input is shown in Figure 10. Relative to the NF performance shown in Figure 8, the conversion gain in CRR2 reduces from 39.5 to 33 dB over the RF input range from 0.2 to 1 GHz while CRR1 maintained its conversion-gain performance of

about 40 dB over the entire RF band from 1 to 1.7 GHz. The conversion-gain performance is also measured across the IF while the LO is constant at 1.3 GHz in CRR1 and 0.7 GHz in CRR2. The resulting conversion gain curves are plotted in Figure 11. The bandwidths of both CRR1 and CRR2 remain almost the same since they use the same AI, $1/f$ NC, passive mixer, TIA, and CML buffer. In this figure, CRR1 achieves almost 4.5 dB-higher gain than CRR2 due to the higher loss of the differential balun and the lack of on-chip inductor to resonate with the paracitic capacitors at the input of the receiver.

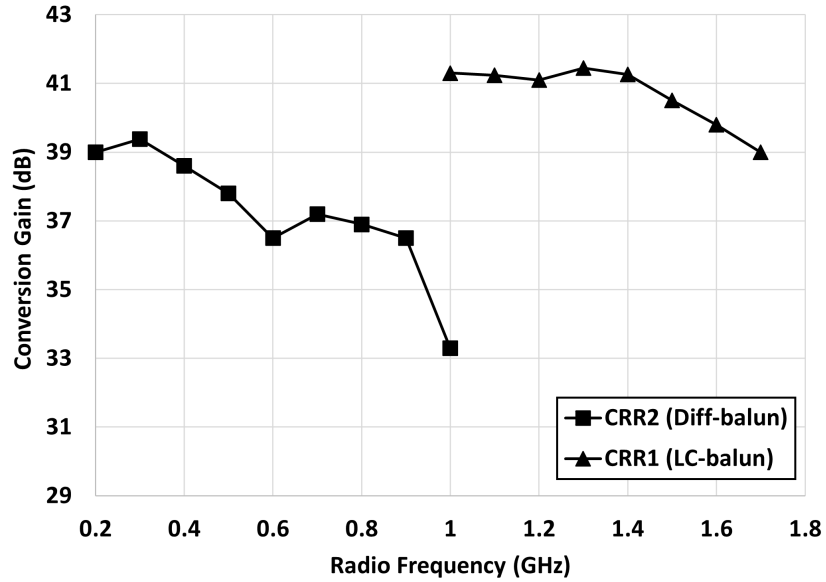

Figure 10. The conversion-gain performance of CRR1 and CRR2 versus the RF input.

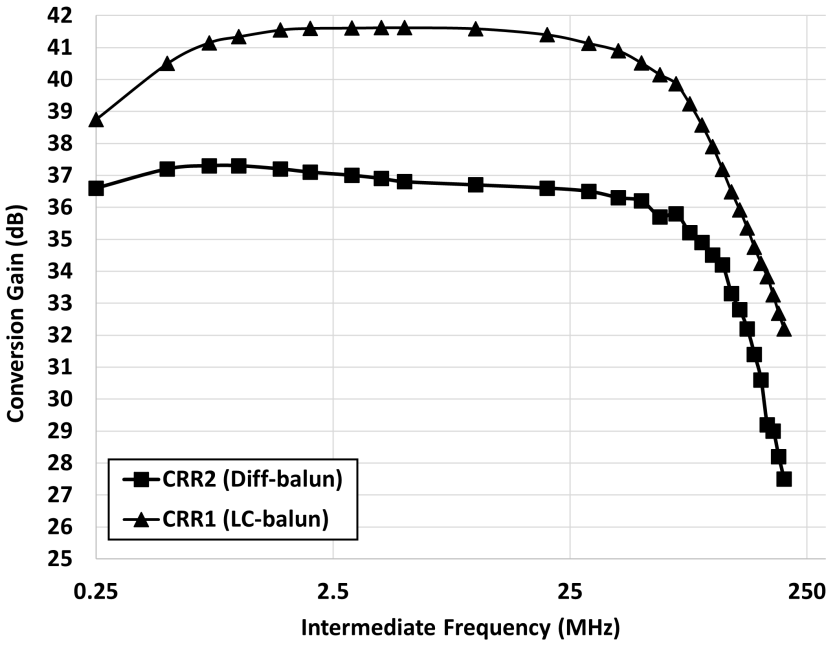

Figure 11. The conversion-gain performance of CRR1 and CRR2 versus the IF.

The S_{11} performance of both CRR1 and CRR2 is measured versus the RF input using a VNA, and the results are shown in Figure 12. It illustrates that CRR1 with the LC balun achieves an $S_{11} < -10$ dB over a wide RF bandwidth from 1.1 to 1.7 GHz. CRR2 achieves an $S_{11} < -10$ dB over a band of 0.6 to 1.2 GHz. Although S_{11} is higher than -10 dB for frequencies below 0.6 GHz in CRR2, due to the reduced parasitic capacitor contribution at lower frequencies, resulting in reduced RF loss, it could nonetheless maintain a good

NF and conversion gain. At 0.2 GHz, the S_{11} is −6.2 dB, which is equivalent to the a mismatch-induced loss of 1.2 dB.

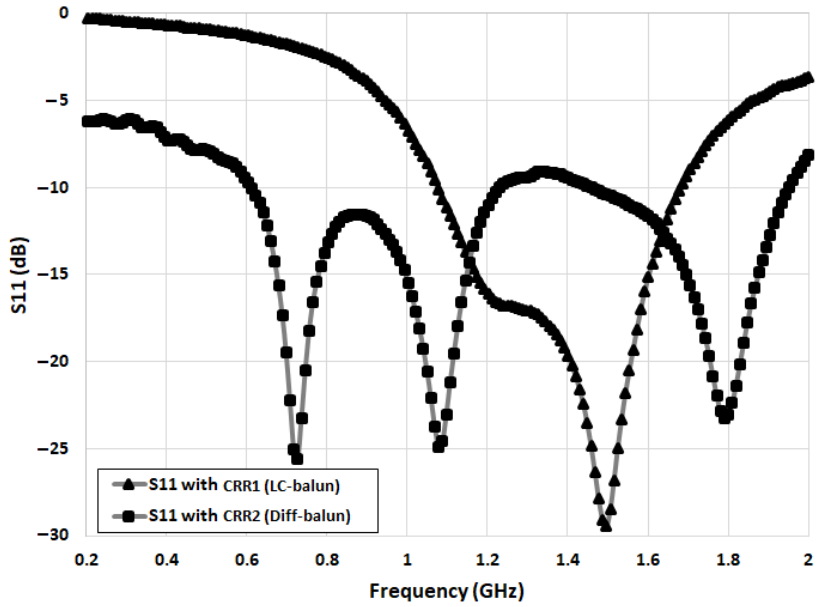

Figure 12. The S11 performance of CRR1 and CRR2 versus the RF input.

The linearity performance of CRR1 and CRR2 is characterized using P1dB and the in-band third-order intercept point (IIP3). The P1dB measurement is performed by applying a single input tone that is 5 MHz offset from the LO signal, where the signal power is swept from −50 to −20 dBm. This is performed when the LO signal is at 1.3 GHz in CRR1 and 0.7 GHz in CRR2. The resulting output power versus the input power is plotted in Figure 13. It shows that CRR1 achieves an input P1dB of −35.5 dBm, while CRR2 achieves a higher input P1dB of −31 dBm, which is relative to the gain difference reported above.

The IIP3 performance is evaluated using a two-tone test applied to the input with 10 MHz and 11 MHz offsets from the LO signal, while the LO frequency is at 1.3 GHz in CRR1 and 0.7 GHz in CRR2. The input power swept from −50 to −35 dBm. This generates two fundamental tones of 10 MHz and 11 MHz along with two intermodulation products of 9 MHz and 12 MHz at the output. The output fundamental tone and the third-order intermodulation products are plotted versus the input power in Figure 14. It illustrates that CCR1 achieves an IIP3 of −28.2 dBm, while CRR2 achieves an IIP3 of −21.5 dBm. Note that there may be a few dBs of uncertainty in the IIP3 results since the CML buffer may limit the linearity.

The overall performance summary of CRR1 and CRR2 along with a comparison to other works using a current-reuse topology is reported in Table 1. The results show that CRR2 operates at lower frequency compared to CRR1 in our earlier work. Otherwise, the overall performance remains similar. Notably, in CRR2, the conversion gain is reduced and the NF increased, but linearity is improved. Moreover, CRR2 achieves a higher bandwidth of 110 MHz compared to CRR1 (90 MHz).

Overall, this circuit topology, in either of the forms presented, achieved a high BB bandwidth, making it suitable for wide modulation bandwidth applications. The NF, IIP3, and bandwidth performances compare well with the state-of-the-art methods considering the power consumption and technology node of the presented receivers.

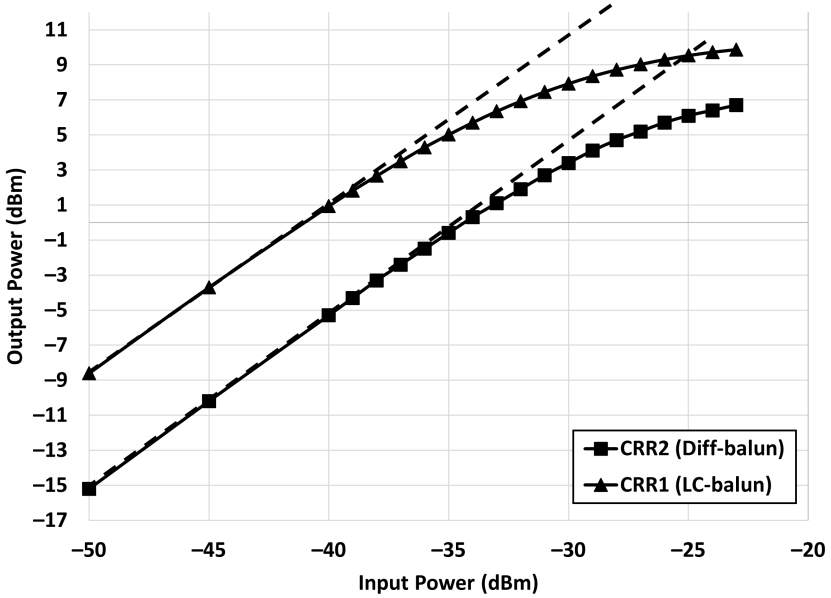

Figure 13. The measured output signal power of CRR1 and CRR2 versus a single-tone input power sweep.

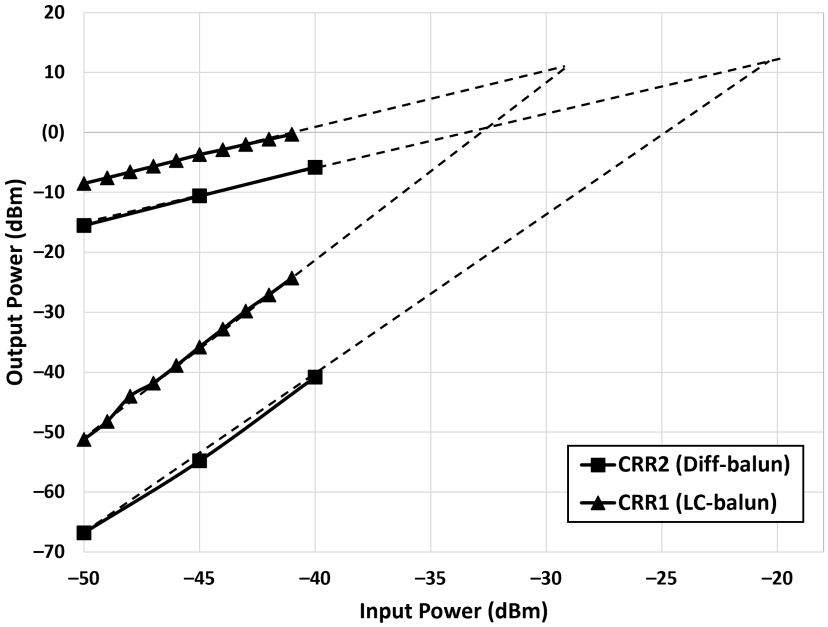

Figure 14. The measured third-order intercept points of CRR1 and CRR2 versus a two-tone input power sweep.

The presented architecture shows that it can provide good performance metrics regardless of the input network selected for impedance matching. An LC balun input matching strategy (CRR1) shows that a more uniform gain and NF can be obtained at the cost of added inductor die area. CRR2 exhibits more conversion gain and NF variations over its operating frequency range, and it has a lower frequency of operation, but it requires significantly reduced active areas (the lowest reported in the table), which can be an advantage in some applications.

Table 1. Performance summary and comparison to other works.

Parameters	This Work CRR2 (Diff. Balun)	This Work CRR1 (LC Balun)	TMTT 2020 [4]	JSSC 2014 [8]	Elec. 2020 [12]	MWCL 2019 [13]	JSSC 2017 [21]	IEEE 2021 [22]	JSSC 2021 [3]	JSSC 2018 [6]	TMTT 2019 [5]
Application	IoT	L-band	IoT	ZigBee	ZigBee	IoT	Bluetooth	BLE	IoT	ZigBee	BLE
Process node	130 nm CMOS	130 nm CMOS	65 nm CMOS	65 nm CMOS	130 nm CMOS	65 nm CMOS	28 nm CMOS	65 nm CMOS	28 nm CMOS	65 nm CMOS	130 nm CMOS
Freq. (GHz)	0.2–1	1–1.7	2.4–2.4	2.4	2.4	0.91	2.4	2.4–2.48	1.8–2.8	2.4	2.4
Bandwidth (MHz)	110	90	2	2	2	20	1.5	2	2	2	2
S11 (dB	<-10	<-10	<-10	<-10	<-10	<-10	<-10	<-10	<-10	<-10	<-10
Gain (dB)	33–39.5	41.5	49.5	57	45	40.7	43.4	42	45	57.8	42
NF (dB)	6–10.5	6.5	8.2	8.5	3.5	1.94	7.8	13.2	6	15.7	7.2
IIP3 (dBm)	−21.5 *	−28.2 *	−25.75 *	$-6^{\dagger}$	N/A	−25.6 *	−20 *	−25 *	−13 *	−18.5 *	−17 *
P_{DC}@VDD (mW)	2@1.2	2@1.2	2.16@1.2	1@1.2	2.9@1	3.6@1.8	4.3@1.8	1.13@0.8	0.38@0.8	1.78@1	1.7@1.2
Active Area (mm^2)	0.025	0.54	1.16	0.3	0.7	0.559	0.4	0.85	0.2	0.45	0.7

* In-band IIP3, † Out-of-band IIP3.

4. Conclusions

A low-power and wideband RF-to-BB current-reuse receiver front-end was fabricated in TSMC 130 nm CMOS technology. The current sharing of the TIA and LNTA reduces the power consumption significantly. Moreover, a CCCG LNTA topology boosts the transconductance without consuming extra power. An AI and $1/f$ NC technique enhances the receiver NF performance and RF bandwidth. The performance of the receiver front-end is verified with both an input differential balun without an on-chip inductor and an input LC balun with an on-chip inductor to demonstrate the robustness of the architecture. In fact, the receiver may be tuned for different RF bands by changing the components of the matching network. The results show the receiver covers an RF band from 0.2 to 1 GHz and from 1 to 1.7 GHz with a differential balun and LC balun, respectively. This work shows that the proposed CRR is well-suited for different matching circuits over a wide RF range.

Author Contributions: Conceptualization, A.A. and F.N.; methodology, A.A.; software, A.A.; validation, A.A.; formal analysis, A.A.; investigation, A.A.; resources, A.A.; data curation, A.A.; writing—original draft preparation, A.A.; writing—review and editing, A.A. and F.N.; visualization, A.A.; supervision, A.A. and F.N.; project administration, A.A.; funding acquisition, F.N. All authors have read and agreed to the published version of the manuscript.

Funding: This research received funding from the Natural Sciences and Engineering Research Council of Canada.

Acknowledgments: The author would like to thank CMC Microsystems for enabling chip fabrication and providing access to the EDA tools. Moreover, the authors thank Sequans Communications and its supportive team in both hardware platform and RFIC departments for providing laboratory equipment and technical support during the measurements.

Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

P1dB	1 dB compression point
AI	Active inductor
BB	Baseband
CG	Common gate
CCCG	Cross-coupled common gate
CMOS	Complementary metal-oxide semiconductor
CML	Current mode logic
CS	Common source
CRR	Current-reuse Receiver
CS	Common source
DSB	Double sideband
ÉTS	École de technologie supérieure
IF	Intermediate frequency
IIP3	Third-order intercept point
IoT	Internet of Things
LNA	Low-noise amplifier
LNTA	Low-noise transconductance amplifier
LO	Local oscillator
NF	Noise figure
NC	Noise cancellation
DSB	Double sideband
PCB	Printed circuit board
RF	Radio frequency
TIA	Transimpedance amplifier
VCO	Voltage-controlled sscillator
VNA	vector network analyzer
V_{TH}	Voltage threshold

Appendix A. AI Input Impedance Derivation

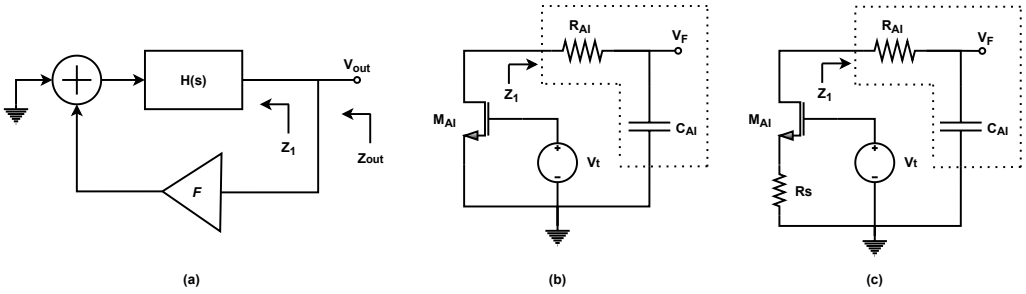

Figure A1. (**a**) Output impedance of a negative-feedback system. The open-loop circuit of (**b**) Figure 3a and (**c**) Figure 3b.

The block diagram of a negative-feedback system when calculating the output impedance is shown in Figure A1a. The feedback network, F, reduces the output impedance of Z_1 such that the following is the case.

$$Z_{out}(s) = \frac{Z_1}{1 + FH(s)}. \tag{A1}$$

Hence, Z_{out} increases if $KH(s)$ reduces. This means $KH(s)$ with a low pass transfer function results an inductive output impedance.

The open-loop circuit of Figure 3a can be modeled as Figure A1b. $H(s)$ is realized by a first-order low-pass $R_{AI}C_{AI}$ filter and F by transistor M_{AI}. The impedance looking into the $R_{AI}C_{AI}$ filter, Z_1, is given by the following.

$$Z_1(s) = R_{AI} + \frac{1}{C_{AI}s}. \tag{A2}$$

Moreover, the loop-gain is calculated by the following.

$$FH(s) = -\frac{V_F}{V_t} = \frac{g_m}{C_{AI}s}. \tag{A3}$$

Finally, referring to (A1), the output impedance, Z_{out}, is given by the following.

$$Z_{out}(s) \cong \frac{\frac{R_{AI}C_{AI}s+1}{C_{AI}s}}{1+\frac{g_m}{C_{AI}s}} = \frac{R_{AI}C_{AI}s+1}{C_{AI}s+g_m}. \tag{A4}$$

Accordingly, the inductive behavior of the active-inductor circuit is thus demonstrated, where at low frequencues, the output impedance is $1/g_m$ and it increases with frequency to R_{AI} if $R_{AI} >> 1/g_m$.

Now, we add the source-degeneration resistor, R_s, to transistor M_{AI}, which is shown in Figure A1c. The loop-gain is then calculated by the following.

$$FH(s) = -\frac{V_F}{V_t} = \frac{g_m\frac{1}{C_{AI}s}}{1+g_mR_s}. \tag{A5}$$

Again, from (A1), the closed loop output impedance is calculated such that the following is the case.

$$Z_{out(withR_S)}(s) \cong \frac{g_{m,AI}R_S(R_{AI}C_{AI}s+1)+R_{AI}C_{AI}s}{g_{m,AI}R_SC_{AI}s+g_{m,AI}+C_{AI}s}. \tag{A6}$$

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