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RESEARCH ARTICLE

A Comprehensive Approach to Flexible LVRT Strategies for Inverter-Based PPMs Enhancing Voltage-Support, Overcurrent Protection, and DC-Link Voltage Quality

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ABSTRACT This paper focuses on enhancing the resilience of Power Park Modules (PPMs), connected to the grid via power electronic units, under asymmetrical voltage sag conditions. We particularly address three interconnected constraints crucial for Low-Voltage Ride-Through (LVRT) capability of PPMs: grid voltage support, overcurrent protection, and the DC-link voltage quality. Existing literature often overlooks the holistic consideration of these factors, prompting this study to introduce and compare three flexible LVRT strategies compliant with recent German grid codes. The proposed strategies use distinct approaches to reinforce the LVRT capability of the PPMs. Strategy A employs static gain factors to control positive- and negative-sequence reactive current (PSRC and NSRC) and the negative sequence of the active current (NSAC). Strategy B aims to enhance the DC-link voltage quality by eliminating real power oscillations through the flexible choice of NSAC and gain factors controlling PSRC and NSRC. Strategy C enhances DC-bus voltage quality by eliminating NSAC and employing flexible equal gain factors for PSRC and NSRC, mitigating both real and imaginary power oscillations. Testing on an inverter-based PPM, involving 400 kW PV module and 200 A, storage system, reveals the superior performance of strategy C. Additional tests evaluate Strategy C's performance with var/voltage regulation equipment (On-Load-Tap-Changing transformer), demonstrating stable and promising performance. Through the introduced approaches, the authors believe that this research work is useful for developing future grid codes and improving the safety and reliability of grid-connected power systems.

INDEX TERMS Asymmetrical voltage sag, current limitation, DC-link voltage, fast fault current injection (FFCI), grid codes, low-voltage-ride-through (LVRT), renewable energy source (RES), RfG NC, power park module (PPM), power systems, voltage support.

NOMENCLATURE

ACRONYMS

RES	Renewable Energy Source.
VSI	Voltage Source Inverter.
ESS	Energy Storage System.
PCC	Point of Common Coupling.
RfG NC	Requirements for Generators Network Code.
PGS	Power Generating System.
PPM	Power Park Module.

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SPGM	Synchronous Power Generating Module.
OPPM	Offshore Power Park Module.
LVRT	Low-Voltage-Ride-Through.
FFCI	Fast Fault Current Injection.
PSAC	Positive-Sequence Active Current.
NSAC	Negative-Sequence Active Current.
PSRC	Positive-Sequence Reactive Current.
NSRC	Negative-Sequence Reactive Current.
RPO	Real Power Oscillations.
IPO	Imaginary Power Oscillations.
VSS	Voltage-Support Strategy.
FOPS	Flexible Oscillating-Power Strategy.
VUF	Voltage Unbalance Factor.
MPPT	Maximum Power Point Tracking.
MRF-PLL	Multiple Reference Frame Phase-Locked Loop.
OLTC	On-Load-Tap-Changing.

VARIABLES AND PARAMETERS

$\boldsymbol{v}$	Voltage vector across the connection point i.e., secondary terminals of transformerT_1.
$\boldsymbol{i}$	Three-phase injected current vector.
$\boldsymbol{e}^+, \boldsymbol{e}^-$	Positive- and negative-sequence grid voltage vectors across the secondary terminals of transformer T_2.
$\boldsymbol{u_i}$	Voltage vector across the inverter's terminals.
$\boldsymbol{i_p^+}, \boldsymbol{i_p^-}$	Positive- and negative-sequence active current vectors.
$\boldsymbol{i_q^+}, \boldsymbol{i_q^-}$	Positive- and negative-sequence reactive current vectors.
v, i	Instantaneous voltage and current.
V, I	Voltage and current amplitudes.
$\Delta I_q^+, \Delta I_q^-$	Required increments of positive- and negative-sequence reactive current.
k^+, k^-	Gain factors of the positive- and negative-sequence reactive current.
k_p	Gain factor applied to control the NSAC.
E^+, E^-	Amplitudes of $\boldsymbol{e}^+$and $\boldsymbol{e}^-$.
R_g, L_g	Equivalent grid resistance and inductance.
v_{dc}	Voltage across the DC-bus.
C_{dc}	DC-bus capacitance.
P, Q	Active and reactive powers.
p,q	Instantaneous real and imaginary powers.
ω	Grid velocity.
θ^+, θ^-	Instantaneous phase-angles of positive- and negative-sequence grid voltage.
θ	Phase-shift between the positive and negative sequences of the grid voltage.
δ	Phase-angle of the vector equivalent to $(\boldsymbol{v}^+ + \boldsymbol{v}^-)$.
R_s, R_{sh}	Series and shunt resistances in the single-diode model of a PV cell.
I_{ph}	Photocurrent through a PV cell.
I_s	Diode saturation-current.
A_{bat}	Nominal capacity of the battery.
$\mathrm{Ch_{bat}}$	Batter's extracted charge.
P_{min}	Minimum charging power of the battery.
i_L	Current through an inductor of a DC-DC converter.
E_{oc}	Battery's open-circuit voltage at full charge
C, L	Capacitor and Inductor of a DC-DC converter.
d	Duty-cycle of a DC-DC converter's gate-signal.

SUPERSCRIPTS

+, -, 0	Positive, negative, and zero sequences.
ref	Reference signal.

SUBSCRIPTS

a, b, c	Variables expressed in the abc reference frame.
n	Nominal amplitude.
0	Pre-fault amplitude.
$\perp$	Orthogonal (voltage).
max	Maximum amplitude.
p, q	Active and reactive (current).
$\sim$	Oscillating term.
c, s	Cosine and sine oscillating terms.
dc	Signal defined across the DC-bus.
D, Q	Direct and Quadrature components.
pv	Related to photovoltaic control system.
cell	Related to a PV cell.
bat	Related to the storage system.

I. INTRODUCTION

Global warming continues to bring about remarkable changes in weather patterns from one year to the next. It is unequivocal that the major source of this warming is the emission of gases produced from the extensive utilization of fossil fuels [1]. According to the road map, recently issued by the International Energy Agency (IEA), the energy sector is responsible for about 50% of total gas emissions worldwide [1]. Hence, there is a compelling need for a rapid energy transition plan that necessitates a shift from fossil-fuel-dependent energy production to clean and sustainable alternatives. According to projections by the International Renewable Energy Agency (IRENA), the share of Renewable Energy Sources (RESs) in the global primary energy supply is expected to surge from 15% in 2015 to a remarkable 75% by the year 2050 [2]. The global energy transition program has set a target of achieving carbon dioxide (CO_2) emissions neutrality in the energy sector by the second half of this century, specifically by 2050 [1]. This ambitious objective has garnered support from various countries. For example, major CO_2-producing countries such as China (30%), the USA (15%), the European Union (EU) (10%), and India (7%) in 2019, have drawn up long-term strategies with more stringent emission reduction goals [3]. The EU, for instance, has outlined plans to curtail energy-related greenhouse gas emissions by 40 to 60% by the year 2030, ultimately reaching net-zero emissions by

2050. To realize these aspirations, the EU intends to boost its reliance on RESs by approximately 40% by 2030 [3].

RESs hold a pivotal role in both isolated and grid-connected applications. In remote or off-grid regions, they stand as the primary generators of electricity. In grid-connected scenarios, their integration objectives revolve around enhancing the flexibility and reliability of the grid by optimizing production and demand management. Nevertheless, the synergy between RESs and the grid encounters substantial challenges, particularly when confronted with fault conditions. Moreover, the grid is perpetually susceptible to disturbances and faults, with short circuits representing the most severe grid faults, leading to voltage sags [4], [5]. These circumstances have the potential to impact grid stability and power quality [6], [7], [8]. Consequently, they affect the performance of connected equipment, notably power inverters, which play a crucial role in managing power flow between RESs and the grid. Conversely, the quality of the power injected into the grid from RESs can also perturb the grid, especially with high RES's penetration.

A grid voltage sag becomes evident when there is a drop in the voltage magnitude observed by the inverter at the Point of Common Coupling (PCC). This decrease can occur uniformly across all three phases, resulting in a symmetrical voltage sag, or it can be uneven across the phases, leading to an asymmetrical, namely unbalanced, three-phase voltage sag. It is important to highlight that asymmetrical voltage sags are the most frequently encountered scenarios. Furthermore, they cause a grid voltage imbalance giving rise to low-frequency ripple in the real and imaginary powers. The ripple in the real power also referred to as Real power Oscillations (RPO) can impact the DC-bus voltage, potentially leading to instability and the disconnection of the inverter. As for the Imaginary power Oscillations (IPO), they can induce unwanted fluctuations in the grid voltage amplitude. Apart from voltage sags, short-circuit faults can also generate transient overcurrent that may surpass the maximum threshold supported by semiconductor devices, ultimately resulting in inverter failure [5]. Moreover, if the voltage at the point of connection is not promptly restored, protective under-voltage breakers will be enabled to disconnect the inverter from the grid [9]. Initially, the early grid codes, formulated by transmission-system operators for grid-connected sources, restricted Power Generation Systems (PGSs) from varying reactive power and often denied interconnection in numerous scenarios [10]. However, as the penetration of RESs has risen significantly, grid disconnections might lead to a critical reduction in active-power supply from RESs, triggering grid instability concerns. Modern grid codes have thus introduced stringent technical regulations for grid-connected PGSs under grid voltage sag conditions, often referred to as Fault-Ride-Through (FRT) requirements, with a specific focus on Low-Voltage-Ride-Through (LVRT) capability.

Under these regulations, inverters are required to maintain their connection to the grid during specific fault scenarios and contribute to the rapid restoration of the grid voltage. Initially, these grid codes primarily required the injection of the Positive-Sequence Reactive Current (PSRC) to support the positive-sequence grid voltage [11]. However, this strategy did not address the elimination of negative sequence components and, in some cases, could lead to overvoltage in non-faulty phases. Subsequent versions of the codes now require the injection of both positive and negative sequences of reactive current [12], [13], [14], [15], [16], [17]. The inclusion of the negative sequence aims to help decrease the amplitude of negative-sequence grid voltage.

These codes have also permitted curtailment of active power to prioritize reactive power. In addition, they have established limits on the amplitudes of reactive current sequences to ensure they do not surpass the maximum current supported by the inverter. It is, however, worth noting that the transmission system operators have not yet established specific requirements for active current components.

In recent years, researchers have been actively engaged in the refinement of the control strategies to enhance the performance of grid-connected PGSs when confronted with voltage sag conditions. This enhancement primarily involves the injection of active and reactive currents, encompassing both positive and negative sequences. In this regard, various flexible control strategies have been proposed for grid-connected inverters operating under different voltage sag scenarios [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28]. Hamouda et al. introduce a unity power factor control strategy aimed at supporting the grid voltage through the injection of reactive current, albeit the injection of a negative sequence is not addressed [18]. Wang et.al. propose a Flexible Oscillating-Power Strategy (FOPS), enabling the flexible control of both real and imaginary powers' oscillations [19]. However, this approach overlooks the crucial concept of voltage support, which is a vital criterion. Moreover, it does not consider the current limitation constraints. In [20], the proposed study introduces a current limitation algorithm tailored to Austria's national grid codes, requiring the injection of positive- and negative-sequence reactive current to support the grid voltage. Although this algorithm is assessed using a realistic simulation model, it uses an ideal DC-bus voltage. In addition, it only focuses on the current limitation during dynamic voltage support and omits the remaining LVRT requirements. Çelik et.al. develop a control strategy geared toward maximizing power delivery from a grid-connected distributed generation system during grid voltage sag situations [21]. The authors also propose a sequence extractor to swiftly extract symmetrical components. The primary objective of this strategy is the optimization of a FOPS to achieve a versatile control of both real and imaginary powers oscillations. However, they omit considerations related to reactive power injection and voltage support capability.

Several research works address the analysis and control of the DC-link voltage and harmonic reduction. In [22], the authors propose a control scheme for

reference-current-generator-based power control, effectively eliminating oscillations on both DC and AC sides. The approach, featuring closed-loop control for active power, stands out by successfully suppressing DC-link voltage oscillations, reducing the need for a large DC-side capacitor, and enhancing the overall stability and safety of grid-connected primary energy resources compared to existing strategies. In [23], Çelik introduces a Lyapunov-based control algorithm for three-phase shunt active power filters, enhancing harmonic compensation in Electrical Vehicle (EV) applications and on the grid. The proposed approach effectively mitigates harmonics under diverse nonlinear loads and grid disturbances, offering several improvements such as THD compliance, Lyapunov-estimator-based signal extraction, dynamic performance optimization, and filter elimination. In [24], the authors propose a sliding-mode-based adaptive-linear-neuron proportional-resonant (ADALINE-PR) control method for Vienna rectifier used as battery charger in EV. The approach ensures robust DC-link voltage regulation, real-time adaptation of source current errors, and simplified derivation of reference current signals, resulting in superior dynamic and steady-state performance with reduced harmonics and ripples compared to existing studies. Note that all strategies, discussed in this paragraph, omit the voltage-support concept.

In the quest to enhance the voltage-support capability of inverter-based energy sources, several Voltage Support Strategies (VSSs) have been proposed in the literature. In [25] Camacho et.al. introduce a suite of control strategies, each tailored to specific voltage-support objectives while considering overcurrent protection. These strategies primarily aim to maximize the positive-sequence voltage, minimize the negative-sequence voltage, and reduce the voltage imbalance. When armed with an accurate grid parameter estimation, these strategies have the potential to optimize the voltage-support capability. However, they do not delve into the consequences of generated power oscillations and their effect on the DC-link voltage. In [26], the authors develop a control strategy with the goal of maximizing voltage support capability, constraining injected current, and eliminating RPO. However, this work omits the evaluation of the DC-link voltage quality. In [27], the proposed strategy generates current references aimed at optimizing the inverter's voltage support capability while considering grid parameters and overcurrent protection. This approach also provides flexibility in prioritizing active or reactive power injection. However, authors do not explore the impact of the generated currents on power oscillations. In [28], the authors put forth a multi-objective control strategy aimed at maximizing the positive-sequence voltage while imposing current limitation. This work investigates the influence of RPO on the DC-bus voltage performance and addresses RPO control. However, it does not address the minimization of negative-sequence voltage or the control of IPO. Note that the aforementioned optimized VSSs rely on grid parameters (resistance and conductance), implying their need for accurate real-time estimators. Moreover, the potential effects of these proposed strategies on the DC-bus voltage quality remain unexplored.

Numerous research studies have undertaken a comprehensive review of existing control strategies in the context of unbalanced voltage sag conditions. In [29], the authors conduct a comparative analysis of FOPSs and VSSs across various grid profiles. They also introduce a current limitation technique designed to shield the inverter from overcurrent issues. The performance of these reviewed strategies is evaluated based on their ability to mitigate power oscillations and enhance the voltage support capability. The findings indicate that both FOPSs and VSSs exhibit the potential to support the grid during voltage sag conditions, even though this aspect has not been thoroughly explored in the literature regarding FOPSs. Additionally, it is observed that VSSs can optimize the voltage support performance. However, these strategies have not addressed the power oscillations' impact on the performance of the DC-link voltage.

In [30], Silva et.al. conduct a review of power control strategies applicable to inverter-based wind energy systems connected to the grid under voltage sag conditions. The authors present detailed expressions describing the resulting power oscillations and the behavior of the DC-bus voltage. Results underscore the significance of limiting RPO. However, the evaluation of voltage support capabilities for the reviewed strategies is not addressed. In [31], the authors explore power control strategies specifically for PV systems operating under unbalanced voltage sag conditions. They compare three primary strategies in terms of dynamic response and the ripple in DC-link voltage. Furthermore, they assess the performance of these strategies on the PV side, considering aspects such as Maximum Power Point Tracking (MPPT) efficiency and thermal stress in the capacitors of the DC-bus and PV array. The results show that the strategy based on the control of RPO provides the best quality of the DC-bus voltage. A comparative review of the LVRT performance of PV systems to overcome related challenges is also detailed in [32]. It demonstrates that each strategy can partially meet LVRT requirements and highlights the complexity of achieving this objective without addressing all pertinent challenges.

Overall, previous research papers that focus on optimizing voltage support tend to treat the DC-bus as an ideal and stable voltage source. Conversely, studies concentrating on the robustness of the DC-bus often overlook aspects related to LVRT and voltage support performance.

In light of the above, this paper introduces three LVRT strategies designed for grid-connected inverters operating under asymmetrical voltage sags conditions. These strategies combine the advantages of both FOPSs and VSSs to address all essential conditions required for LVRT compliance. More importantly, the proposed strategies differ from conventional literature approaches that rely on power references. Instead, they directly generate current's references by conforming to the Fast Fault Current Injection (FFCI) requirements specified by grid codes. Additionally, these references depend on the maximum current capacity of the inverter fed from various

DC sources typically associated with RESs and Energy Storage Systems (ESSs).

The main novelty of this work is the design of flexible LVRT control strategies addressing simultaneously the three LVRT-related issues: the voltage-support capability, the protection of the inverter against overcurrent, and the DC-link voltage quality. The proposed strategies rely on different formulations of the appropriate current references considering the grid codes requirements and the flexible mitigation of real and imaginary powers oscillations. To the best of our knowledge, the voltage-support capability of the converter along with enhancing the DC-link voltage quality and limiting the overcurrent is first addressed in this paper.

The paper is organized as follows: Section II discusses the contemporary European grid codes relevant to inverter-based Power Park Modules (PPMs) facing voltage sag scenarios. In Section III, we delve into the essential prerequisites for meeting LVRT criteria. Section IV explains in detail the proposed flexible control strategies. Section V describes the power system elements, used to test the proposed strategies, and the associated control architectures. The outcomes stemming from distinct case studies are presented and analyzed in Section VI. Finally, Section VII encapsulates the concluding remarks and findings of this paper.

II. BRIEF REVIEW OF RECENT GRID CODES UNDER VOLTAGE SAG CONDITION

The European standard EN 50160 characterizes a voltage sag as a situation where the RMS voltage at the PCC falls below 90% of its nominal value for a duration ranging from 10 milliseconds to 1 minute. The voltage sag is considered resolved once all three phases have recovered, meaning their amplitudes return to the dip-end threshold of 0.9 p.u. [33]. Most critical voltage sags are due to symmetrical or asymmetrical short circuits occurring in the Medium Voltage (MV) grid or larger. The severity of the voltage sag at the PCC basically depends on the grid impedance, the fault type, and the transformer's connection.

In 2016, the European Commission introduced Regulation (EU 2016/631), which outlined grid connection requirements known as the Requirements for Generators Network Code (RfG NC) [16]. These requirements consider various factors under voltage sag conditions, including the type of voltage sag (symmetrical or asymmetrical), the voltage level at the PCC, and the category of the PGS. PGSs are classified into three main types: Synchronous Power Generating Modules (SPGMs), Power Park Modules (PPMs) and Offshore Power Park Modules (OPPMs). SPGMs are generators that are synchronously connected to the grid. PPMs encompass asynchronously connected generators and power electronic interfaced units, such as PV plants and EVs [17]. OPPMs are PPMs with an offshore connection point. Moreover, each PGS type is in turn subdivided into four distinct categories depending on its capacity power limits and the voltage level at the PCC as reported in Table 1 [16], [17], [35], [36], [37], [38], [39], [40], [41], [42], [43], [44], [45], [46], [47], [48], [49].

TABLE 1. Classification of PGSs upon the capacity power limits according to RfG NC.

PGS category	Capacity power limits	Connection voltage
A	0.8 MW to 1 MW	LV/MV under 110 kV
B	1 MW to 50 MW	MV under 110 kV
C	50 MW to 75 MW	MV/HV under 110 kV
D	above 75 MW	HV above 110 kV

The RfG NC has established common requirements for fault and post-fault operation, focusing on two key aspects: LVRT capability and FFCI. LVRT capability entails that PGS must remain connected to the grid during and after fault clearance for a specified duration, which depends on the depth of the voltage sag. Regarding FFCI, PGSs are required to inject the appropriate reactive current to support the grid [16], [17], [36], [37]. However, this requirement is only imposed to PGSs connected to the MV grid or larger. It is worth mentioning that the RfG NC sets out general requirements for grid-connected PGSs, and individual EU countries are responsible for establishing their own grid codes while ensuring compliance with the RfG NC.

Given the focus of this paper on power-electronic-interfaced units, the following section provides a detailed overview of the LVRT and FFCI requirements specifically applicable to PPMs.

A. LVRT REQUIREMENTS FOR PPMs

The concept of LVRT outlines the specific conditions under which PPMs must maintain their connection to the grid during and after a fault event. The requirements governing LVRT are defined by the RfG NC and are represented graphically by the voltage-against-time curve depicted in FIGURE 1. In accordance with the RfG NC guidelines, the PPM is strictly prohibited from disconnecting from the grid if the voltage profile remains above the curve illustrated in FIGURE 1 [16]. More precisely, the profile of FIGURE 1 is divided into three regions. In region 1, the PPM should never be disconnected from the grid. In zone 2, the PPM may disconnect even before the full voltage recovery. Finally, in zone 3, the PPM may remain connected or disconnect upon the decision of the transmission system operator.

The parameters introduced in FIGURE 1 have the following meanings:

- U_{ret}: This represents the voltage level across the PCC at the onset of the fault. During a fault, this voltage may decrease significantly, possibly down to 0.15 p.u. or even reach 0 p.u.
- U_{clear} is the voltage level at the PCC after the fault clearance.
- t_{clear} is the tolerated time interval before the fault clearance at the U_{clear} level. Typically, this interval ranges

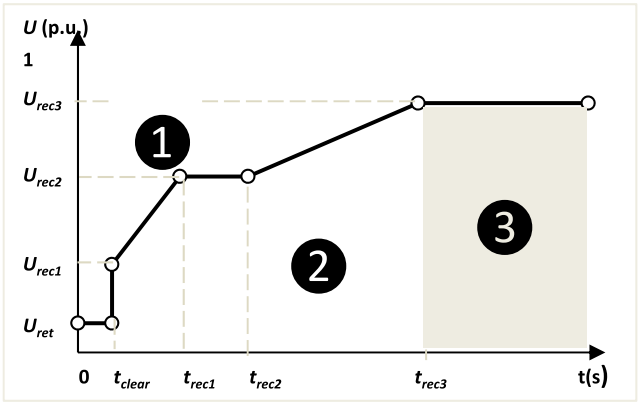

FIGURE 1. Voltage-against-time profile describing the general LVRT requirements as specified by RfG NC.

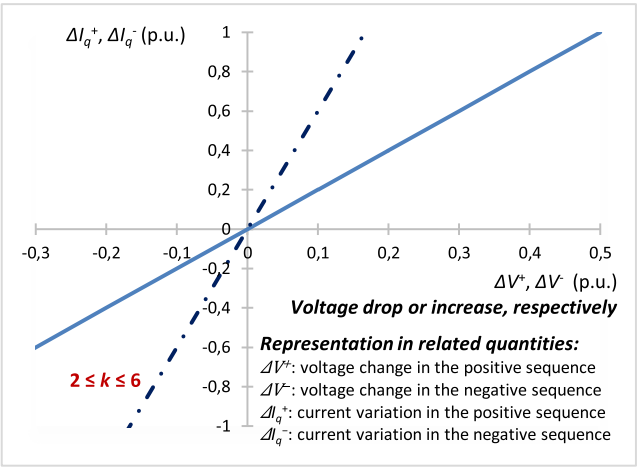

FIGURE 2. Reactive current injection requirements according to recent German and European grid codes for MV and HV grid-connected PPMs.

from 0.14 to 0.15 seconds, but in certain cases, it may be extended to 0.25 seconds if it aligns with safety and system operation requirements.

- t_{rec1}, t_{rec2}, t_{rec3}: These are specific time points in the LVRT scenario. After the fault clearance, the voltage should recover linearly from U_{clear} to an initial recovery level called U_{rec1} at time t_{rec1}. Between t_{rec1} and t_{rec2}, the voltage may stay at the level U_{rec1}. Then it should increase again from U_{rec1} to the final recovery level U_{rec2} at time t_{rec3}.

The specific limit values for these voltage levels and their corresponding times are determined by the national grid codes of individual EU countries. As an example, Table 2 provides LVRT requirements for PPMs connected to the MV grid, as defined by European standard EN5049-2 and German grid codes VDE-AR-N 4110. These features mostly cover PPMs connected to a grid below 110 kV [15], [40], [41], [42]. For PPMs connected to high voltage (HV) grids, typically above 110 kV, more stringent requirements are imposed, often tolerating U_{ret} to reach 0 p.u.

B. FAST FAULT CURRENT INJECTION REQUIREMENT

The RfG NC requires the injection of an appropriate amount of reactive current to contribute to the fast recovery of the grid voltage and avoid disconnecting the PPM from the grid. Since most grid faults are asymmetrical, the injection of a reactive current with both positive and negative sequences is required to enhance the voltage-support capability [11], [16]. Indeed, the injection of the PSRC boosts the positive sequence of the voltage, while injecting the Negative-Sequence Reactive Current (NSRC) mitigates the negative sequence of the voltage, which reduces the voltage imbalance and the sag severity.

FIGURE 2 provides the required reactive current profile as defined by German grid codes for MV and HV [40], [41]. Note that several countries have also adopted this requirement such as Spain, Luxembourg, and Austria [38], [39], [43], [47]. The required increments in the PSRC and NSRC (ΔI_q^+ and ΔI_q^-) are outlined as follows:

$$\Delta I_q^+ = I_q^+ - I_{q0}^+ = k^+ \frac{V_0 - V^+}{V_n} I_n \tag{1}$$

$$\Delta I_q^- = I_q^- - I_{q0}^- = k^- \frac{V^-}{V_n} I_n \tag{2}$$

I_{q0}^+ and I_{q0}^- are the amplitudes of the pre-fault positive- and negative-sequence reactive current, respectively. I_q^+ and I_q^- are their counterparts during the post-fault operation. I_n is the nominal amplitude of the injected current. V_0 and V_n are the pre-fault and the nominal amplitudes of the voltage across the connection point of the PPM to the grid. V^+ and V^- are the amplitudes of the post-fault positive- and negative-sequence voltage across the connection point. Additionally, k^+ and k^- represent positive and negative gain factors; their extreme values are bounded as follows:

$$2 \leq k^{\pm} \leq 6 \tag{3}$$

III. FORMULATION OF CURRENT COMPONENTS REQUIREMENTS FOR ENHANCED LVRT PERFORMANCE

Consider the power system configuration depicted in FIGURE 3, which illustrates a typical structure of a PPM. This system consists of a PV connected to an ESS through a common DC-bus [51], [53]. The active power flow is performed from the DC-bus to an AC LV-bus via a VSI. The LV-bus is thereafter connected to the PCC through a step-up transformer T_1. The PCC is, in turn, connected to an IEEE-9-bus via a second step-up transformer T_2 and a transmission line. The occurrence of a short circuit fault in the transmission line gives rise to the following three critical issues:

- A voltage sag occurring at the PCC, which could potentially trigger the under-voltage protection system, leading to the disconnection of the VSI. In situations involving high power generation, this event might even

TABLE 2. LVRT Characteristics for MV connected PPMs.

	Grid code (MV)	U_{ret} (p.u.)	U_{clear} (p.u.)	U_{rec1} (p.u.)	U_{rec2} (p.u.)	t_{clear} (s)	t_{rec1} (s)	t_{rec2} (s)	t_{rec3} (s)
Symmetrical fault	EN 50549-2 [37]	0.05 to 0.15	U_{ret} to 0.15	U_{clear}	0.85	0.14 to 0.25	t_{clear}	t_{rec1}	1.5 to 3
	VDE-AR-N 4110:2018-11 [40]	0.15	0.15	0.15	0.85	0.15	0.15	0.15	3
Asymmetrical fault	EN 50549-2 (MV) [37]	0.05	0.05	0.05	0.85	0.14 to 0.25	t_{clear}	t_{clear}	2 to 3
	VDE-AR-N 4110:2018-11 [40]	0.15	0.15 to 0.75	0.75	0.85	0.22	0.22 to 3	3	5

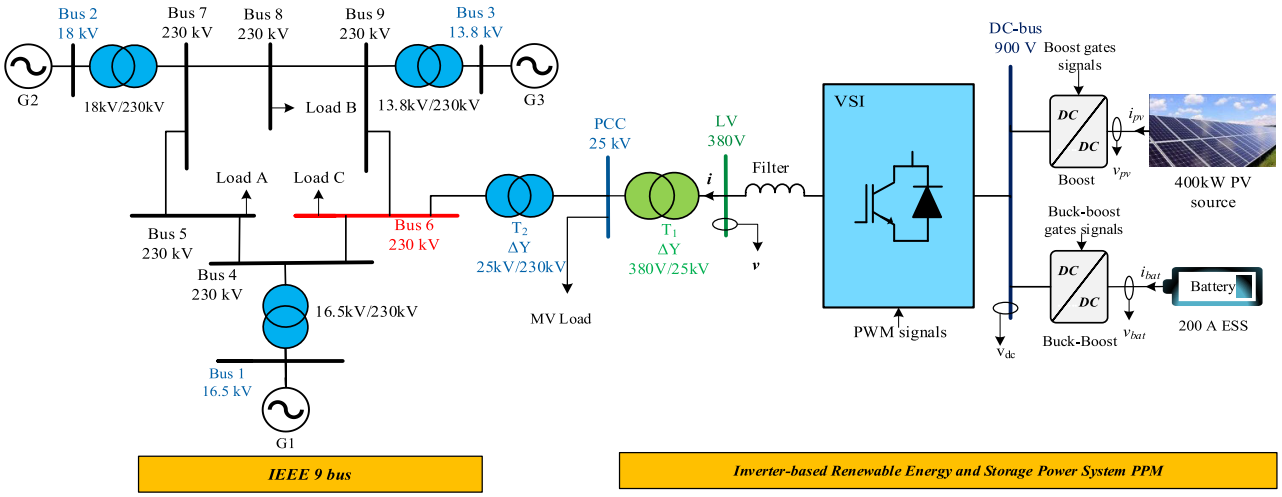

FIGURE 3. Inverter-Based PPM Connected to IEEE-9-bus.

induce a grid collapse due to an abrupt decrease of the available power.

- Important transient currents are provided and lead to excessive heating of the power components within the VSI and, in severe cases, potentially resulting in VSI failure.
- In case of asymmetrical grid voltage sags, significant oscillations are created in the instantaneous real and imaginary powers. The RPO subsequently generate undesired ripple in the DC-bus voltage and have the potential to destabilize the VSI. Additionally, IPO lead to undesirable fluctuations in the voltage amplitude across the connection point of the PPM, which may, in turn, propagate back and worsen the DC-bus voltage.

To adhere to the grid code requirements and prevent disconnection from the grid, it is imperative to address the following three constraints:

(1) Prioritizing grid voltage support to swiftly attain the recovery threshold voltage (0.9 V_n) and avert grid instability.
(2) Implementing current limitation measures to protect the inverter's semiconductors against overcurrent.
(3) Ensuring the quality of the DC-link voltage to strengthen the DC-bus stability.

This paper puts a particular emphasis on the constraint related to DC-bus voltage quality. In many previous research attempts, this aspect was often overlooked for the sake of simplicity, with the DC-bus being treated as an ideal voltage source, which does not accurately reflect real operational scenarios [25], [26], [27]. To properly address this problem with several constraints, the symmetrical components method is used [19], [55]. This technique decomposes the unbalanced voltage across the connection point of the PPM and the injected currents into three balanced sequences: positive sequence ($\boldsymbol{v}^+$ and $\boldsymbol{i}^+$), negative sequence ($\boldsymbol{v}^-$ and $\boldsymbol{i}^-$), and zero sequence ($\boldsymbol{v}^{\boldsymbol{0}}$ and $\boldsymbol{i}^{\boldsymbol{0}}$).

$$\boldsymbol{v} = \boldsymbol{v}^+ + \boldsymbol{v}^- + \boldsymbol{v}^{\boldsymbol{0}} \tag{4}$$

$$\boldsymbol{i} = \boldsymbol{i}^+ + \boldsymbol{i}^- + \boldsymbol{i}^{\boldsymbol{0}} \tag{5}$$

Note that in the case of a three-wire system, if the fault occurs upstream of the transformer T_2, i.e., in the transmission line, the zero sequence of the voltage at the PCC is inherently removed by T_2. On the other hand, the positive and negative sequences of the line current can be decomposed into two orthogonal and decoupled quantities namely active and reactive currents as depicted in FIGURE 4. Considering this, the active current is responsible for the active power, while

the reactive power is related to the reactive current.

$$\boldsymbol{i}^+ = \boldsymbol{i}_p^+ + \boldsymbol{i}_q^+ \qquad I^+ = \sqrt{I_p^{+^2} + I_q^{+^2}} \tag{6}$$

$$\boldsymbol{i}^- = \boldsymbol{i}_p^- + \boldsymbol{i}_q^- \qquad I^- = \sqrt{I_p^{-^2} + I_q^{-^2}} \tag{7}$$

$\boldsymbol{i}_p^+$ and $\boldsymbol{i}_p^-$ are the positive- and negative-sequence active current aligned with $\boldsymbol{v}^+$ and $\boldsymbol{v}^-$, respectively. $\boldsymbol{i}_q^+$ and $\boldsymbol{i}_q^-$ are the positive- and negative-sequence reactive currents aligned with the orthogonal positive- and negative-sequence voltage across the connection point namely $\boldsymbol{v}_\perp^+$ and $\boldsymbol{v}_\perp^-$, respectively. I_p^+, I_q^+, I_p^-, and I_q^- are the amplitudes of $\boldsymbol{i}_p^+$, $\boldsymbol{i}_q^+$, $\boldsymbol{i}_p^-$, and $\boldsymbol{i}_q^-$, respectively. I^+ and I^- are the amplitudes of the positive- and negative-sequence grid current, respectively. Consequently, it is essential to accurately determine the four sequences of the line currents (I_p^+, I_q^+, I_p^-, and I_q^-) to achieve the LVRT capability. This needs a simultaneous consideration of constraints related to the voltage support performance, overcurrent mitigation, and the robustness of the DC-link voltage.

A. OPTIMIZED SUPPORT OF THE GRID VOLTAGE

The expressions of the positive- and negative-sequence voltage across the connection point of the PPM are given as follows:

$$\boldsymbol{v}^+ = \boldsymbol{e}^+ + R_g \boldsymbol{i}_p^+ + L_g \frac{d\boldsymbol{i}_q^+}{dt} \tag{8}$$

$$\boldsymbol{v}^- = \boldsymbol{e}^- + R_g \boldsymbol{i}_p^- + L_g \frac{d\boldsymbol{i}_q^-}{dt} \tag{9}$$

Here $\boldsymbol{e}^+$ and $\boldsymbol{e}^-$ are the positive- and negative-sequence grid voltage across the secondary terminal of transformer T_2, respectively. R_g and L_g denote the equivalent resistance and inductance of the grid seen from the point of connection i.e., the secondary side of transformer T_1.

The voltage at the point of connection is clearly influenced by the transmission line impedance and the injected currents. The ideal voltage support scenario is performed by increasing the magnitude of $\boldsymbol{v}^+$ to the nominal grid voltage amplitude and decreasing the amplitude of $\boldsymbol{v}^-$ to zero. In view of this, the phase-angle between $\boldsymbol{i}_p^+$ and $\boldsymbol{v}^+$ should be set to zero. The same conditions can be applied to $\boldsymbol{i}_q^+$ and $\boldsymbol{v}_\perp^+$. As the derivative term ($d\boldsymbol{i}_q^- \big/ dt$) is negative, $\boldsymbol{i}_q^-$ and $\boldsymbol{v}_\perp^-$ should also be in phase. In contrast, $\boldsymbol{i}_p^-$ and $\boldsymbol{v}^-$ should have opposite directions to produce a negative product term that decreases the amplitude of $\boldsymbol{v}^-$. The previously discussed conditions can be expressed analytically using the mathematical formulation given in (10), where V^+ and V^- represent the amplitudes of $\boldsymbol{v}^+$ and $\boldsymbol{v}^-$, respectively.

$$\begin{bmatrix} \boldsymbol{i}_p^+ \\ \boldsymbol{i}_p^- \\ \boldsymbol{i}_q^+ \\ \boldsymbol{i}_q^- \end{bmatrix} = \begin{bmatrix} \frac{I_p^+}{V^+} & 0 & 0 & 0 \\ 0 & \frac{-I_p^-}{V^-} & 0 & 0 \\ 0 & 0 & \frac{I_q^+}{V^+} & 0 \\ 0 & 0 & 0 & \frac{I_q^-}{V^-} \end{bmatrix} \begin{bmatrix} \boldsymbol{v}^+ \\ \boldsymbol{v}^- \\ \boldsymbol{v}_\perp^+ \\ \boldsymbol{v}_\perp^- \end{bmatrix} \tag{10}$$

Note that since $\boldsymbol{i}_p^-$ is in opposite direction to $\boldsymbol{v}^-$, the inverter should be able to absorb the NSAC. To enable this operating scenario, a path for the energy circulation into the DC-bus should be added. This can be achieved using a battery-based ESS or a controlled chopper with an energy dissipative resistor. This setup helps prevent overvoltage across the DC-bus [25].

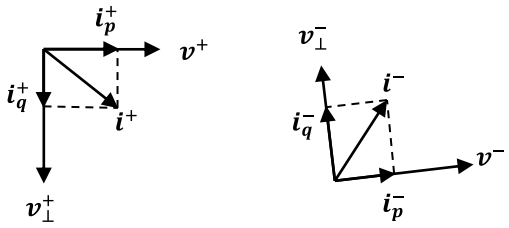

FIGURE 4. Decomposition of active and reactive currents into positive and negative sequences.

Substituting now the condition of (10) into (8) and (9) yields:

$$V^+ = E^+ + R_g I_p^+ + L_g \omega I_q^+ \tag{11}$$

$$V^- = E^- - R_g I_p^- - L_g \omega I_q^- \tag{12}$$

Here E^+ and E^- denote the amplitudes of $\boldsymbol{e}^+$ and $\boldsymbol{e}^-$, respectively. These equations reveal that achieving an optimized voltage support depends not only on the injected grid current components, but also on accurate estimation of the grid parameters [25], [26]. Indeed, the active current is more effective with a resistive grid. When it comes to an inductive grid, the impact of the reactive current is more important.

The optimal voltage support scenario aims to increase V^+ to the recovery threshold value while eliminating V^-. As discussed above, achieving this optimization needs to make appropriate choices regarding the current components. However, it is important to note that this optimization may lead to overcurrent and significant power oscillations.

B. PROTECTION OF THE INVERTER AGAINST OVERCURRENT

To avoid the overheating of power semiconductors and the inverter's damage, the injected current amplitude should never exceed the maximum allowed value (I_{max}) regardless the voltage support approach and the sag severity. Therefore, we shall consider the relationships between different current components and the total current. Additionally, it is important to recognize that the amplitude of the current is not uniform in the three phases. Given that $\boldsymbol{i}_p^-$ and $\boldsymbol{v}^-$ have opposite directions, we can determine the maximum amplitude of the three-phase active current, I_{pmax} as follows.

$$I_{pmax} = \sqrt{I_p^{+^2} + I_p^{-^2} - 2I_p^+ I_p^- cos\theta_{min}} \tag{13}$$

$$cos\theta_{min} = min\left\{cos\theta, cos\left(\theta - \frac{2\pi}{3}\right), cos\left(\theta + \frac{2\pi}{3}\right)\right\} \tag{14}$$

$$\theta = tan^{-1}\left(\frac{v_D^+ v_Q^- + v_Q^+ v_D^-}{v_D^+ v_D^- - v_Q^+ v_Q^-}\right) \tag{15}$$

v_D^+ and v_Q^+ are the DQ components of the positive-sequence voltage across the secondary terminals of transformer T_1. v_D^- and v_Q^- are the DQ components of the negative sequence.

On the other hand, the maximum amplitude of the three-phase reactive current is computed as follows:

$$I_{qmax} = \sqrt{I_q^{+^2} + I_q^{-^2} + 2I_q^+ I_q^- \cos\theta_{max}} \tag{16}$$

$$cos\theta_{max} = max\left\{cos\theta, cos\left(\theta - \frac{2\pi}{3}\right), cos\left(\theta + \frac{2\pi}{3}\right)\right\} \tag{17}$$

To protect the inverter's semiconductors against overcurrent while maximizing its voltage support capability, the optimal scenario consists in injecting a maximum amplitude of the total three-phase current that matches the maximum current allowed by the inverter's semiconductors (I_{max}). Consequently, the correlation between the maximum current amplitude I_{max} and the maximum amplitudes of active and reactive currents, I_{pmax} and I_{qmax}, can be derived from (6) and (7) as follows:

$$I_{max} = \sqrt{I_{pmax}^2 + I_{qmax}^2} \tag{18}$$

As for the grid codes requirements, they recommend limiting the amplitudes of reactive current positive- and negative-sequence, I_q^+ and I_q^-, respectively, to the nominal value I_n to protect the power system against overcurrent. They also specify a tolerated range of values for the gain factors k^+ and k^- that control the amount of reactive current references. These values are commonly set from 2 to 6 as required by German grid codes.

To evaluate the current limitation effectiveness using this approach, the required boosts of reactive current, ΔI_q^+ and ΔI_q^- defined in (1)-(2), are both set to I_n. Considering this, we determine the variation of k^+ and k^- versus V^+ and V^-, respectively as illustrated in FIGURE 5. This figure shows that the values of the gain factors within the range from 2 to 6 do not always guarantee a limitation of PSRC and NSRC amplitudes I_q^+ and I_q^-. Indeed, k^+ should remain within the region bounded by the axis of V^+ and the curve $k^+ = f(V^+)$. Similarly, k^- should remain within the region bounded by the axis of V^- and the curve $k^- = f(V^-)$. To properly address this issue, the strategies introduced in this paper will incorporate the current limitation constraint into the formulation of the gain factor's analytical expressions. This key point will be addressed and discussed in detail in section IV.

C. CONTROL OF OSCILLATING POWERS

In case of asymmetrical voltage sags, the real power, denoted p, is decomposed into a DC component usually referred to as active power (P) and an oscillating AC component ($\tilde{p}$):

$$P = \boldsymbol{v}^+\boldsymbol{i}_p^+ + \boldsymbol{v}^-\boldsymbol{i}_p^- \tag{19}$$

$$\tilde{p} = \boldsymbol{v}^+\boldsymbol{i}_p^- + \boldsymbol{v}^-\boldsymbol{i}_p^+ + \boldsymbol{v}^+\boldsymbol{i}_q^- + \boldsymbol{v}^-\boldsymbol{i}_q^+ \tag{20}$$

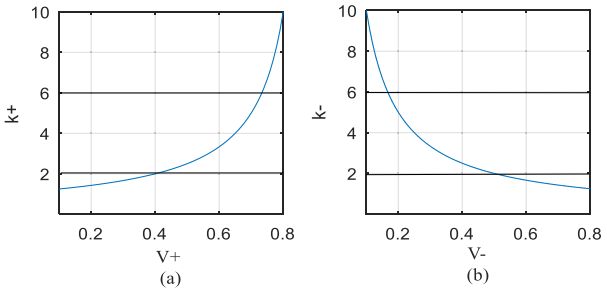

FIGURE 5. Range of gain factors k^+ (a) and k^-(b) to limit the amplitudes of reactive current sequences to its nominal value.

Only the positive and negative sequences of the active current, $\boldsymbol{i}_p^+$ and $\boldsymbol{i}_p^-$, contribute to the active power (P). On the other hand, both sequences of the active and the reactive currents ($\boldsymbol{i}_p^+$, $\boldsymbol{i}_p^-$, $\boldsymbol{i}_q^+$, and $\boldsymbol{i}_q^-$) interact with their reverse counterparts of the grid voltage ($\boldsymbol{v}^-$, $\boldsymbol{v}^+$, $\boldsymbol{v}_\perp^-$, and $\mathbf{v}_\perp^+$), as shown in (20), giving rise to undesirable RPO. Substituting (10) into (19) and (20), yields the expressions of the active power and the oscillating component as elaborated in (21) and (22), respectively. The analytical development is detailed in Appendix A.

$$P = \frac{3}{2}\left(V^+I_p^+ - V^-I_p^-\right) \tag{21}$$

$$\tilde{p} = \underbrace{\frac{3}{2}\left(V^-I_p^+ - V^+I_p^-\right)\cos\delta}_{\tilde{p}_c} + \underbrace{\frac{3}{2}\left(V^+I_q^- - V^-I_q^+\right)\sin\delta}_{\tilde{p}_s} \tag{22}$$

$$\delta = 2\omega t + \theta^+ + \theta^- \tag{23}$$

θ^+ and θ^- are instantaneous phase-angles of positive- and negative-sequence grid voltage. ω is the grid velocity. Likewise, the imaginary power referred to us q, consists of DC component representing the reactive power (Q) and an oscillating component ($\tilde{q}$) computed as given in (24) and (25), respectively:

$$Q = \boldsymbol{v}_\perp^+\boldsymbol{i}_q^+ + \boldsymbol{v}_\perp^-\boldsymbol{i}_q^- \tag{24}$$

$$\tilde{q} = \boldsymbol{v}_\perp^+\boldsymbol{i}_p^- + \boldsymbol{v}_\perp^-\boldsymbol{i}_p^+ + \boldsymbol{v}_\perp^+\boldsymbol{i}_q^- + \boldsymbol{v}_\perp^-\boldsymbol{i}_q^+ \tag{25}$$

The positive- and negative-sequence reactive current, $\boldsymbol{i}_q^+$ and $\boldsymbol{i}_q^-$, impact the reactive power Q, while the interaction between the two sequences of the active and reactive currents with their reverse counterparts of the grid voltage, as shown in (25), produces undesirable ripples in the waveforms of the imaginary power.

Substituting (10) into (24) and (25), we obtain the expressions of reactive power and the oscillating component as given in (26) and (27) (See Appendix A for details).

$$Q = \frac{3}{2}\left(V^+I_q^+ + V^-I_q^-\right) \tag{26}$$

$$\tilde{q} = \underbrace{\frac{3}{2}\left(V^-I_p^+ + V^+I_p^-\right)\sin\delta}_{\tilde{q}_s} + \underbrace{\frac{3}{2}\left(V^-I_q^+ + V^+I_q^-\right)\cos\delta}_{\tilde{q}_c} \tag{27}$$

The following remarks may be raised:
- Considering (19), the choice of $\boldsymbol{i_p^-}$ in opposite direction to $\boldsymbol{v}^-$ contributes to curtailing the active power, being highly encouraged by recent grid codes.
- $\tilde{p}$ and $\tilde{q}$ are two oscillating components at twice the grid frequency and consisting each of two terms. Moreover, the oscillating quantities $\tilde{p}_c$ and $\tilde{q}_s$ depend on the active currents, while $\tilde{p}_s$ and $\tilde{q}_c$ are related to the reactive currents.

1) CONTROL OF REAL POWER OSCILLATIONS

The RPO caused by active currents ($\tilde{p}_c$) can be eliminated by setting the NSAC $\boldsymbol{i_p^-}$ to the following expression:

$$\boldsymbol{i_p^-} = -\frac{I_p^+}{V^+}\boldsymbol{v}^- \tag{28}$$

This condition is perfectly aligned with the voltage support concept discussed in the previous subsection A, which entails the inverter absorbing the NSAC. Similarly, the RPO caused by reactive currents ($\tilde{p}_s$) can be removed by imposing the following NSRC $\boldsymbol{i_q^-}$:

$$\boldsymbol{i_q^-} = \frac{I_q^+}{V^+}\boldsymbol{v}_\perp^- \tag{29}$$

This implies that $\boldsymbol{i_q^-}$ should be in phase with $\boldsymbol{v}_\perp^-$, being quite consistent with the voltage support requirements. Consequently, the optimized voltage support capability can be achieved with zero oscillations in the real power.

2) CONTROL OF IMAGINARY POWER OSCILLATIONS

The IPO caused by the reactive currents ($\tilde{q}_c$) could be nullified by pushing $\boldsymbol{i_q^-}$ to be in opposite phase to $\boldsymbol{v}_\perp^-$ such that:

$$\boldsymbol{i_q^-} = -\frac{I_q^+}{V^+}\boldsymbol{v}_\perp^- \tag{30}$$

On the other hand, the removal of the second oscillating term ($\tilde{q}_s$), caused by the active current, could be achieved by imposing $\boldsymbol{i_p^-}$ to be in phase with $\boldsymbol{v}^-$ such that:

$$\boldsymbol{i_p^-} = \frac{I_p^+}{V^+}\boldsymbol{v}^- \tag{31}$$

Note that the derived relationships in (30) and (31) that cancel out the IPO are not consistent with the voltage support concept requiring $\boldsymbol{i_q^-}$ and $\boldsymbol{v}_\perp^-$ to be in phase, and $\boldsymbol{i_p^-}$ to be in opposite phase to $\boldsymbol{v}^-$.

D. QUALITY OF THE DC-LINK VOLTAGE

The quality of the DC-link voltage serves as a critical factor in ensuring its resilience against transient ripples that occur during and after asymmetrical voltage sags, thus contributing to strengthening the inverter's stability. The amplitude of the ripple in the DC-bus voltage, namely $\tilde{V}_{dc}$, basically relies on four factors including the amplitude of RPO ($\tilde{P}$), the DC component of the DC-link voltage (V_{dc}), the DC-bus capacitance (C_{dc}), and the grid velocity (ω) [28], [31].

$$\tilde{V}_{dc} = \frac{\tilde{P}}{\omega V_{dc} C_{dc}} \tag{32}$$

$\tilde{P}$ is computed using (33):

$$\begin{aligned}\tilde{P} &= \sqrt{\tilde{P}_c^2 + \tilde{P}_s^2} \\ &= \frac{3}{2}\sqrt{\left(V^- I_p^+ - V^+ I_p^-\right)^2 + \left(V^+ I_q^- - V^- I_q^+\right)^2}\end{aligned} \tag{33}$$

Here $\tilde{P}_c$ and $\tilde{P}_s$ denote the magnitudes of the two oscillating terms of the real power $\tilde{p}_c$ and $\tilde{p}_s$, respectively. The magnitude of RPO is clearly affected by the amplitudes of the positive- and negative-sequence voltage, V^+ and V^-, respectively. These sequences are also interconnected with the IPO, as discussed in subsection C. Consequently, it can be inferred that the DC-bus voltage ripple is directly linked to the RPO, though it also exhibits an indirect correlation with the IPO.

IV. PROPOSED FLEXIBLE MULTI-OBJECTIVE LVRT STRATEGIES

In view of the above discussion, the formulation of an effective control strategy to meet LVRT requirements needs to take into consideration the following limitations of the power system:
- Perfect voltage support cannot be achieved without respecting the inverter capacity limits, as this is crucial to protect power semiconductors against overcurrent.
- LVRT strategies are only applied when the voltage-against-time profile illustrated in FIGURE 1 remains within region 1, which requires maximum voltage support performance.
- The simultaneous achievement of a perfect voltage support with elimination of power oscillations is an important challenge. Indeed, eliminating RPO is possible without compromising the voltage support performance. However, eliminating IPO requires the injection of NSAC, which increases the amplitude of the negative-sequence voltage, and reduces the voltage support effectiveness.
- The ripple in the DC-link voltage is influenced by RPO, which theoretically can be eliminated. However, eradicating RPO tends to maximize IPO. This, in turn, results in increased AC voltage fluctuations, deteriorating the power quality and the DC-bus voltage stability.

To properly address these complex challenges, this section introduces three novel LVRT strategies. To execute efficient LVRT operations while adhering to the aforementioned constraints, it is mandatory to determine the appropriate current references generated once the voltage sag is detected.

The following detection method is commonly used [51]: Define the voltage unbalance factor (VUF) as the ratio between the amplitude of the negative-sequence voltage, V^-, and that of the positive sequence, V^+.

$$\text{VUF} = \frac{V^-}{V^+} \tag{34}$$

If V^+ falls below 0.9 p.u., and the VUF exceeds the predefined limit of 0.02, this implies the occurrence of an

asymmetrical voltage sag. If the VUF remains below 0.02, it means that the voltage sag is symmetrical [51].

Most existing strategies in the literature typically derive current references indirectly through the determination of power references. In contrast, the strategies presented in this paper take a different approach by directly determining the current references. They are rooted in recent German FFCI requirements, which outline the general form of reactive current references [36], [37]. Given that the pre-fault amplitudes of the reactive current sequences, I_{q0}^{+} and I_{q0}^{-}, are set to zero, the expressions of the PSRC and NSRC references are given as follows.

$$I_q^{+ref} = k^+ \frac{V_0 - V^+}{V_n} I_n \tag{35}$$

$$I_q^{-ref} = k^- \frac{V^-}{V_n} I_n \tag{36}$$

The appropriate selection of the gain factors is of amount importance to fulfill the LVRT requirements. Considering this, the following strategies are proposed.

A. STRATEGY A

This strategy uses static gain factors to determine the PSRC and NSRC references. It is aligned with the approaches found in some existing strategies presented in reference [20], or those utilized by some EU countries, such as Denmark [44]. As previously discussed in section III-B, the imposed range of the gain factors does not always ensure a complete protection of the inverter against overcurrent. Nevertheless, this strategy is introduced in this paper for the sake of evaluation and comparative analysis.

1) CURRENT REFERENCES

The expressions given in (35) and (36) are adopted to compute the references for the PSRC and NSRC. As for the NSAC reference, it is derived from (10) and (28) as follows.

$$I_p^{-ref} = k_p \frac{V^-}{V^+} I_p^{+ref}, \quad 0 \le k_p \le 1 \tag{37}$$

The introduced gain k_p allows a flexible control of the term $\tilde{p}_c$ caused by the active current components in the RPO. Similar expressions have been proposed in the literature [19]. However, in previous approaches, the gain k_p was typically constrained within the range $[-1,1]$. In contrast, as demonstrated in the previous section, our approach mentioned that the NSAC should not be injected; rather, it should be absorbed by the storage system. This choice serves three main objectives: optimizing voltage support capability, reducing RPO, and accommodating active power curtailment in compliance with recent grid codes. Additionally, the value of k_p should not exceed 1 to limit IPO. In fact, when k_p equals 0, the NSAC is eliminated, while k_p equals 1 removes the term $\tilde{p}_c$.

2) CURRENT LIMITATION

Since the gain factors associated to the PSRC and NSRC remain fixed, the restriction on current amplitude cannot be applied directly to the corresponding current references. Nevertheless, PSRC and NSRC references should be limited to the nominal current I_n. The maximum amplitude of the whole reactive current can be determined by substituting (35) and (36) into (16), which yields as in (38), shown at the bottom of the page.

Furthermore, it is important to ensure that the total active current does not exceed the rated value I_n. To express this restriction formally, we can represent (13) in terms of I_p^{-ref} by substituting I_p^{+ref} from (37) into (13) and replacing I_{pmax} by I_n. This yields the following expression of the maximum allowed NSAC reference, denoted as I_{pmax}^{-ref}:

$$I_{pmax}^{-ref} = \frac{k_p V^- I_n}{\sqrt{V^{+2} + \left(k_p V^-\right)^2 - 2k_p V^+ V^- \cos\theta_{min}}} \tag{39}$$

The generated reference for the NSAC should therefore be bounded by the limit set by I_{pmax}^{-ref}.

3) RESULTING POWERS

The expression of the injected active power can be derived by substituting (37) into (21), which yields:

$$P = \frac{3}{2} \frac{I_p^{+ref}}{V^+} \left(V^{+2} - k_p V^{-2}\right) \tag{40}$$

By substituting (35) and (36) into (26), we obtain the following expression of the injected reactive power:

$$Q = \frac{3}{2} \frac{I_n}{V_n} \left(k^- V^{-2} - k^+ V^{+2} + k^+ V^+ V_0\right) \tag{41}$$

$$I_{qmax} = \frac{I_n}{V_n} \sqrt{\left(k^+ \left(V_0 - V^+\right)\right)^2 + \left(k^- V^-\right)^2 + 2k^+ k^- V^- \left(V_0 - V^+\right) \cos\theta_{max}} \tag{38}$$

$$\tilde{p} = \frac{3}{2} \frac{V^-}{V_n} \left[V_n I_p^{+ref} \left(1 - k_p\right) \cos\delta + \left(\left(k^- + k^+\right) V^+ - k^+ V_0\right) I_n \sin\delta\right] \tag{42}$$

$$\tilde{q} = \frac{3}{2} \frac{V^-}{V_n} \left[V_n I_p^{+ref} \left(1 + k_p\right) \sin\delta + \left(\left(k^- - k^+\right) V^+ + k^+ V_0\right) I_n \cos\delta\right] \tag{43}$$

Furthermore, by replacing (35)-(37) in (22) and (27), we deduce the expressions of the RPO and IPO as in (42) and (43), shown at the bottom of the previous page.

The voltage ripple across the DC-bus can be determined as in (44) by substituting (35), (36), and (37) into (32) and (33).

As can be seen from (44), the DC-bus voltage ripple could be limited when k_p is set to 1. However, with fixed values of k^+ and k^-, the most adopted approach is to use equal values for both gain factors.

To offer a better control of the gain factors, and optimize the current limitation performance, two flexible LVRT strategies are proposed in the two following subsections.

B. STRATEGY B

Strategy B aims to ensure the robustness of the DC-link voltage by primarily eliminating RPO. As previously elucidated in the preceding section III, the NSAC can be absorbed by the storage system rather than being injected into the grid. This approach serves several purposes: 1) enhancing the voltage support capability, 2) eradicating RPO and ripples in the DC-link voltage, and 3) enabling active power curtailment in alignment with modern grid codes requirements.

1) CURRENT REFERENCES

To remove the term $\tilde{p}_c$ caused by active current in the RPO, the reference for the NSAC is derived from (28) as follows.

$$I_p^{-ref} = \frac{V^-}{V^+} I_p^{+ref} \tag{45}$$

The condition for gain factors, k^+ and k^-, that effectively eliminates the term $\tilde{p}_s$ caused by the reactive current in the RPO, is determined by substituting (35) and (36) into (22) and nullifying the term $\tilde{p}_s$, which yields:

$$k^- = k^+ \left(\frac{V_0}{V^+} - 1 \right) \tag{46}$$

The determination of the value of k^+ is contingent upon the current limitation constraint, as elaborated in the subsequent subsection.

2) CURRENT LIMITATION

The maximum current amplitude in the three phases is constrained to I_{max}. However, the active current maximum amplitude, I_{pmax}, as defined in (13), might surpass I_{max}. Therefore, it should be limited to the rated value I_n through limiting NSAC reference I_p^{-ref} to a maximum value I_{pmax}^{-ref}. Substituting I_p^{+ref} in (45) into (13) and replacing I_{pmax} by I_n, the resulting expression of I_{pmax}^{-ref} is obtained as follows:

$$I_{pmax}^{-ref} = \frac{V^- I_n}{\sqrt{V^{+2} + V^{-2} - 2V^+V^- \cos\theta_{min}}} \tag{47}$$

Furthermore, the maximum magnitude of the reactive current is ascertained by inserting (35) and (36) into (16), while considering (46):

$$I_{qmax} = k^+ \frac{(V_0 - V^+)\sqrt{V^{+2} + V^{-2} + 2V^+V^- \cos\theta_{max}}}{V_n V^+} I_n \tag{48}$$

To maintain the total current amplitude within the limit of I_{max}, the gain factor k^+ is subsequently determined by substituting (18) into (48), which yields:

$$k^+ = \frac{V_n}{I_n} \frac{V^+}{(V_0 - V^+)} \sqrt{\frac{I_{max}^2 - I_{pmax}^2}{V^{+2} + V^{-2} + 2V^+V^- \cos\theta_{max}}} \tag{49}$$

Note that the obtained value of k^+ should be confined within the range from 2 to 6 to comply with the FFCI requirements, as long as the amplitude of the reactive current remains below the rated value I_n.

3) RESULTING POWERS

The expression of the resulting active power can be derived by substituting (45) into (21), which yields:

$$P = \frac{3}{2} \frac{I_p^{+ref}}{V^+} \left(V^{+2} - V^{-2} \right) \tag{50}$$

This expression illustrates that the choice of the NSAC reference can effectively reduce the total injected active power, enabling active power curtailment.

Now, by substituting (35) and (36) into (26) and considering (46), we obtain the following expression of the injected reactive power.

$$Q = \frac{3}{2} \frac{I_n}{V_n} \frac{k^+}{V^+} (V_0 - V^+) \left(V^{-2} + V^{+2} \right) \tag{51}$$

The reactive power is completely eliminated when the voltage reaches its pre-fault value namely V_0. With the proposed choice of the gain factors and NSAC reference, the RPO expressed in (22) is nullified, and the resulting voltage-ripple across the DC-link is also eliminated. Substituting (35), (36), and (45) into (27) and considering (46), leads to the following expression of IPO.

$$\tilde{q} = 3 \frac{V^-}{V_n} \left[V_n I_p^{+ref} \sin\delta - k^+ (V_0 - V^+) I_n \cos\delta \right] \tag{52}$$

C. STRATEGY C

It is worth mentioning that Strategy B maximizes IPO, potentially leading to significant fluctuations in the AC voltage. These fluctuations can impact the amplitudes of the voltage sequences and the current references. This gives rise to

$$\tilde{V}_{dc} = \frac{3}{2\omega V_{dc} C_{dc}} \frac{V^-}{V_n} \sqrt{\left(V_n I_p^{+ref} (1 - k_p) \right)^2 + \left(\left(V^+(k^- + k^+) - k^+ V_0 \right) I_n \right)^2} \tag{44}$$

unwanted ripples in the real power waveform, which may in turn affect the DC-bus voltage and result in system instability. To address this concern, strategy C will be focusing on limiting both real and imaginary powers oscillations.

1) CURRENT REFERENCES

To restrict both real and imaginary powers, the reference of the NSAC is set to zero. Moreover, we will use equal values of the gain factors k^+ and k^-:

$$I_p^{-ref} = 0 \tag{53}$$

$$k^+ = k^- \tag{54}$$

2) CURRENT LIMITATION

Since I_p^{-ref} is set to zero, the maximum amplitude of the active current I_{pmax} becomes equal to the PSAC reference I_p^{+ref}, generated by the DC-bus voltage compensator. This reference value should not exceed I_n. The maximum amplitude of the total reactive current is determined as in (55) after substituting (35) and (36) into (16), taking into account (54).

The restriction on current amplitude can be implemented by capping I_{qmax} according to (18). The expression of the gain factors k^- and k^+ in (56), that satisfies the above condition, is elaborated by substituting (18) into (55) and substituting I_{pmax} by I_p^{+ref}.

3) RESULTING POWERS

The expression of the resulting active power is derived by eliminating I_p^- in (21), which yields:

$$P = \frac{3}{2} I_p^{+ref} V^+ \tag{57}$$

Substituting (35) and (36) into (26), while taking into account (54), yields the following expression of the injected reactive power:

$$Q = \frac{3}{2} k^+ \frac{I_n}{V_n} \left(V^{-2} - V^{+2} + V^+ V_0 \right) \tag{58}$$

Substituting (35) and (36) into (27) while considering (53) and (54), the expressions of RPO and IPO are obtained as follows:

$$\tilde{p} = \frac{3}{2} \frac{V^-}{V_n} \left[V_n I_p^+ \cos\delta + k^+ \left(2V^+ - V_0\right) I_n \sin\delta \right] \tag{59}$$

$$\tilde{q} = \frac{3}{2} \frac{V^-}{V_n} \left[V_n I_p^+ \sin\delta + k^+ V_0 I_n \cos\delta \right] \tag{60}$$

Oscillations in both real and imaginary powers are limited, which will help reduce fluctuations in the AC and DC voltages. However, since the oscillations are not completely removed, the voltage ripple across the DC-bus still exists. Substituting (35) and (36) into (32) while considering (33), (53) and (54), yields:

$$\tilde{V}_{dc} = \frac{3}{2} \frac{V^-}{V_n} \frac{\sqrt{\left(V_n I_p^{+ref}\right)^2 + \left(k^+ I_n \left(2V^+ - V_0\right)\right)^2}}{\omega V_{dc} C_{dc}} \tag{61}$$

V. SIMULATION TESTBENCH

A 600 kVA PPM is considered in this study as already depicted in FIGURE 3. The PPM consists of 400 kW PV field and a 200 A battery connected to a common 900 V DC-bus through DC-DC converters enabling a flexible management of the power extracted from the DC sources [52], [53]. A second conversion stage i.e., a two-level VSI is used to dispatch the power from the DC-bus to a 380 V AC LV-bus. The 25 kV PCC is connected to a 230 kV IEEE-9-bus through the step-up transformer T_2 and a 5 km transmission line. The parameters of the IEEE-9-bus are detailed in Appendix B.

A. DC SOURCES FEEDING THE DC-BUS

The PV energy system consists of two sets of 72 PV strings connected in parallel and feeding two DC-DC boost converters. Each string is composed of nine series connected modules. The single-diode model depicted in FIGURE 6 is used to represent each PV cell [56], [57]. Considering this, the cell's current varies as a function of the voltage across its terminals as given in equation (62) [58], [59].

$$i_{cell} = I_{ph} - I_s \left(e^{\frac{q(R_s i_{cell} + v_{cell})}{KT}} - 1\right) - \frac{R_s i_{cell} + v_{cell}}{R_{sh}} \tag{62}$$

i_{cell} and v_{cell} are the current generated by and the voltage across one PV cell. I_{ph} represents the photocurrent. R_s and R_{sh} are the series and shunt resistors, respectively. I_s is the saturation current of one diode D_{pv}. q, η, K and T are the electron charge, the ideality-factor of the diode, the Boltzmann constant, and the operating temperature, respectively.

On the other hand, FIGURE 7 depicts a simplified power circuit of one DC-DC boost converter fed by 72 PV strings and the MPPT-based control block diagram [58], [59], [60], [61], [62]. The corresponding average state-space model is

$$I_{qmax} = k^+ \frac{\sqrt{\left(V_0 - V^+\right)^2 + V^{-2} + 2V^- \left(V_0 - V^+\right) \cos\theta_{max}}}{V_n} I_n \tag{55}$$

$$k^+ = k^- = \frac{V_n}{I_n} \times \sqrt{\frac{I_{max}^2 - I_p^{+ref\,2}}{\left(V_0 - V^+\right)^2 + V^{-2} + 2V^- \left(V_0 - V^+\right) \cos\theta_{max}}} \tag{56}$$

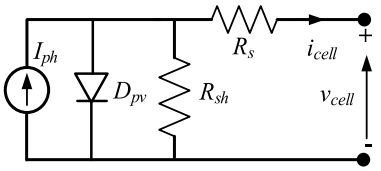

FIGURE 6. Single-diode model of the PV cell.

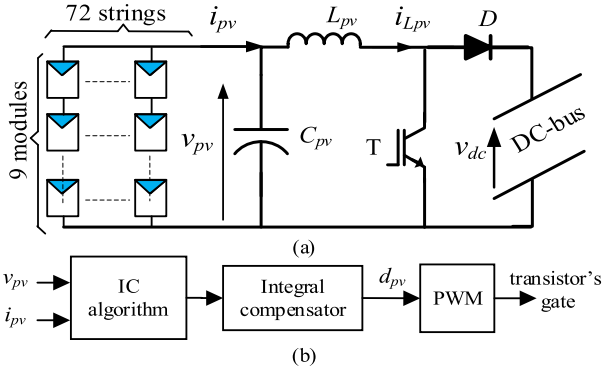

FIGURE 7. Power circuit and control diagram of one DC-DC boost converter connected to 72 PV strings and feeding the DC-bus.

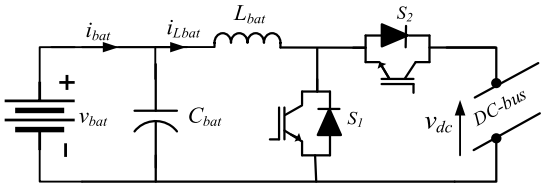

FIGURE 8. Power circuit of one DC-DC boost converter connected to 72.

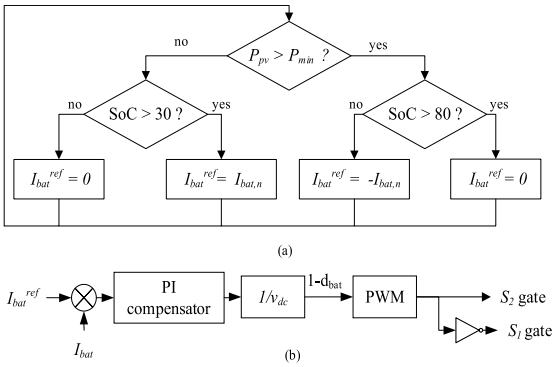

FIGURE 9. (a) Flowchart of the battery charge discharge reference current (b) simplified block diagram of the buck-boost controller.

given in (63) [58], [59].

$$\begin{cases} \dfrac{d}{dt} i_{Lpv} = \dfrac{1}{L_{pv}} v_{pv} + \dfrac{1}{L_{pv}} \left(d_{pv} - 1\right) v_{dc} \\ \dfrac{d}{dt} v_{pv} = -\dfrac{1}{C_{pv}} i_{Lpv} + \dfrac{1}{C_{pv}} i_{pv} \end{cases} \tag{63}$$

C_{pv} and L_{pv} are the capacitance and inductance used in the boost converter. i_{Lpv} is the current through the inductor L_{pv}, v_{pv} and i_{pv} are the voltage across and current generated by the PV array, respectively. v_{dc} is the DC-bus voltage assumed to be constant and perfectly regulated by the grid-connected converter. d_{pv} is the duty cycle of the PWM signal feeding the transistor's gate. Considering this, the MPPT technique employs the incremental conductance (IC) algorithm along with an Integral (I) compensator and a pulse width modulation (PWM) module to generate the appropriate gate signal for the boost converter's power transistor [61], [62].

As for the energy storage system, we used two packs of lead-acid batteries connected each to a bidirectional DC-DC buck-boost converter as depicted in FIGURE 8 [63]. v_{bat} is the battery terminal voltage. C_{bat} and L_{bat} are the capacitance and inductance of the buck-boost converter, respectively. i_{Lbat} is the current through the inductor L_{bat}. S_1 and S_2 are two power semiconductors, capable to conduct a bidirectional current. i_{bat} is the battery's current. The corresponding average state-space model is described by (64) [64], [65].

$$\begin{cases} \dfrac{d}{dt} i_{Lbat} = \dfrac{1}{L_{bat}} v_{bat} - \dfrac{1}{L_{bat}} \left(1 - d_{bat}\right) v_{dc} \\ v_{bat}(t) = E_{oc} - K_{bat} \left(\dfrac{Ch_{bat}}{A_{bat}(I_{bat} = 0, T)} \right) - R_{bat} i_{bat}(t) \end{cases} \tag{64}$$

E_{oc} is the battery's open-circuit voltage at full charge. K_{bat} is a constant specific to the battery, A_{bat} is the nominal capacity, R_{bat} is the internal resistance, and $\mathrm{Ch_{bat}}$ is the extracted charge. d_{bat} is the duty cycle corresponding to the 'on' state over a pulse period of the power switch S_1. Therefore, the duty cycle corresponding to the 'on' state of S_2 is $(1 - d_{bat})$.

$$\begin{cases} \dfrac{di_D^+}{dt} = -\dfrac{R}{L} i_D^+ + \omega i_Q^+ + \dfrac{1}{L} u_{iD}^+ - \dfrac{1}{L} v_D^+ \\ \dfrac{di_Q^+}{dt} = -\dfrac{R}{L} i_Q^+ - \omega i_D^+ + \dfrac{1}{L} u_{iQ}^+ - \dfrac{1}{L} v_Q^+ \\ \dfrac{di_D^-}{dt} = -\dfrac{R}{L} i_D^- - \omega i_Q^- + \dfrac{1}{L} u_{iD}^- - \dfrac{1}{L} v_D^- \\ \dfrac{di_Q^-}{dt} = -\dfrac{R}{L} i_Q^- + \omega i_D^- + \dfrac{1}{L} u_{iQ}^- - \dfrac{1}{L} v_Q^- \\ \dfrac{dv_{dc}}{dt} = \dfrac{i_{dc}}{C_{dc}} - \dfrac{3}{2 C_{dc} v_{dc}} \left(v_D^+ + v_D^- + v_Q^+ + v_Q^-\right) \left(i_D^+ + i_D^- + i_Q^+ + i_Q^-\right) \end{cases} \tag{65}$$

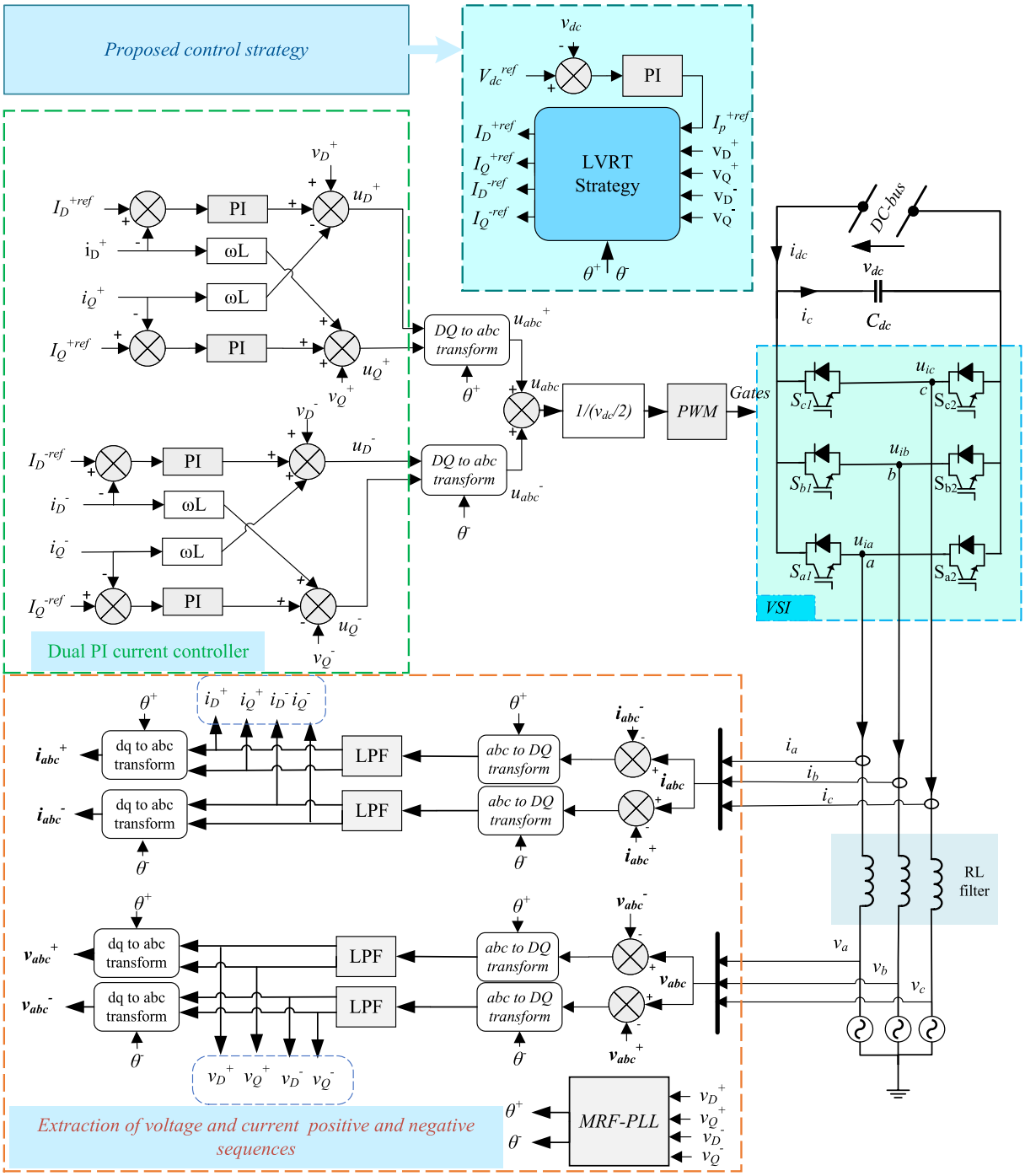

FIGURE 10. Power circuit of the grid-connected inverter and the corresponding controller established in dual synchronous reference frame.

The approach used to determine the appropriate reference charge- and discharge-current of the battery, namely I_{bat}^{ref}, is depicted in the flowchart of FIGURE 9.a.

SoC is the battery's state of charge, P_{pv} is the active power delivered by the PV system, P_{min} is the minimum charging power of the battery and $I_{bat,n}$ is the nominal battery's current. If the available PV power (P_{pv}) surpasses P_{min} and the battery's SoC is under the threshold set to 80%, then I_{bat}^{ref} is set to $-I_{bat,n}$ implying the battery is being charged at its nominal current. Once the SoC exceeds 80%, the battery charging process is halted, implying that I_{bat}^{ref} is set to zero.

Conversely, if P_{pv} is less than P_{min}, and the battery's SoC is greater than 30%, I_{bat}^{ref} is set to $I_{bat,n}$ implying that the battery contributes to the power injection into the grid. Consequently, the SoC will decrease. Once it reaches the 30% threshold value, I_{bat}^{ref} is set to zero and the battery is no longer contributing to the grid support. Afterwards, a PI compensator along with a PWM module are used to control the buck-boost

converter and generate the target reference current as depicted in the flowchart of FIGURE 9b.

B. GRID-CONNECTED VSI

The power circuit of the grid-connected VSI is depicted in FIGURE 10. The corresponding dynamic model, established in a dual reference frame synchronized with the positive- and negative-sequence grid voltage, is as in (65), shown at the bottom of the page 14, [9], [68], [67]. ($i_D^+, i_Q^+, i_D^-, i_Q^-$) are the DQ components of the positive- and negative-sequence grid current expressed in the dual synchronous reference frame [66], [67]. ($v_D^+, v_Q^+, v_D^-, v_Q^-$) are the DQ components of the positive- and negative-sequence voltage across the secondary terminals of transformer T_1. The DQ components are obtained from the measured signals in the abc reference frame using two Park transformations and four low-pass filters as shown in the bottom part of the block diagram of FIGURE 10 [66], [67].

A Multiple-Reference-Frame-Phase-Locked Loop (MRF-PLL) is also implemented to estimate the instantaneous phase-angles of positive- and negative- sequence grid voltages, namely θ^+ and θ^-, being mandatory to perform the two Park transformations [66]. u_{iD}^+, u_{iQ}^+, u_{iD}^-, and u_{iQ}^- are the DQ components of the positive- and negative-sequence voltage across the inverter's terminals. R and L are the grid filter resistance and inductance, respectively.

On the other hand, different voltage and current control loops are implemented to control the VSI as depicted in the upper part of the block diagram of FIGURE 10. First, a PI compensator-based outer loop is implemented to regulate the DC-bus voltage. The control-law generated by the DC voltage compensator is used by the proposed LVRT control strategy to determine the appropriate DQ components of the positive- and negative-sequence current references, namely I_D^{+ref}, I_Q^{+ref}, I_D^{-ref} and I_Q^{-ref}, respectively. Finally, we used a dual PI-based current controller implemented in a dual synchronous reference frame to enable the grid currents, i_D^+, i_Q^+, i_D^-, and i_Q^-, to follow their target references [68]. The derived control-laws for the inverter, u_D^+, u_Q^+, u_D^-, and u_Q^-, are transformed to the abc reference frame and applied at the input of a PWM modulator to generate the transistors' gates signals.

VI. NUMERICAL TEST CASES

To evaluate the proposed LVRT strategies, we conducted numerical simulations using the Matlab/Simulink software. The system parameters are summarized in Table 3.

In this section, we will evaluate and compare the performance of the proposed strategies in different fault scenarios. Among the obtained results, the following are particularly noteworthy:

1) The amplitudes of the injected currents I_p^+, I_p^-, I_q^+ and I_q^-.

TABLE 3. Power system and controllers' parameters.

Parameter		symbol	Value
Sample frequency		f_c	10 kHz
Grid fundamental frequency		ω	120π rd/s
Output filter resistance		R	0.0167 Ω
Output filter inductance		L	0.25 mH
Inverter-rated current (amplitude)		I_n	900 A
inverter fault current		I_{max}	1.2 *p.u.*
Short-circuit current/ maximum duration		$I_{max\text{-}sc}$	2.5 p.u. / 40 ms
DC-bus voltage		V_{dc}	900 V
DC-bus capacitance		C_{dc}	40 mF
Battery's nominal current		I_{bat}^{nom}	200 A
Battery's voltage		V_{bat}	450 V
Battery's nominal capacity		A_{bat}	1 kAh
PV source power		P_{pv}	400 kW
Dual PI current controller	proportional gain	K_{p_pi}	0.7
	integral gain	K_{i_pi}	10
DC-bus PI Controller	proportional gain	K_{p_dc}	2.5 p.u.
	integral gain	K_{i_dc}	100 p.u.
Buck-boost PI controller	proportional gain	K_{p_bat}	0.9 p.u.
	integral gain	K_{i_bat}	10 p.u.

2) The waveforms of the injected three-phase currents, serving for the assessment of the current limitation strategy.

3) Instantaneous real and imaginary powers which illustrate the impact of the proposed strategies on power oscillations.

4) The DC-link voltage providing insight into the assessment of robustness requirements.

5) The positive- and the negative-sequence voltage at various locations such as the connection point of the inverter (LV AC side), the PCC, and bus 6. These voltage sequences are useful to evaluate the performance of voltage support.

A. RESULTS

1) TEST CASE I: BG FAULT ACROSS BUS 8

In this scenario, a ground fault (bg fault) occurred in bus 8, leading to a voltage sag that had an impact on the amplitude of phase b voltage across bus 6, which drops to 0.36 p.u. The fault is then propagated to the PCC via Transformer T_2, resulting in a voltage sag in phases a and b, causing a drop in their amplitudes to 0.674 p.u. and 0.597 p.u., respectively. Consequently, different values of the VUF were recorded at various locations. For instance, it is about 0.33 across bus 8, 0.23 across bus 6 and 0.28 at the PCC. In addition to the location, these values are contingent on the presence of transformers and the currents amplitudes in each bus.

FIGURE 11 illustrates the waveforms of the powers generated by the PV system and the battery. Notably, the negative power values associated with the battery denote a charging process that occurs before, during, and after the fault event. It is due to the SoC being below 80%. Conversely, the PV source consistently supplies its nominal power. The outcomes

reveal that the produced powers exhibit minimal transient fluctuations, with the PV source experiencing less than a 1.5% deviation, while the battery shows a 9% fluctuation.

First, the results obtained using Strategy A, with reactive current gain factors set to 6 and the NSAC set to zero ($k_p = 0$), are depicted in FIGURE 12. These results highlight that the approach based on using static reactive current gain factors can potentially lead to DC-Bus instability, even when the current amplitude is limited. This phenomenon can be attributed to the fact that the voltage profile undergoes changes while the gain factors k^+ and k^- controlling the reactive currents remain fixed, resulting in currents and powers oscillations.

The increase of RPO leads in turn to the degradation of the DC-bus voltage quality experiencing an important transient ripple. This example underscores the crucial importance of having flexibility in choosing gain factors to achieve stable performance. Similar results are obtained for different values of k_p. As for LVRT capability, it can be achieved, in this case study, for k^+ and k^- inferior to 6.

Secondly, FIGURE 13 displays the results obtained using Strategy B. It demonstrates that the current limitation capability and DC-bus stability experience both a better performance compared to Strategy A. The current amplitude is indeed maintained between 0.96 p.u. and 1.2 p.u. Only one transient peak of about 1.24 p.u. and surpassing the allowable limit has occurred in only one cycle. This operation scenario can be tolerated and has no impact on the safety of the inverter's semiconductors, regarding the parameters listed in Table 3. As for the power oscillations, it was theoretically anticipated that RPO would be eliminated using this strategy. However, the results reveal significant oscillations in the waveforms of both real and imaginary powers resulting in an oscillating DC-link voltage. The latter experienced two transient peaks of about 1.064 p.u. and 0.94 p.u. at the onset of the fault and a voltage ripple during the transient regime with an amplitude inferior to 2.5%.

The obtained performance of the RPO and DC-link voltage can be attributed to two factors. First, this strategy increases IPO. These oscillations give rise to fluctuations in AC voltage, impacting the amplitudes of voltage sequences and current references, and resulting in RPO. The latter gives rise to unwanted ripple in the DC-link voltage. Second, the current references generated by the control strategy are constrained by the gain factors values being limited from 2 to 6, to satisfy FFCI requirements. This operation range restricts the control of power oscillations and the maximization of current injection with respect to the inverter capacity. This fact can be demonstrated by the saturation of the gain factors values as illustrated in FIGURE 15.a. Note that despite the oscillatory waveform, the DC-bus voltage exhibited a robust behavior, maintaining its amplitude within the range 0.95 p.u. to 1.03 p.u. Therefore, the LVRT requirement is favorably met, enabling the grid voltage support.

On the other hand, the imbalance factor at the AC-side of the inverter was reduced to 0.187. However, effective voltage support at the PCC was hindered by both the voltage drop induced by the transformers and the relatively low amount of injected current/power compared to the required amount. Indeed, the IEEE-9-bus power generators produce short-circuit powers ranging from 128 MVA to 247.5 MVA, while the simulated PPM generates a 600 kVA short-circuit power. To enhance the voltage support capability, we shall therefore increase the total power injected into the PCC.

Finally, FIGURE 14 shows the results obtained with Strategy C. Notable observations include the full capacity operation of the inverter, which improves the voltage support effectiveness, as evidenced by a VUF of 0.12 at the point of connection of the inverter. Robust behavior of the DC-bus voltage is also confirmed. Nevertheless, oscillations are observed in the waveforms of voltage sequences, instantaneous powers, and consequently, the DC-link voltage. The enhanced performance using this strategy is due to the gain factors flexibility showing less saturated values compared to strategy B as illustrated in FIGURE 15.b.

The DC-bus voltage exhibited oscillations with amplitudes ranging from 0.96 p.u. to 1.03 p.u. Only one transient peak of 1.04 p.u. occurred at the fault's initiation. The fluctuations of this voltage during the transient regime remain within the range 3% to 3.5%. These issues can be addressed more effectively using advanced non-linear DC-bus voltage and line current controllers.

The summarized results of the proposed strategies B and C under this test case are provided in Table 4.

2) TEST CASE II: BCG FAULT ACROSS BUS 8

In the event of a bcg fault occurring in bus 8, bus 6 experiences an unbalanced voltage sag leading to a decrease in the voltage amplitudes to 0.87 p.u., 0.31 p.u., and 0.34 p.u. in phases a, b and c, respectively. At the PCC, the voltage amplitudes of phases a, b, and c are 0.6 p.u., 0.28 p.u., and 0.678 p.u., respectively.

With Strategy A, the results indicate that LVRT capability is only achieved when k^+ and k^- are both inferior to 3 and k_p set to zero. For k_p set to 1, the entire range from 2 to 6 fails to guarantee compliance with LVRT requirements.

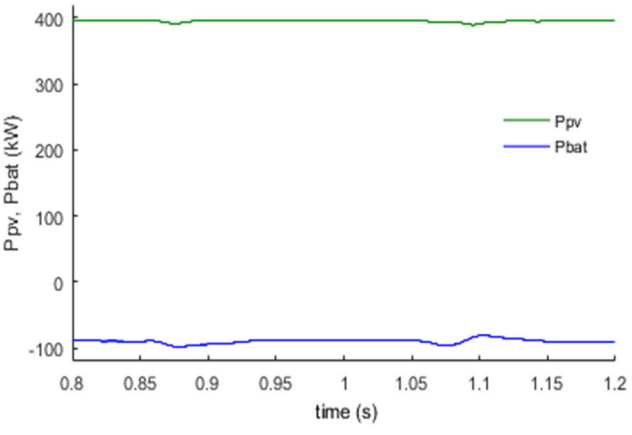

FIGURE 11. Power produced from the PV field and the battery.

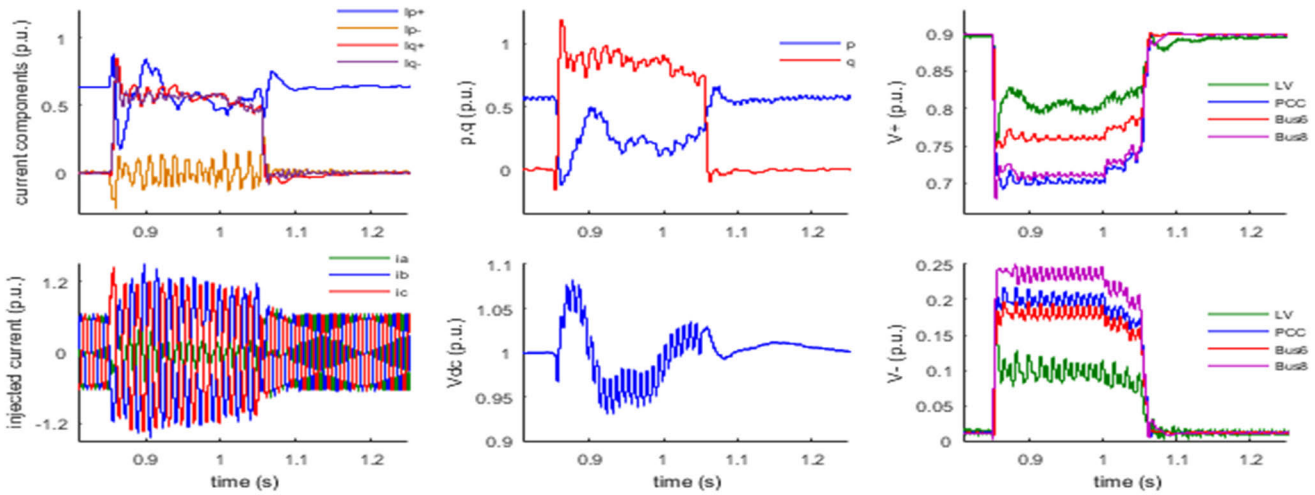

FIGURE 12. Simulation results for $k_p = 0$, $k^+ = k^- = 6$ under a voltage sag caused by a bg fault across the bus 8.

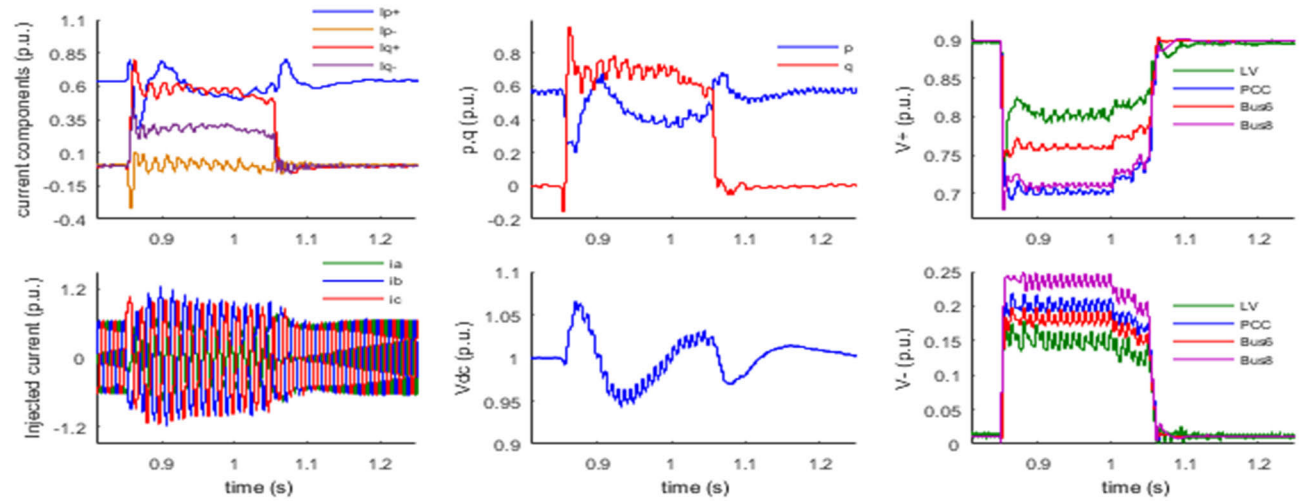

FIGURE 13. Simulation results with Strategy B under a voltage sag caused by a bg fault across the bus 8 for k^+ and k^- between 2 and 6.

TABLE 4. Performance evaluation of proposed strategies for test case I.

		Strategy B	Strategy C
DC-bus voltage	Transient peaks:	0.94, 1.064 p.u.	0.961, 1.041 p.u.
	Fluctuations	<2.5%	<3.5%
Current	Amplitude	0.96-1.2 p.u.	1.2 p.u.
	Transient peak	1.24 p.u.	1.28 p.u.
LVRT		Medium	High
VUF	Faulty bus	0.33	0.33
	Inverter side	0.187	0.12

TABLE 5. Performance evaluation of proposed strategies for test case II.

		Strategy B	Strategy C
DC-bus voltage	Transient peaks:	0.911, 1.056 p.u.	0.953, 1.037 p.u.
	Fluctuations	<2.5%	<2%
Current	Amplitude	1.35 p.u.	1.2- 1.35 p.u.
	Transient peak	1.45 p.u.	1.45 p.u.
LVRT		Low	Medium
VUF	Faulty bus	-	1
	Inverter side	-	0.27

A summary of the performances obtained with Strategies B and C is provided in Table 5. FIGURE 16 shows the results obtained using Strategy B. It is observed that the power oscillations are limited, leading to a stable DC-link voltage, at the

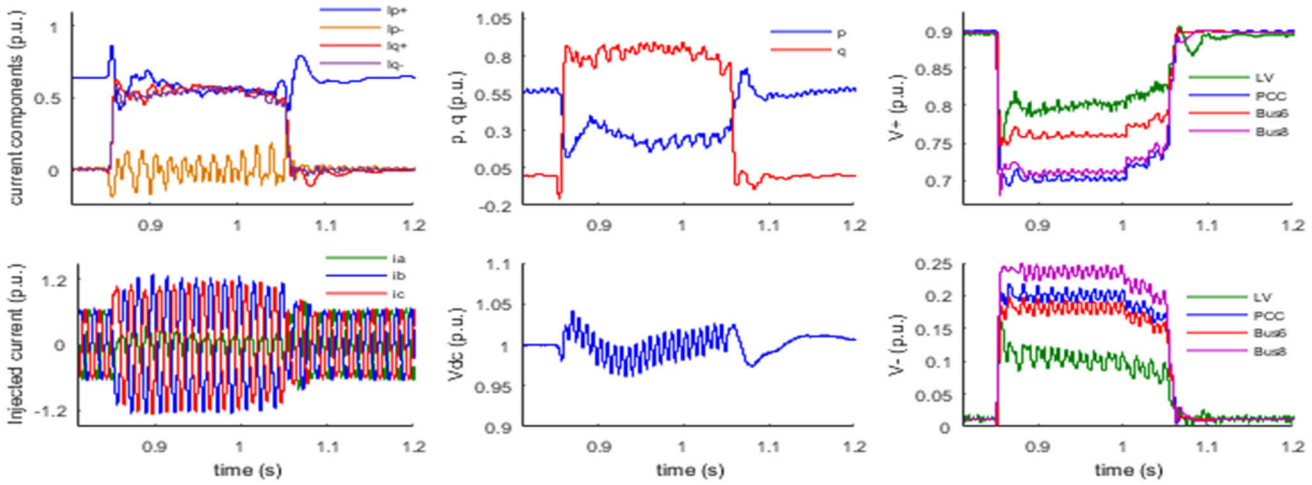

FIGURE 14. Simulation results with Strategy C under a voltage sag caused by a bg fault across the bus 8 with k^+ and k^- between 2 and 6.

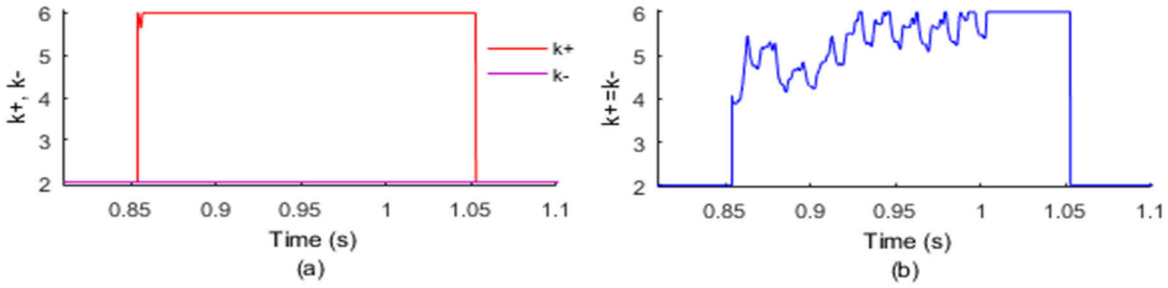

FIGURE 15. Gain factors variation under a bg fault across the bus 8: (a) using strategy B ($k^+ \neq k^-$), (b) using strategy C ($k^+ = k^-$).

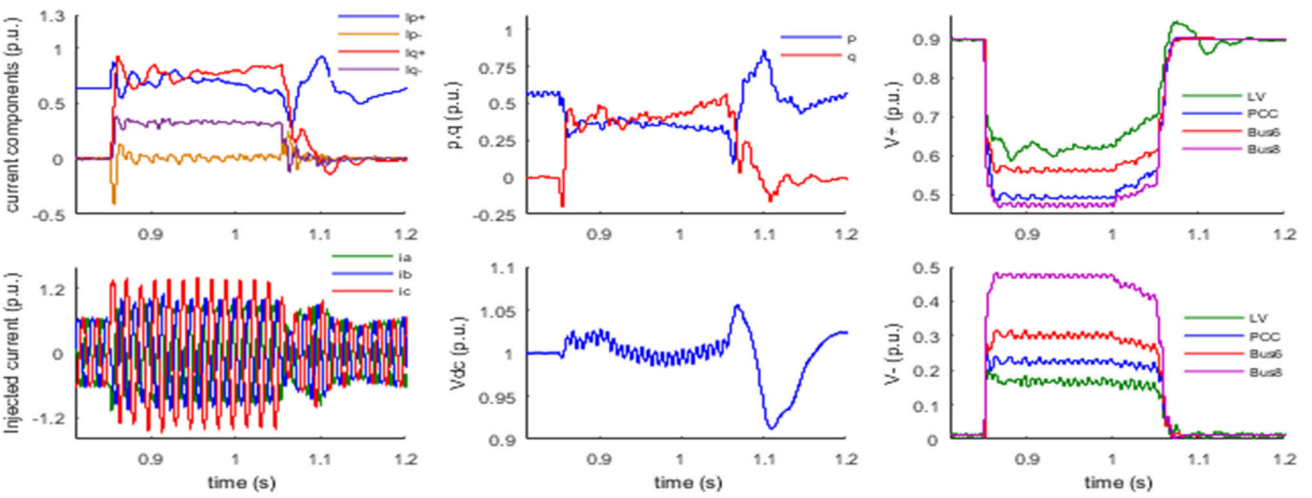

FIGURE 16. Simulation results with Strategy B under a voltage sag caused by a bcg fault across the bus 8 for k^+ and k^- between 2 and 6.

onset of the fault. However, when the grid voltage recovers, we can see important transient oscillations in the DC-bus voltage. The reported amplitudes of this waveform are 0.911 p.u. and 1.056 p.u. Furthermore, the current limitation objective is not achieved. Specifically, the phase c current amplitude is equal to 1.35 p.u., exceeding the maximum allowable value.

The current limitation technique should ideally restrict this value, but the imposed range of gain factors hinders the fulfillment of this requirement. This fact is proved by the saturated value of the gain factor k^- as illustrated by FIGURE 18.a., which limits the strategy objectives achievement in terms of power oscillations and current limitation.

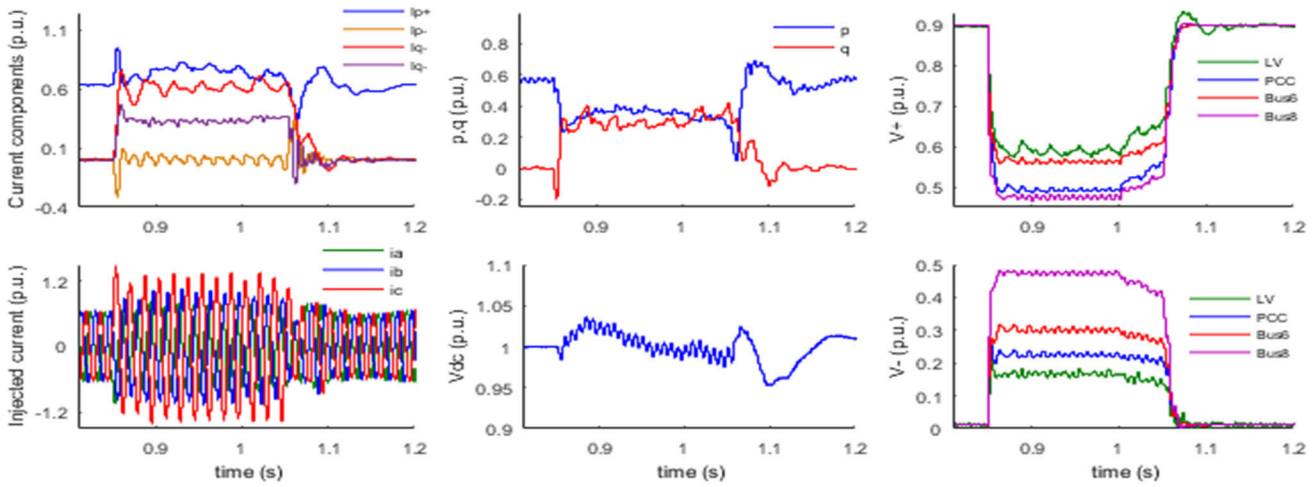

FIGURE 17. Simulation results with Strategy C under a voltage sag caused by a bcg fault across the bus 8 (k^+ and k^- between 2 and 6).

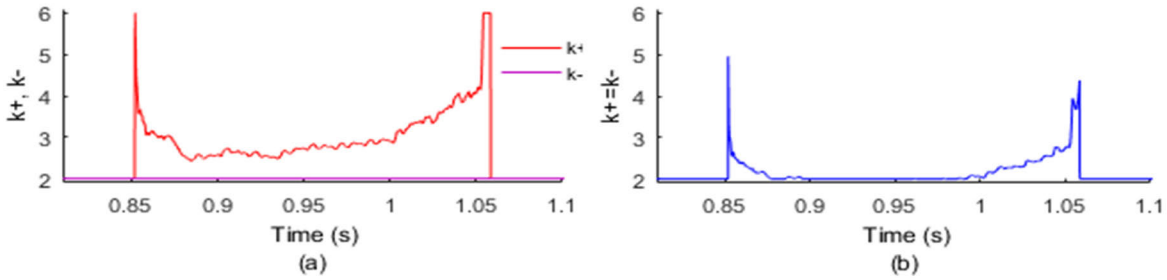

FIGURE 18. Gain factors variation under a bcg fault across the bus 8: (a) using strategy b ($k^+ \neq k^-$), (b) using strategy C ($k^+ = k^-$).

It is worth noting that with gain factors limited within the range 0.5 to 4, results using Strategy B demonstrated better LVRT capability.

The obtained results using Strategy C are displayed in FIGURE 17 showcasing improved performance compared to Strategy B. Specifically, there is a lower transient deviation in the DC-bus voltage, remaining under 7%. The voltage fluctuations, with a maximum of 2%, fall within the allowed limit of 5%. The maximum amplitude of the injected current deviates between 1.2 p.u. and 1.35 p.u., occasionally exceeding I_{max}. Note that the inverter can support a short-circuit current beyond I_{max} if its duration does not exceed 40 ms. This issue arises due to the FFCI requirements, which mandate a minimum gain factor of 2 if the reactive current component is under I_n, while the value of k^- required by the current limitation technique occasionally falls below this threshold in this scenario. This fact explains the saturated value of the gain factor as depicted in FIGURE 18.b. Consequently, during this time period, the injected current exceeds the allowable limit. The voltage support is optimized through the sustained full-capacity operation, primarily impacting the negative-sequence voltage, and reducing the VUF to 0.27. This contrasts with the VUF values at the PCC, bus 6, and bus 8, which are obtained as 0.46, 0.535, and 1, respectively. Nonetheless, for a more effective voltage support capability, a higher current output, i.e. a higher rate of power production from the PPM, would be beneficial.

3) TEST CASE III: BG FAULT ACROSS BUS 6

When a bg fault occurs in bus 6, it leads to a 4% increase in the voltage amplitudes of the remaining two phases. The transformer T_2 alters the fault type, resulting in an uneven impact on the voltage at the PCC. Specifically, phases a and c experience a voltage drop of 0.1 p.u., while the voltage across phase b decreases to 0.358 p.u.

The voltage at the point of connection of the inverter is also affected asymmetrically by the fault, and the observed behavior depends on the control strategy employed by the inverter. The LVRT capability using Strategy A is only achieved when the gain factor is below 3. The voltage support performance is impacted by the fact that it is not always possible to maximize the injected current.

Table 6 summarizes the performance of strategies B and C. Moreover, FIGURE 19 displays the results obtained using Strategy B. Unfortunately, RPO is not eliminated due to the influence of IPO on AC voltage fluctuations.

The DC-link voltage exhibits an oscillating transient behavior at the onset of the fault with peaks equal to 0.91 and 1.09 p.u., respectively. In addition, a transient peak equal to 0.93 p.u. occurred at the recovery of the grid voltage.

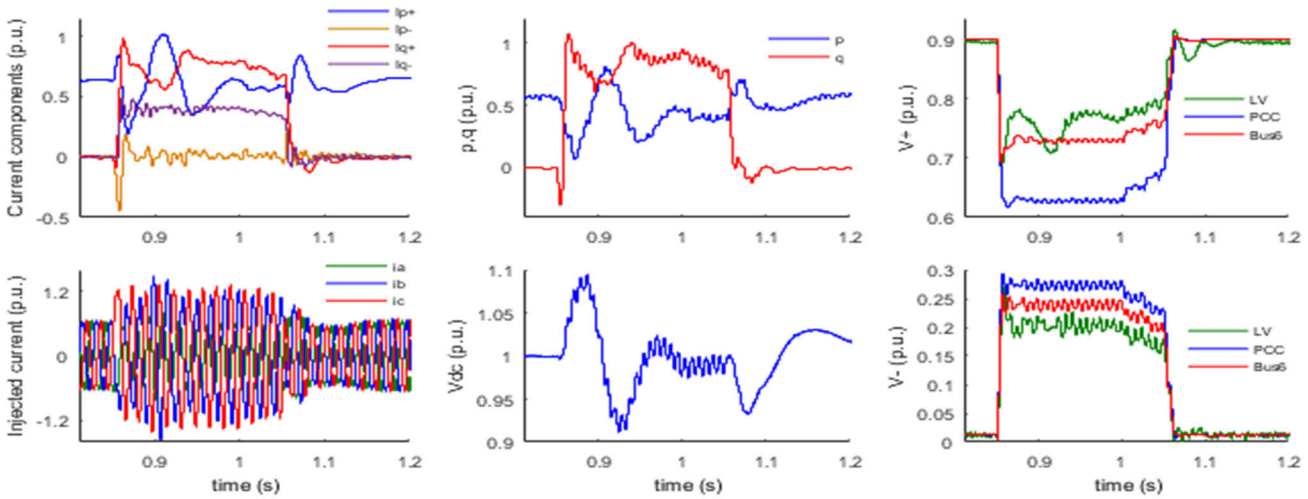

FIGURE 19. Simulation results with Strategy B under a voltage sag caused by a bg fault across the bus 6 for k^+ and k^- between 2 and 6.

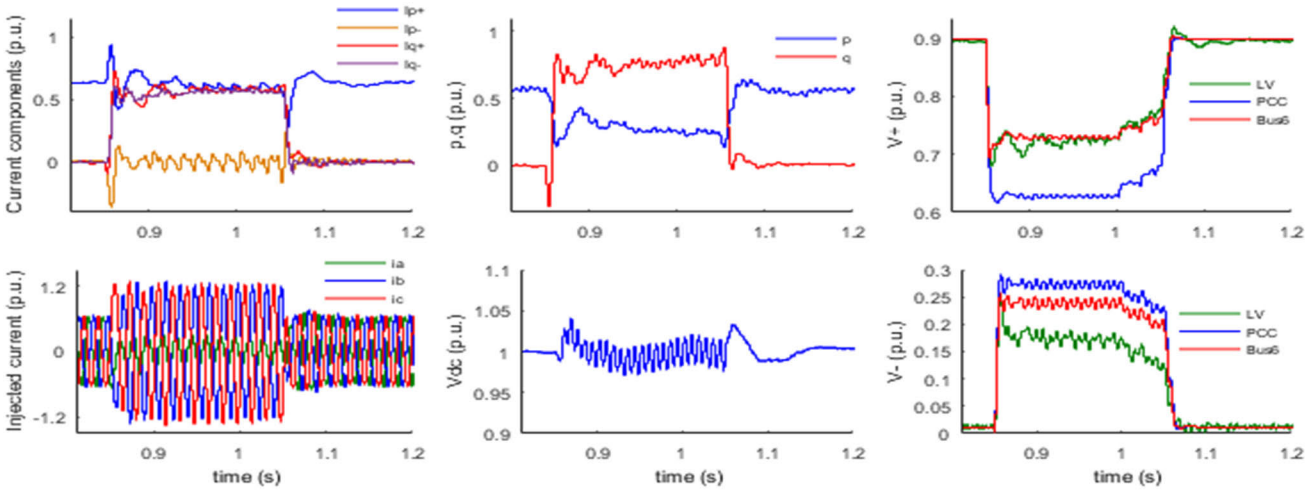

FIGURE 20. Simulation results with Strategy C under a voltage sag caused by a bg fault across the bus 6 for k^+ and k^- between 2 and 6.

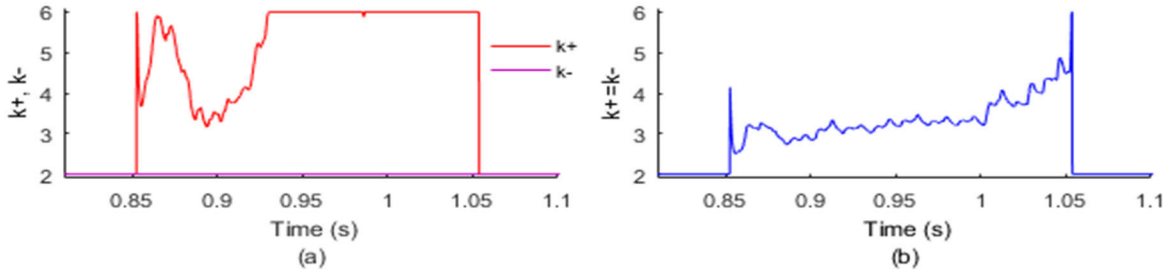

FIGURE 21. Gain factors variation under a bg fault across the bus 6: (a) using strategy C (k^+=k^-), (b) using strategy b (k^+≠k^-).

As for the maximum current amplitude, it shows an oscillating behavior with an amplitude ranged from 1.2 to 1.3 p.u. Similarly to the previous results, the gain factor k^- is saturated to 2 as depicted in FIGURE 21.a. These results lead to critical LVRT performance and a risk of disconnection of the inverter from the grid.

The results, obtained with Strategy C, are illustrated in FIGURE 20. The current waveforms demonstrate the injection of the maximum allowed amplitude in two phases (a and c). This reduces the VUF to 0.23. Additionally, Strategy C yields better-quality of the injected power and DC-link voltage compared to Strategy B. The reported transient peak

TABLE 6. Performance evaluation of proposed strategies for test case III.

		Strategy B	Strategy C
DC-bus voltage	Transient peaks:	0.91, 0.93, 1.09 p.u.	0.97, 1.04 p.u.
	Fluctuations	< 2.5%	< 3.5%
Current	Amplitude	1.2-1.3 p.u.	1.2-1.26 p.u.
	Transient peak	1.5 p.u.	-1.3 p.u.
LVRT		Low	Medium
VUF	Faulty bus	0.32	0.32
	Inverter side	0.25	0.23

values are equal to 0.97 p.u. and 1.04 p.u., respectively; their fluctuation amplitude is inferior to 3.5%. The current waveforms show a maximum amplitude of 1.2 to 1.3 p.u. The gain factors are varying according to FIGURE 21.b.

In this test case, Strategy C performs better in terms of LVRT capability than both Strategies A and B. However, it is crucial to remind that the maximum available current amplitude limits the voltage support effectiveness.

4) ENHANCING PERFORMANCE: VOLTAGE REGULATION EQUIPMENT INTEGRATION WITH LVRT-BASED PPM

In this section, we modified the structure of the proposed test bench with the integration of a voltage regulation equipment, aiming to assess the synergistic effects when coupled with strategy C. The incorporation of a voltage regulator introduces an additional layer of control. By combining LVRT strategy and voltage regulation, we aim to uncover potential enhancements in the system stability, resilience, and overall operational efficiency.

It is worth mentioning that the proposed LVRT strategies, implemented on the grid-connected inverter to contribute to the grid voltage support, are in no way a replacement of the voltage regulation equipment, such as tap changers and capacitor banks.

Such equipment is strategically placed across feeders to maintain voltage within the tolerated range [69], [70], [71], [72], [73], [74]. This is crucial for ensuring stable voltage delivery to end-users, a requirement increasingly essential in smart grids [69]

In the preceding simulation tests, we employed traditional power converters and transformers devoid of voltage regulation equipment. This approach allows us to contrast the results with existing LVRT and voltage support strategies, typically excluding var/voltage regulation equipment [19], [20], [21], [22], [23], [24], [25], [26], [27], [28]. While var/voltage regulators could reduce the produced voltage drop, our aim, following the structure outlined in [50], was to generate various voltage sag types across the PCC using the IEEE-9-bus model, representing the grid. This approach simplifies the production of different sag types, particularly challenging near the PCC. To further enhance grid stability and performance, we explore the combined use of LVRT strategies and an On-Load-Tap-Changing (OLTC) transformer, chosen for its ability to regulate voltage by adjusting the tap position of the transformer [72].

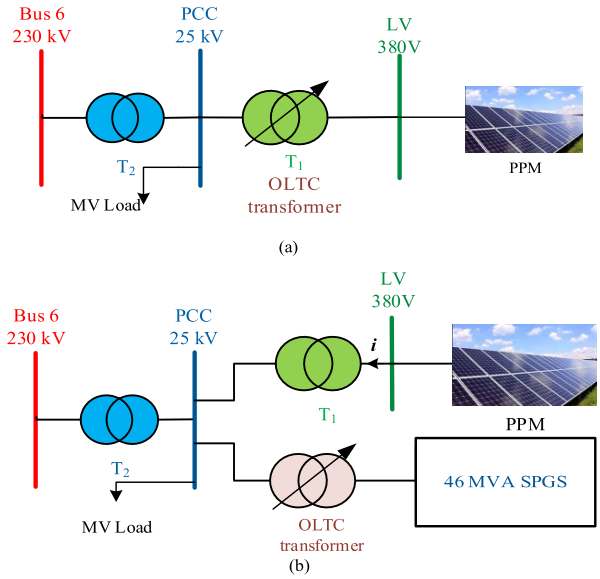

FIGURE 22. Combination of LVRT strategy and voltage regulation equipment.

To assess this combination, we suggest replacing transformer T_1, connecting the PPM to the PCC, with an OLTC transformer as depicted in FIGURE 22.a. Simulation results, employing strategy C during an important fault across the bus 6 (bg fault), are shown in FIGURE 23. The outcomes reveal stable performance for both PPM and the grid, with reduced AC voltage fluctuation and maintained current and DC-link voltage quality. Positive-sequence voltage increases across the PCC and the bus 6 similarly to results without voltage regulation (FIGURE 20). However, mitigating negative-sequence voltage has proved to be slightly less effective with the OLTC transformer. This fact is due to the lack of ability to separately regulate the positive- and negative-sequence voltage.

Additionally, separate control of the transformer's windings during unbalanced voltage sag may degrade system performance.

Considering that the capacity of the inverter, in terms of maximum current supported by semi-conductors, limits the voltage support performance, we propose a second solution for a better effectiveness. This involves introducing a second power source connected to the grid through an OLTC transformer, as illustrated in FIGURE 22.b. The power system is a 47 MVA synchronous power generating system (SPGS) with a 12 kV nominal voltage.

The obtained results, illustrated in FIGURE 24, show an improved voltage support capability and LVRT performance. Indeed, compared to the outcomes depicted in FIGURE 20 and FIGURE 23, the negative sequence of the voltage across the PCC has favorably decreased and the positive sequence has increased across all buses: the LV side, the PCC, and

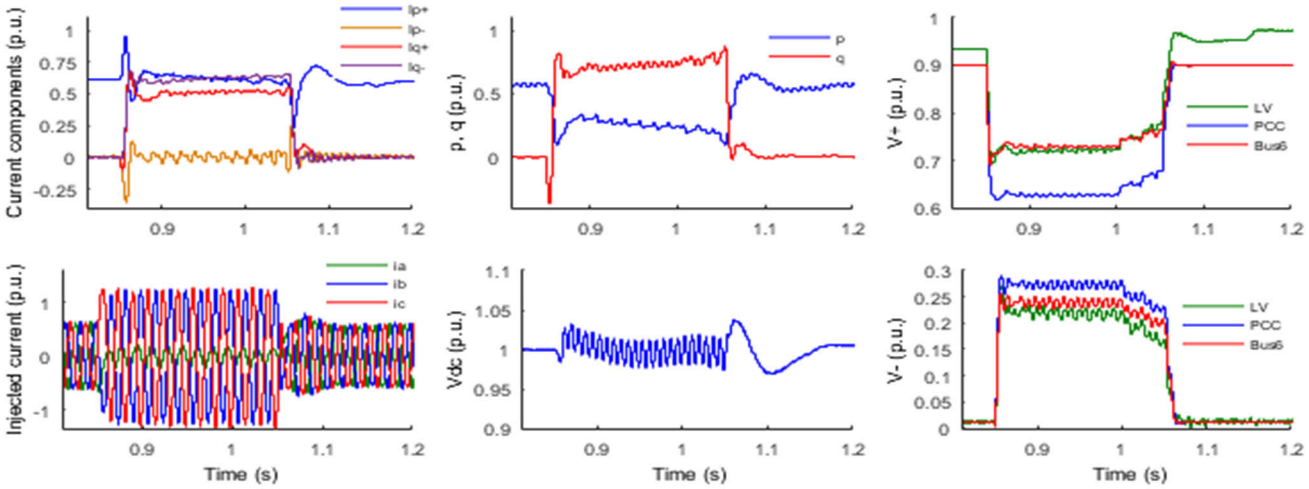

FIGURE 23. Simulation results with Strategy C under test case III after replacing transformer T1 by an OLTC transformer.

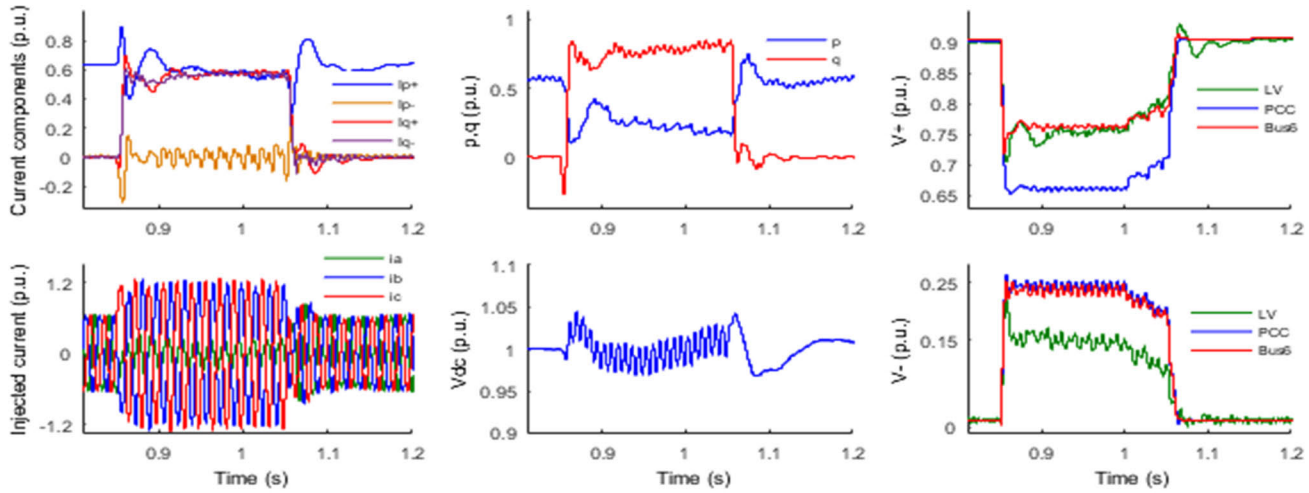

FIGURE 24. Simulation results with Strategy C under test case III after adding a SPGS linked to the PCC through an OLTC transformer.

bus 6. Additionally, DC-link stability and current quality are maintained.

Notice that simulations using the SPGS without an OLTC transformer revealed significant undervoltage across various levels during overload scenarios. This emphasizes the crucial role of var/voltage regulation equipment in maintaining voltage levels under frequent power loss conditions [73], [74], [75]. However, the effectiveness of var/voltage regulation equipment decreases under short-duration unbalanced voltage sags, requiring therefore additional solutions such as LVRT strategies. Different placements of OLTC transformers were explored, approving challenges in number and location [73], [74]. Literature suggests optimal placement near sensitive feeders suffering from voltage disturbances caused by power losses [70], [74].

In summary, LVRT strategies and var/voltage regulators complement each other for a robust power grid, addressing steady-state stability and transient disturbances. While var/volt regulation mitigates voltage variations, LVRT strategies focus on fast voltage sag events. Future research should explore the coordination between the two approaches for optimal performance.

B. DISCUSSIONS

The simulation outcomes highlighted the following challenges related to asymmetrical voltage sags:

1) The DC-bus voltage is affected by both RPO and IPO, making it crucial to address both.
2) The impact of NSAC on negative-sequence voltage is relatively minor compared to NSRC due to the grid predominantly inductive nature. However, the injection of NSAC tends to raise the negative-sequence voltage amplitude. Therefore, we recommend avoiding the injection of NSAC into the grid to enhance the DC-bus voltage quality and the voltage support performance.
3) Using static gain factors for reactive current references cannot provide optimal results due to the dynamic profile of the voltage sag, making it challenging to

select an appropriate static value. Therefore, the gain factors should be continuously updated throughout the whole fault and post-fault period to synchronize with the dynamic characteristics of the LVRT profile.

4) Imposing a range for gain factors, as mandated by FFCI, ensures a minimum effective injection of reactive current but could lead to overcurrent or affect the DC-bus voltage quality.
5) Effective voltage support hinges on the ratio of the injected power to base power. Higher injected power levels can significantly impact the PCC voltage, especially in mitigating voltage imbalance during deep voltage sags.
6) During transient responses, DC-link voltage and injected current amplitudes may exceed limits. These peaks can be reduced, and response times improved using advanced non-linear controllers. Control techniques avoiding the use of PWM modulator are also expected to provide a better dynamic response.
7) The synergy between LVRT strategy and var/voltage regulation equipment can enhance the resilience of the power system. However, it needs further investigation.

It can therefore be deduced that the flexible control of gain factors varying dynamically in terms of the instantaneous faulty voltage profile, surpasses the performance achieved with static values. This flexibility empowers the inverter to operate at its full capacity, enhancing its ability to provide a robust voltage support. This approach underscores the alignment of strategies B and C with the dynamic aspects of LVRT, showcasing their responsiveness to evolving conditions. Table 7 summarizes the obtained performances of the three proposed LVRT strategies under the test cases. The results affirm that Strategy C consistently ensures best LVRT performance in all scenarios, exhibiting superior stability compared to Strategies A and B.

Besides, Table 8 summarizes a comparative analysis of the proposed approach with existing control strategies for grid-connected inverters operating under asymmetrical voltage sags. The strategies developed in [19], [20], [21], [22], [23], [24] focus on the DC-bus voltage quality. However, they omit the concept of voltage support, which is a fundamental constraint in the LVRT requirements to avoid the disconnection from the grid. In [25], [26], [27], [28], the authors focus on the voltage support capability while considering only the overcurrent limitation, ignoring the DC-link voltage performance. In [28], though the reference of the RPO is set to zero, the DC-link voltage suffers from an important low-frequency ripple.

Compared to the existing research literature, the proposed work addresses simultaneously three LVRT constraints: the voltage support capability, overcurrent limitation, and the DC-link voltage quality. Indeed, through a flexible mitigation of RPO and IPO, the quality of the DC-link voltage is enhanced during the fault and post-fault operation. Moreover, current research addressing unbalanced grid voltage sag conditions frequently relies on power converters that incorporate LVRT or voltage support strategies without considering var/voltage regulation equipment. This equipment plays a crucial role in modern grid systems. They regulate voltage levels and manage reactive power, ensuring steady-state grid stability facing disturbances such as undervoltage resulting from power losses. Significantly, in their proposal, [75] introduced an LVRT strategy coupled with a STATCOM to uphold voltage levels during unbalanced voltage sag conditions. Unfortunately, the authors failed to consider symmetrical components decomposition, resulting in distorted currents that have the potential to reduce power quality and inhibit DC-link voltage performance.

TABLE 7. Resumed LVRT performance for proposed strategies.

Case	Strategy	A	B	C
I	DC-bus stability	yes for $k^+ < 5$	M	H
	Current limitation	yes	H	H
	LVRT	yes for $k^+ < 5$	M	H
II	DC-bus stability	yes for $k^- \leq 4$	L	H
	Current limitation	yes for $k^+ = 2$	P	M
	LVRT	yes for $k^+ = 2$	L	M
III	DC-bus stability	yes for $k^+ \leq 3$	M	H
	Current limitation	yes for $k^+ \leq 3$	M	M
	LVRT	yes for $k^+ \leq 3$	L	M

Performance: P: Poor, L: Low, M: Medium, H: High

TABLE 8. Resumed comparison study for the novelty of the proposed strategies.

Strategy	DC bus performance	Overcurrent limitation	Voltage-support
[20]	no	yes	no
[21]	no	yes	no
[22]	yes	yes	no
[23]	yes	yes	no
[24]	yes	yes	no
[25]	no	yes	yes
[26]	no	yes	yes
[27]	no	yes	yes
[28]	no	yes	yes
Proposal	yes	yes	yes

VII. CONCLUSION

In this paper, we addressed three primary objectives: first, identifying the appropriate current references for inverter-based generators to meet Low-Voltage-Ride-Through (LVRT) requirements; second, evaluating recent corresponding grid codes, and finally, offering recommendations for the development of future grid codes.

This work's primary innovation lies in concurrently tackling the voltage support capability, overcurrent protection, and enhancing the DC-link voltage performance. To achieve these goals, we addressed two additional constraints, related to the control of both real- and imaginary-power oscillations. Moreover, this study implies a concerted effort to integrate

grid code specifications, encompassing grid voltage support, through fast positive- and negative-sequence fault-current injection, and LVRT capability.

Additionally, this paper examines the performance of the PPM with LVRT strategy in conjunction with var/voltage regulation equipment, demonstrating promising results. Nevertheless, further investigation is needed to optimize the synergy and enhance the operation and performance of the power system.

Our key findings shed light on critical aspects of LVRT performance. We observed that effective LVRT capability during asymmetrical voltage sags requires flexible management of the gain factors controlling the current references. Additionally, among the proposed strategies, Strategy C, limiting both real- and imaginary-power oscillations, demonstrated superior and robust LVRT performance compared to Strategy A, based on static gain factors to develop current references, and Strategy B, focusing on nullifying the RPO.

Furthermore, although current grid codes may not currently stipulate specific requirements for eliminating the negative-sequence active current (NSAC), our research indicates that doing so can significantly enhance LVRT performance. This enhancement manifests in optimized voltage support, reduced power oscillations, and a robust DC-link voltage performance.

These findings offer crucial insights for future grid codes. In this context we propose two key adjustments: first, perform a fine-tuning of the fault-current gain factors' boundary to prioritize limiting the maximum amplitude of the injected current. Second, we recommend discouraging the injection of the NSAC. These modifications could significantly contribute to the development of more robust grid codes, enhancing the reliability and stability of power systems and promoting a secure transition towards sustainable energy.

APPENDIX A

This appendix provides a detailed exposition of the formulas (21), (22), (26) and (27) governing the oscillations in real and imaginary powers. By substituting (10) into (20) and (25), the explicit expressions of RPO and IPO can be derived as in (66) and (67), shown at the bottom of the page.

The voltage vectors expressed in the (α, β) frame are:

$$\boldsymbol{v}^{+}=\begin{bmatrix} V^{+}cos\left(\omega t+\theta^{+}\right) \\ V^{+}sin\left(\omega t+\theta^{+}\right) \end{bmatrix}, \boldsymbol{v}^{-}=\begin{bmatrix} V^{-}cos\left(\omega t+\theta^{-}\right) \\ -V^{-}sin\left(\omega t+\theta^{-}\right) \end{bmatrix} \tag{68}$$

Taking into account the phase shifts where $\boldsymbol{v}_{\perp}^{+}$ lags $\boldsymbol{v}^{+}$ by 90° and $\boldsymbol{v}_{\perp}^{-}$ leads $\boldsymbol{v}^{-}$ by 90°, we can compute the orthogonal voltage components using (69):

$$\boldsymbol{v}_{\perp}^{+,-}=\begin{bmatrix} 0 & 1 \\ -1 & 0 \end{bmatrix}\boldsymbol{v}^{+,-} \tag{69}$$

Equation (70) summarizes the expressions of the obtained vectors:

$$\boldsymbol{v}_{\perp}^{+}=\begin{bmatrix} V^{+}sin\left(\omega t+\theta^{+}\right) \\ -V^{+}cos\left(\omega t+\theta^{+}\right) \end{bmatrix}, \boldsymbol{v}_{\perp}^{-}=\begin{bmatrix} -V^{-}sin\left(\omega t+\theta^{-}\right) \\ -V^{-}cos\left(\omega t+\theta^{-}\right) \end{bmatrix} \tag{70}$$

Substituting (68) and (70) into (66) and (67), and performing vector products, yields:

$$\boldsymbol{v}^{-}\boldsymbol{v}^{+}=\boldsymbol{v}_{\perp}^{-}\boldsymbol{v}_{\perp}^{+}=V^{+}V^{-}cos\left(2\omega t+\theta^{+}+\theta^{-}\right) \tag{71}$$

$$\boldsymbol{v}^{-}\boldsymbol{v}_{\perp}^{+}=-\boldsymbol{v}^{+}\boldsymbol{v}_{\perp}^{-}=V^{+}V^{-}\sin\left(2\omega t+\theta^{+}+\theta^{-}\right) \tag{72}$$

APPENDIX B

This appendix provides a comprehensive overview of the parameters associated with the IEEE-9-bus used in this paper [50]. The IEEE-9-bus configuration includes three generators, transmission lines, and loads, all referenced to a base power of 100 MVA. The generators are situated at buses 1, 2, and 3, and their specifications are summarized in tables 9–11.

TABLE 9. Parameters of the IEEE-9-bus generators.

Bus	V [kV]	$S_{Short\text{-}circuit}$ [MVA]	P [MW]	Q [MVAR]
1	16.5	247.5	150	50
2	18	192	163	50
3	13.8	128	85	8

TABLE 10. Parameters of the IEEE-9-bus transmission lines.

Line		Length [km]	resistance [Ω/km]	inductance [H/km]	capacitance [F/km]
From Bus	To Bus				
4	5	100	0.0529	1.192e-3	8.82e-9
4	6	100	0.08993	1.29e-3	7.922e-9
5	7	100	0.16928	2.259e-3	15.34e-9
6	9	100	0.20631	2.38e-3	17.95e-9
7	8	100	0.044965	1.01e-3	7.471e-9
8	9	100	0.062951	1.414e-3	10.47e-9

$$\tilde{p}=\frac{3}{2}\left[\left(V^{-}I_{p}^{+}-V^{+}I_{p}^{-}\right)\frac{v^{-}v^{+}}{V^{+}V^{-}}+\left(V^{-}I_{q}^{+}-V^{+}I_{q}^{-}\right)\frac{v^{-}v_{\perp}^{+}}{V^{-}V^{+}}\right] \tag{66}$$

$$\tilde{q}=\frac{3}{2}\left[\left(V^{-}I_{p}^{+}+V^{+}I_{p}^{-}\right)\frac{v^{+}v_{\perp}^{-}}{V^{+}V^{-}}+\left(V^{-}I_{q}^{+}+V^{+}I_{q}^{-}\right)\frac{v_{\perp}^{-}v_{\perp}^{+}}{V^{-}V^{+}}\right] \tag{67}$$

TABLE 11. Parameters of the IEEE-9-bus loads.

Bus	V [kV]	P [MW]	Q [MVAR]
5	230	100	40
6	230	102	10
8	230	100	30

REFERENCES

[1] IEA (International Energy Agency). (2021). *Net Zero by 2050 a Roadmap for the Global Energy Sector*. [Online]. Available: https://www.iea.org/reports/net-zero-by-2050

[2] IRENA. (2018). *Global Energy Transformation: A Roadmap to 2050*. [Online]. Available: https://www.irena.org/publications/2018/Apr/Global-Energy-Transition-A-Roadmap-to-2050

[3] G. Amanatidis. (Jan. 2019). *European Policies on Climate and Energy Towards 2020, 2030 and 2050*. Policy Dept. Econ., Sci. Quality Life Policies. [Online]. Available: https://www.europarl.europa.eu/RegData/etudes/BRIE/2019/631047/IPOL_BRI

[4] M. H. J. Bollen, *Understanding Power Quality Problems: Voltage Sags and Interruptions*. New York, NY, USA: IEEE Press Series on Power Engineering, 2000, doi: 10.1109/9780470546840.

[5] Y. Han, Y. Feng, P. Yang, L. Xu, Y. Xu, and F. Blaabjerg, "Cause, classification of voltage sag, and voltage sag emulators and applications: A comprehensive overview," *IEEE Access*, vol. 8, pp. 1922–1934, 2020.

[6] J. Beyza and J. M. Yusta, "The effects of the high penetration of renewable energies on the reliability and vulnerability of interconnected electric power systems," *Rel. Eng. Syst. Saf.*, vol. 215, Nov. 2021, Art. no. 107881.

[7] E. A. Feilat, S. Azzam, and A. Al-Salaymeh, "Impact of large PV and wind power plants on voltage and frequency stability of Jordan's national grid," *Sustain. Cities Soc.*, vol. 36, pp. 257–271, Jan. 2018.

[8] M. A. Jarrahi, H. Samet, and T. Ghanbari, "Novel change detection and fault classification scheme for AC microgrids," *IEEE Syst. J.*, vol. 14, no. 3, pp. 3987–3998, Sep. 2020.

[9] M. Hamdi and M. Hamouda, "A short review of grid voltage sags and current control techniques of voltage source inverters in distributed power generation systems," in *Renewable Energy Production and Distribution*, vol. 1. New York, NY, USA: Academic, 2022, ch. 12, pp. 415–445, doi: 10.1016/B978-0-323-91892-3.00012-1.

[10] *IEEE Standard for Interconnecting Distributed Resources With Electric Power Systems*, Standards IEEE 1547-2003, IEEE-SA Standards Board, Sep. 2008.

[11] A. Cabrera-Tobar, E. Bullich-Massagué, M. Aragüés-Peñalba, and O. Gomis-Bellmunt, "Review of advanced grid requirements for the integration of large scale photovoltaic power plants in the transmission system," *Renew. Sustain. Energy Rev.*, vol. 62, pp. 971–987, Sep. 2016.

[12] F. Letaief, M. Hamouda, and K. Al-Haddad, "Review and discussion of recent codes for inverter-based RESs and PPMs under grid voltage sag conditions," in *Proc. IEEE Int. Conf. Artif. Intell. Green Energy (ICAIGE)*, Sousse, Tunisia, Oct. 2023, pp. 1–6, doi: 10.1109/ICAIGE58321.2023.10346391.

[13] M. Mohseni and S. M. Islam, "Review of international grid codes for wind power integration: Diversity, technology and a case for global standard," *Renew. Sustain. Energy Rev.*, vol. 16, no. 6, pp. 3876–3890, Aug. 2012.

[14] R. Bründlinger, "Grid codes in Europe: Overview on the current requirements in European codes and national interconnection standards," in *Proc. NEDO/IEA PVPS Task 14th Workshop*, Nov. 2019, pp. 1–32.

[15] M. Ali et al., "Implementation of the network code on requirements for grid connection of generators," Eur. Commission, Directorate-Gen. Energy, Publications Office Eur. Union, Luxembourg, U.K., Final Rep., 2021, doi: 10.2833/610006.

[16] *Network Code on Requirements for Grid Connection of Generators*, document 2016/631, Commission Regulation (EU), Apr. 2016.

[17] *Technical Specification: Distributed Energy Resources Connection With the Grid*, Standard IEC/TS 62786, Int. Electrotech. Commission, Apr. 2017.

[18] M. Hamouda, H. F. Blanchette, and K. Al-Haddad, "Unity power factor operation of indirect matrix converter tied to unbalanced grid," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1095–1107, Feb. 2016, doi: 10.1109/TPEL.2015.2421480.

[19] F. Wang, J. L. Duarte, and M. A. M. Hendrix, "Pliant active and reactive power control for grid-interactive converters under unbalanced voltage dips," *IEEE Trans. Power Electron.*, vol. 26, no. 5, pp. 1511–1521, May 2011, doi: 10.1109/TPEL.2010.2052289.

[20] J. Marchgraber and W. Gawlik, "Dynamic voltage support of converters during grid faults in accordance with national grid code requirements," *Energies*, vol. 13, no. 10, p. 2484, May 2020, doi: 10.3390/en13102484.

[21] D. Çelik and M. E. Meral, "A novel control strategy for grid connected distributed generation system to maximize power delivery capability," *Energy*, vol. 186, Nov. 2019, Art. no. 115850, doi: 10.1016/j.energy.2019.115850.

[22] M. E. Meral and D. Çelik, "Mitigation of DC-link voltage oscillations to reduce size of DC-side capacitor and improve lifetime of power converter," *Electr. Power Syst. Res.*, vol. 194, May 2021, Art. no. 107048.

[23] M. Bajaj, A. Flah, M. Alowaidi, N. Kumar Sharma, S. Mishra, and S. K. Sharma, "A Lyapunov-function based controller for 3-phase shunt active power filter and performance assessment considering different system scenarios," *IEEE Access*, vol. 9, pp. 66079–66102, 2021, doi: 10.1109/ACCESS.2021.3075274.

[24] H. Ahmed and D. Çelik, "Sliding mode based adaptive linear neuron proportional resonant control of Vienna rectifier for performance improvement of electric vehicle charging system," *J. Power Sources*, vol. 542, Sep. 2022, Art. no. 231788, doi: 10.1016/j.jpowsour.2022.231788.

[25] A. Camacho, M. Castilla, J. Miret, L. G. de Vicuña, and R. Guzman, "Positive and negative sequence control strategies to maximize the voltage support in resistive-inductive grids during grid faults," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 5362–5373, Jun. 2018, doi: 10.1109/TPEL.2017.2732452.

[26] M. Garnica, L. G. de Vicuña, J. Miret, M. Castilla, and R. Guzmán, "Optimal voltage-support control for distributed generation inverters in RL grid-faulty networks," *IEEE Trans. Ind. Electron.*, vol. 67, no. 10, pp. 8405–8415, Oct. 2020.

[27] I. Todorović, I. Isakov, S. Grabić, and V. Porobić, "Unbalanced voltages mitigation using the maximized and flexible grid-connected inverter voltage support functionality," *Electr. Power Syst. Res.*, vol. 192, Mar. 2021, Art. no. 106926.

[28] L. Ji, J. Shi, Q. Hong, Y. Fu, X. Chang, Z. Cao, Y. Mi, Z. Li, and C. Booth, "A multi-objective control strategy for three phase grid-connected inverter during unbalanced voltage sag," *IEEE Trans. Power Del.*, vol. 36, no. 4, pp. 2490–2500, Aug. 2021.

[29] F. Letaief, A. B. Rhouma, and M. Hamouda, "Flexible control strategies with current limitation of VSI under unbalanced grid voltage sags," in *Proc. 18th Int. Multi-Conf. Syst., Signals Devices (SSD)*, Monastir, Tunisia, Mar. 2021, pp. 1–6, doi: 10.1109/SSD52085.2021.9429489.

[30] R. M. Silva, A. F. Cupertino, G. M. Rezende, C. V. Sousa, and V. F. Mendes, "Power control strategies for grid connected converters applied to full-scale wind energy conversion systems during LVRT operation," *Electr. Power Syst. Res.*, vol. 184, Jul. 2020, Art. no. 106279, doi: 10.1016/j.epsr.2020.106279.

[31] A. F. Cupertino, L. S. Xavier, E. M. S. Brito, V. F. Mendes, and H. A. Pereira, "Benchmarking of power control strategies for photovoltaic systems under unbalanced conditions," *Int. J. Electr. Power Energy Syst.*, vol. 106, pp. 335–345, Mar. 2019, doi: 10.1016/j.ijepes.2018.10.014.

[32] J. Joshi, A. K. Swami, V. Jately, and B. Azzopardi, "A comprehensive review of control strategies to overcome challenges during LVRT in PV systems," *IEEE Access*, vol. 9, pp. 121804–121834, 2021, doi: 10.1109/ACCESS.2021.3109050.

[33] A. Klajn and M. Bątkiewicz-Pantuła, *Voltage Characteristics of Electricity Supplied by Public Electricity Networks*, Standard EN 50160, Eur. Copper Inst., Brussels, Belgium, 2017.

[34] M. H. J. Bollen and L. D. Zhang, "Different methods for classification of three-phase unbalanced voltage dips due to faults," *Electr. Power Syst. Res.*, vol. 66, no. 1, pp. 59–69, Jul. 2003.

[35] *Annex 1 to Guide for Connection of Power-Generating Plants to the Low Voltage Grid (≤1 KV)*, document Version 1.3, Green Power Denmark, 2022.

[36] *Requirements for Generating Plants to Be Connected in Parallel With Distribution Networks—Part 1: Connection To a LV Distribution Network—Generating Plants up to and Including Type B*, document EN 50549-1, 2019.

[37] *Requirements for Generating Plants to be Connected in Parallel With Distribution Networks—Part 2: Connection to a MV Distribution Network. Generating Plants up to and Including Type B*, document EN 50549-2, 2019.

[38] *Technical and Organisational Rules TOR Generator Type A: Connection and Parallel Operation of Type A Power Generation Installations and Micro-Generation, TOR Erzeuger Typ A*, document Version 1.2, E-Control, Vienna, Austria, 2019.

[39] *Technical and Organisational Rules TOR Generator Type B: Connection and Parallel Operation of Type B Power Generation Plants, TOR Erzeuger Type B*, document Version 1.2, E-Control, Vienna, Austria, 2019.
[40] *Technical Connection Rules for Medium-Voltage*, document VDE-AR-N 4110, VDE FNN, Berlin, Germany, 2018.
[41] *Technical Connection Rules for High-Voltage*, document VDE-AR-N 4120, VDE FNN, Berlin, Germany, 2018.
[42] *Requirements for Connection of Power-Generating Modules to the Public Service Grid*, document 73, Mar. 2020.
[43] *Requirements for Grid Connection of Type A, B, C and D Electricity Generation Facilities*, document ILR/E18/43, Luxembourg Regulatory Inst., 2018.
[44] *Annex 3 to Guide for Connection of Power-Generating Plants to the Medium and High-Voltage Grid (>1 kV)*, document Version 1.2, Green Power Denmark, 2022.
[45] *The Grid Codes*, ESO Nat. Grid Electr. Syst. Operator, Great Britain, U.K., 2023.
[46] *RFG Compliance Verification Power Generating Modules Type B, C and D*, document Version 1.4, Netbeheer Nederland, Amsterdam, The Netherlands, 2022.
[47] *Technical Requirements for the Connection to the Network Necessary for the Implementation of the Codes of Network of Connection*, document BOE-A-2020-8965, Ministry Ecol. Transition Demographic Challenge, Madrid, Spain, 2020.
[48] *The Requirements for the Connection of Generators to the Electricity Grid*, document O3E-323, State Energy Regulatory Council, Vilnius, Lithuania, 2018.
[49] *Rules for the Parallel Operation of Generating and Storage Facilities With the Network of the Distribution System Operator*, Energy Regulatory Office, Distrib. Syst. Operators, Czechia, U.K., 2018.
[50] J. Pettikkattil. (2023). *MATLAB Central File Exchange*. Accessed: Aug. 18, 2023. [Online]. Available: https://www.mathworks.com/matlabcentral/fileexchange/45936-ieee-9-bus
[51] R. C. Dugan, M. F. McGranaghan, S. Santoso, and H. W. Beaty, *Electrical Power Systems Quality*, 3rd ed. New York, NY, USA: McGraw-Hill, 2012.
[52] P. Giroux. (2023). *Grid-Connected PV Array, MATLAB Central File Exchange*. Accessed: Aug. 18, 2023. [Online]. Available: https://www.mathworks.com/matlabcentral/fileexchange/34752-grid-connected-pv-array
[53] O. Hebala. (2023). *Battery Charging/Discharging Controller, MATLAB Central File Exchange*. Accessed: Aug. 18, 2023. [Online]. Available: https://www.mathworks.com/matlabcentral/fileexchange/91750-battery-charging-discharging-controller
[54] G. C. Paap, "Symmetrical components in the time domain and their application to power network calculations," *IEEE Trans. Power Syst.*, vol. 15, no. 2, pp. 522–528, May 2000, doi: 10.1109/59.867135.
[55] F. Wang, J. L. Duarte, and M. A. M. Hendrix, "Design and analysis of active power control strategies for distributed generation inverters under unbalanced grid faults," *IET Gener., Transmiss. Distrib.*, vol. 4, no. 8, p. 905, Aug. 2010, doi: 10.1049/iet-gtd.2009.0607.
[56] Y. Yang, K. A. Kim, F. Blaabjerg, and A. Sangwongwanich, *Advances in Grid-Connected Photovoltaic Power Conversion Systems*. Sawston, U.K.: Woodhead Publishing, 2018.
[57] D.-L. Popa, M.-S. Nicolae, P.-M. Nicolae, and M. Popescu, "Design and simulation of a 10 MW photovoltaic power plant using MATLAB and simulink," in *Proc. IEEE Int. Power Electron. Motion Control Conf. (PEMC)*, Varna, Bulgaria, Sep. 2016, pp. 378–383, doi: 10.1109/EPEPEMC.2016.7752027.
[58] U. C. Nwaneto and A. M. Knight, "Full-order and simplified dynamic phasor models of a single-phase two-stage grid-connected PV system," *IEEE Access*, vol. 11, pp. 26712–26728, 2023, doi: 10.1109/ACCESS.2023.3257164.
[59] V. Badescu, "Dynamic model of a complex system including PV cells, electric battery, electrical motor and water pump," *Energy*, vol. 28, no. 12, pp. 1165–1181, Oct. 2003, doi: 10.1016/s0360-5442(03)00115-4.
[60] S. Mishra, I. Hussain, B. Singh, A. Chandra, K. Al-Haddad, and P. Shah, "Frequency adaptive prefiltering stage for differentiation-based control of shunt active filter under polluted grid conditions," *IEEE Trans. Ind. Appl.*, vol. 55, no. 1, pp. 882–891, Jan. 2019, doi: 10.1109/TIA.2018.2866456.
[61] E. Akin and M. E. Şahın, "Investigation of incremental conductance MPPT algorithm in MATLAB/simulink using photovoltaic powered DC–DC boost converter," in *Proc. 22nd Int. Symp. Power Electron. (Ee)*, Novi Sad, Serbia, Oct. 2023, pp. 1–6, doi: 10.1109/ee59906.2023.10346089.
[62] M. H. Ibrahim, S. P. Ang, M. N. Dani, M. I. Rahman, R. Petra, and S. M. Sulthan, "Optimizing step-size of perturb & observe and incremental conductance MPPT techniques using PSO for grid-tied PV system," *IEEE Access*, vol. 11, pp. 13079–13090, 2023, doi: 10.1109/ACCESS.2023.3242979.
[63] G. Vacheva, V. Dimitrov, and N. Hinov, "Modelling and control of bidirectional buck-boost converter for electric vehicles applications," in *Proc. 16th Conf. Electr. Mach., Drives Power Syst. (ELMA)*, Varna, Bulgaria, Jun. 2019, pp. 1–4, doi: 10.1109/ELMA.2019.8771496.
[64] M. Alramlawi and P. Li, "Design optimization of a residential PV-battery microgrid with a detailed battery lifetime estimation model," *IEEE Trans. Ind. Appl.*, vol. 56, no. 2, pp. 2020–2030, Mar. 2020, doi: 10.1109/TIA.2020.2965894.
[65] I. A. Azzollini, V. D. Felice, F. Fraboni, L. Cavallucci, M. Breschi, A. D. Rosa, and G. Zini, "Lead-acid battery modeling over full state of charge and discharge range," *IEEE Trans. Power Syst.*, vol. 33, no. 6, pp. 6422–6429, Nov. 2018, doi: 10.1109/TPWRS.2018.2850049.
[66] M. Mellouli, M. Hamouda, J. B. H. Slama, and K. Al-Haddad, "A third-order MAF based QT1-PLL that is robust against harmonically distorted grid voltage with frequency deviation," *IEEE Trans. Energy Convers.*, vol. 36, no. 3, pp. 1600–1613, Sep. 2021, doi: 10.1109/TEC.2021.3061027.
[67] P. Xiao, K. A. Corzine, and G. K. Venayagamoorthy, "Multiple reference frame-based control of three-phase PWM boost rectifiers under unbalanced and distorted input conditions," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 2006–2017, Jul. 2008, doi: 10.1109/TPEL.2008.925205.
[68] H.-S. Song and K. Nam, "Dual current control scheme for PWM converter under unbalanced input voltage conditions," *IEEE Trans. Ind. Electron.*, vol. 46, no. 5, pp. 953–959, Oct. 1999, doi: 10.1109/41.793344.
[69] E. T. Jauch, "Volt/Var management? An essential 'SMART' function," in *Proc. IEEE/PES Power Syst. Conf. Expo.*, Seattle, WA, USA, Mar. 2009, pp. 1–7, doi: 10.1109/PSCE.2009.4840018.
[70] S. Rahimi, M. Marinelli, and F. Silvestro, "Evaluation of requirements for Volt/Var control and optimization function in distribution management systems," in *Proc. IEEE Int. Energy Conf. Exhib. (ENERGYCON)*, Florence, Italy, Sep. 2012, pp. 331–336, doi: 10.1109/ENERGYCON.2012.6347777.
[71] M. Tahir, M. E. Nassar, R. El-Shatshat, and M. M. A. Salama, "A review of Volt/Var control techniques in passive and active power distribution networks," in *Proc. IEEE Smart Energy Grid Eng. (SEGE)*, Oshawa, ON, Canada, Aug. 2016, pp. 57–63, doi: 10.1109/SEGE.2016.7589500.
[72] P. Brunelle. (2024). *Three-Phase On-Line Tap Changing Regulating Transformer, MATLAB Central File Exchange*. Accessed: Feb. 17, 2024. [Online]. Available: https://www.mathworks.com/matlabcentral/fileexchange/33375-three-phase-on-line-tap-changing-regulating-transforme
[73] E. T. Jauch, "Smart grid Volt/Var management: Challenges of integrating distribution DG," in *Proc. IEEE PES Innov. Smart Grid Technol. (ISGT)*, Washington, DC, USA, Jan. 2012, pp. 1–5, doi: 10.1109/ISGT.2012.6175775.
[74] H. Sun, Q. Guo, J. Qi, V. Ajjarapu, R. Bravo, J. Chow, Z. Li, R. Moghe, E. Nasr-Azadani, U. Tamrakar, G. N. Taranto, R. Tonkoski, G. Valverde, Q. Wu, and G. Yang, "Review of challenges and research opportunities for voltage control in smart grids," *IEEE Trans. Power Syst.*, vol. 34, no. 4, pp. 2790–2801, Jul. 2019, doi: 10.1109/TPWRS.2019.2897948.
[75] O. Alrumayh, K. Sayed, and A. Almutairi, "LVRT and reactive power/voltage support of utility-scale PV power plants during disturbance conditions," *Energies*, vol. 16, no. 7, p. 3245, Apr. 2023, doi: 10.3390/en16073245.

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