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Real-Time Implementation of Three-Phase Z Packed U-Cell Modular Multilevel Grid-Connected Converter Using CPU and FPGA

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Abstract: The Modular Multilevel Converter (MMC) is a promising converter for medium-/high voltage applications due to its various features. The waveform quality could be enhanced further by expanding the number of generated voltage levels, which increases the number of submodules (SMs); however, this improvement enlarges the size and cost of the converter, posing a persistent challenge. Hence, there exists a trade-off between power quality and the size and complexity of the converter. To verify the performance of such a complex converter and to validate the effectiveness of the control system, especially in the absence of a physical system, Real-Time (RT) simulation becomes crucial. However, the large number of components of a MMC creates important numerical challenges and computational difficulties in RT simulation. This paper proposes a grid-connected MMC employing a Z Packed U-Cell converter as a SM to generate a higher number of voltage levels while minimizing the required number of SMs. The ZPUC-MMC is implemented on an FPGA-based RT simulation platform using Electric Hardware Solver to reduce computational burden and simulation time, while improving the accuracy of the obtained results. Conventional controllers of MMCs are applied to assess the effectiveness and robustness of the proposed system during steady-state and dynamic operations.

Keywords: Modular Multilevel Converter; Z Packed U-Cell Converter; grid-connected converter; decoupled *dq* control; energy sorting and voltage balancing; circulating current control; real-time simulation; CPU; FPGA; electric hardware solver

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1. Introduction

Nowadays, Real-Time (RT) simulation is widely employed in power electronics research field to validate proposed topologies, control, and modulation methods. Moreover, it is recognized by the industry as a functional tool for the development of power electronics devices and systems, offering a substantial reduction in the time needed to create hardware prototypes [1,2]. RT simulation offers immense flexibility and scalability for testing novel concepts, enabling users to validate control system designs even in the absence of a physical plant, particularly when dealing with complex and challenging converter topologies such as the Modular Multilevel Converter (MMC). In addition, identifying and rectifying errors at the simulation stage significantly mitigates the risk of high-cost corrective methods after hardware prototyping [2].

MMCs are widely used in medium-/high voltage applications due to their various features such as low dv/dt, low switching frequency, modularity structure, high-quality output waveforms, reduced AC filter size, flexible scalability to higher power and voltage levels, and a lower expense for redundancy. However, all of these advantages are accompanied by several challenges when it comes to the design and control that are quite complex and depend on various factors, including the number of SM per arm and desired number

of voltage levels [3–5]. Diverse SM configurations have been suggested for the MMC such as the Half-Bridge (HB) [6], Unidirectional cell (U) [7], Full-Bridge (FB) [6], Clamped Double (CD) [8], 3L-Neutral Point Clamp (3L-NPC) [9], 3L-Flying Capacitor (3L-FC) [10], 5L-Cross Connected Cell (5L-CCC) [11], 7L-Packed U-Cell Converter (7L-PUC) [12], and 5L-Z Packed U-Cell Converter (5L-ZPUC) [13–15]. Classification is based on the polarity of SM (uni-/bipolar), number of components within the SM, voltage levels generated per arm by a single SM, and capability for handling a DC fault (DFH) [4,9]. Table 1 presents an overview of various SM configurations outlined in the literature, assessing them based on their component count and the voltage levels they produce. It is evident that employing a multilevel SM topology enhances the quantity of generated voltage levels within each arm [3–5,9,16].

Table 1. Different SM topologies and arm voltage levels.

SM Type	Hardware Perspective			Control Perspective	
SM	**C**	**IGBT**	**Diodes**	**Arm Voltage Levels**	**Multilevel**
HB	N	2*N	2*N	N	NO
U	N	N	2*N	N	NO
FB	N	4*N	4*N	N	NO
CD	2*N	5*N	7*N	3*N	YES
3L-NPC	2*N	4*N	6*N	3*N	YES
3L-FC	2*N	4*N	4*N	3*N	YES
5L-CCC	2*N	6*N	6*N	5*N	YES
7L-PUC	2*N	6*N	6*N	7*N	YES
5L-ZPUC	3*N	6*N	6*N	4*N+1	YES

The large number of components and the non-linear devices in a MMC create important numerical challenges and computational difficulties, which become more complex in RT simulation [17–19]. The RT simulation of a MMC could be implemented on various platforms, including the central processing unit (CPU) and the field-programmable gate array (FPGA). CPU-based RT simulation provides flexibility and ease of implementation, but may encounter challenges in achieving high simulation accuracy due to longer execution times for each node. The computational load on a CPU can restrict the RT simulation capability, especially for detailed-/large-scale systems like MMCs. The processing time per node, often in the range of tens of microseconds, might limit the simulation's fidelity, impacting the accuracy of transient responses [17,20]. Another alternative is provided using FPGA technology, which is particularly well-suited for complex power electronics converter models. FPGA-based RT simulation significantly decreases the simulation time to hundreds of nanoseconds and reduces the latency of the simulated electric power system under test, resulting in higher simulation accuracy [18,21].

Aiming at these problems, this paper is devoted to proposing a three-phase ZPUC-MMC for grid-connected applications which was not presented before, and to adapting the converter model and its control to real-time implementation tools, including eHS with FPGA execution to validate the performance of the proposed topology. The proposed approach offers several advantages in terms of generating a higher number of voltage levels with a reduced number of SMs and a reduced number of components when it is compared to other SM topologies like the HB-MMC [6,13,14]. High-quality output waveforms are obtained with a reduced harmonics content which reduces the size of the grid-side filters. Moreover, the voltage balancing (VB), and energy sorting (ES) algorithms are fully integrated into the Phase-Shift Pulse Width Modulation (PS-PWM), eliminating the need for supplementary control. Due to the complexity of a MMC structure and to the limited availability of a small prototype, RT simulation is used to validate the performance of the proposed converter while using conventional MMC controllers. The CPU-based RT simulation of a ZPUC-MMC presents challenges, particularly as the number of ZPUC-SM

per arm increases. This leads to a substantial increase in CPU load, resulting in overruns and loss of the RT status of the simulation. Although extending the simulation time can reduce overruns, it may compromise the accuracy of the results obtained. Therefore, to overcome limitations encountered in CPU-based RT simulation, FPGA-based RT simulation is employed in this study. A three-phase ZPUC-MMC is implemented using an OPAL-RT Target (OP4510) and Electric Hardware Solver (eHS), which increases the simulation speed, decreases the time-step, and improves the results accuracy. The paper is divided as follows: in Section 2, the proposed three-phase ZPUC-MMC is described, and in Section 3 the modeling and the adopted control system are covered. Section 4 presents the FPGA-based RT implementation of a ZPUC-MMC grid-connected converter using RT-LAB, and an OP4510 Target with eHS. In Section 5, RT simulation results are analyzed and discussed under different modes of operations followed by a summary of the study in the conclusion.

2. Proposed Three-Phase Z Packed U-Cell Modular Multilevel Converter

2.1. ZPUC Submodule in MMC Configuration

ZPUC-MMC, illustrated in Figure 1, is a MMC based on a ZPUC converter for its SM. ZPUC was initially proposed as an inverter for single-/three phase applications and as a submodule (SM) for MMC applications. It features the use of a single DC source in single-/three-phase applications. It is composed of six switches and three floating capacitors; S_1, S_3, and S_5, operate in complement manner with S_2, S_4, and S_6, respectively, thus $2^3 = 8$ switching states exist. It is crucial to ensure that the capacitors' voltages remain balanced. Based on their regulated values, either a seven-level (7L-) or five-level (5L-) output voltage can be achieved. In this study, the 5L-ZPUC configuration is chosen due to its redundant switching states (refer to Table 2), eliminating the need for an extra controller to balance the flying capacitors, as required in the case of 7L-ZPUC. The VB for ZPUC capacitors is fully incorporated within the PS-PWM. To achieve 5L-output across the ZPUC output, the capacitor voltages must be configured according to Equation (1): the voltages of capacitors C_1 and C_2 need to be maintained at $2E$, and the voltage of capacitor C_3 should be held at E. $2E$ is defined as the total DC voltage applied across ZPUC-SM ($V_{dc,ZPUC}$) [13]. The proposed grid-tied ZPUC-MMC converter, as depicted in Figure 1, is composed of three legs, each comprising an upper arm and a lower arm. The number of ZPUC-SM per arm is designated as N, while per leg is indicated by n. The upper and lower arm voltages are composed of $4N + 1$ levels ranging from zero to$4N$E in E steps, where $4N$E is the total DC link voltage, V_{dc} (DC source applied to the MMC). The phase voltages consist of M_{phase} levels spanning from $-2N$E ($-V_{dc}/2$) to $2N$E ($V_{dc}/2$) in increments of $E/2$ as in Equation (2), and the line-to-line voltages are comprised of M_{line} levels distributed between $-4N$E and $4N$E in increments of $E/4$ steps as Equation (3). Within the ZPUC-MMC configuration, the total DC link voltage (V_{dc}) is evenly distributed, with half allocated to both the upper and lower arms ($0.5V_{dc}$ each). This reduces the voltage of each submodule in each arm and results in reducing the switching stresses. However, with other conventional SM topologies such as HB-SM, the total DC link voltage (V_{dc}) is applied to both the upper and lower arm [13,14].

$$V_{c1} = V_{c2} = 2E, V_{c3} = E, \tag{1}$$

$$M_{phase} = 8N + 1, \tag{2}$$

$$M_{line} = 16N + 1, \tag{3}$$

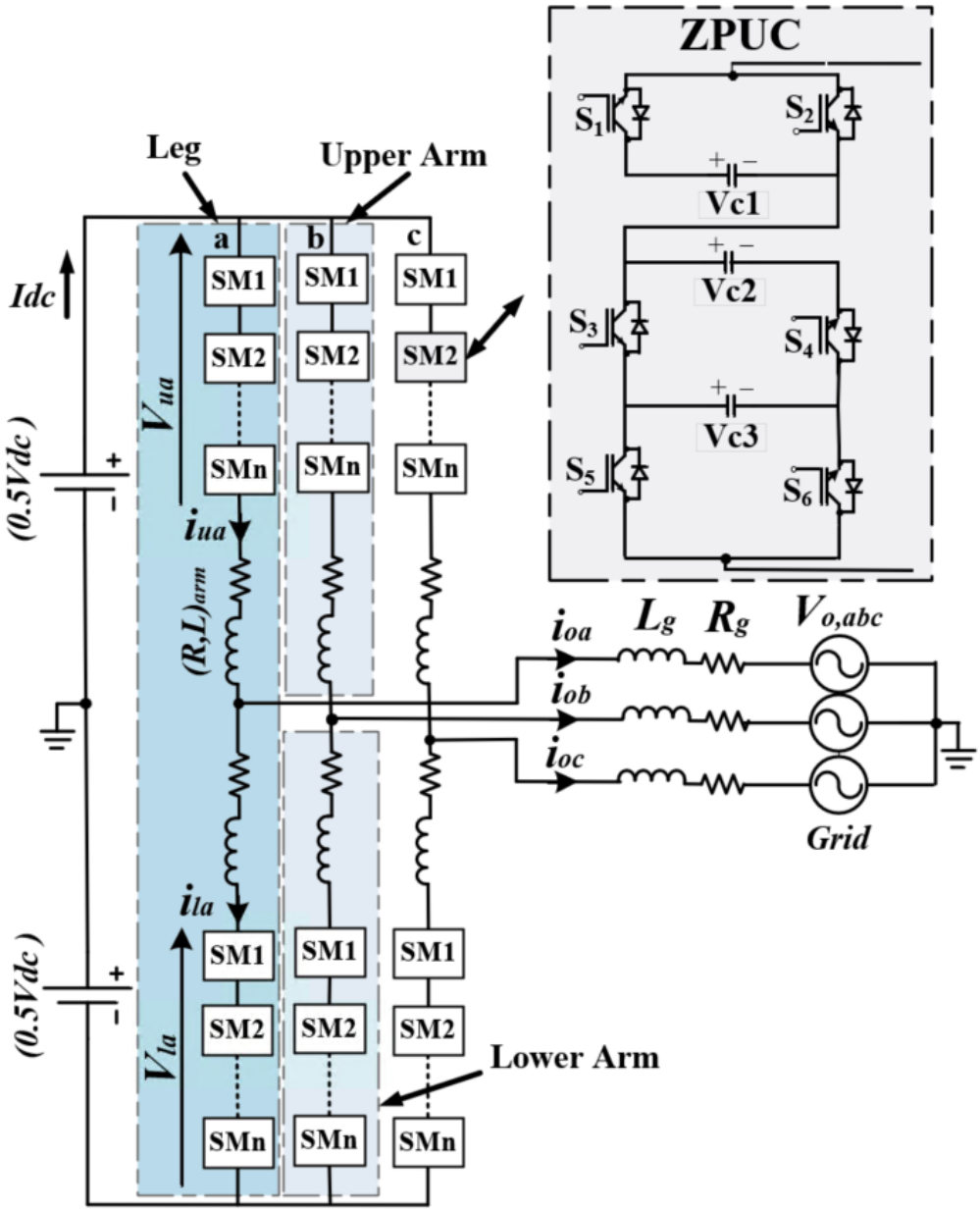


Figure 1. Proposed three-phase ZPUC-MMC grid-connected converter.

Table 2. Switching states of the 5L-ZPUC.

States	S_1 S_3 S_5	V_{zpuc}	V_{zpuc} (5L)
1	1 0 0	$V_{c1} + V_{c2}$	4E
2	1 0 1	$V_{c1} + V_{c2} - V_{c3}$	3E
3	1 1 0	$V_{c1} + V_{c3}$	3E
4	1 1 1	V_{c1}	2E
5	0 0 0	V_{c2}	2E
6	0 0 1	$V_{c2} - V_{c3}$	E
7	0 1 0	V_{c3}	E
8	0 1 1	0	0

2.2. 9L-ZPUC-MMC for Grid-Connected Applications

In the proposed converter within this work, one ZPUC-SM is used in each arm ($N = 1$), resulting in a total of 2 ZPUC-SM per leg ($n = 2$). Upper and lower arm voltages consist of 5L-($4N + 1$), and phase voltages comprise 9L-($8N + 1$). In this paper, the PS-PWM is chosen for its numerous advantages, including uniform distribution of losses across all semiconductor switches and reduced THD. Additionally, the PS-PWM displaces harmonics further from the fundamental frequency, and enhances the speed of integrated VB for auxiliary capacitors [22]. In the PS-PWM, $L - 1$ carriers are needed; where L is the number of generated voltage levels. These carriers should be phase-shifted by an angle of $(360 / L - 1)°$ [13]. Therefore, one sinusoidal reference voltage and four carriers are required to generate 5L- at the output of a single ZPUC-SM. Also, upper arm carriers are phase shifted by an angle of $(360/4)°$ and are positioned at 0°, 90°, 180°, 270°. Lower arm carriers are offset from those in the upper arm by a 180° angle, resulting in their placement at 45°, 135°, 225°, and 315° [13]. The carriers in both the upper and lower arms, alongside the voltage reference are depicted in Figure 2. The VB algorithm ensures energy balance between the upper and lower ZPUC-SM in each phase, as well as balancing the flying capacitors. This is facilitated by the redundant switching states (refer to Table 2), which produce 3E, 2E, and E voltage levels. Initially, the PS-PWM method of [22] is employed to create the various voltage levels. Subsequently, the choice between redundant switching states relies on the direction of the arm current and the voltages across the capacitors. Further information regarding the incorporation of the VB algorithm within the PS-PMW, and criteria concerning arm currents direction and capacitor voltages is detailed in [13]. When employing multiple ZPUC-SMs per arm, both energy sorting and VB algorithms are incorporated into the PS-PWM to guarantee equilibrium of energy distribution among various ZPUC-SM within a single arm and between ZPUC-SMs of upper and lower arms. Comprehensive descriptions of ES and VB algorithms when two ZPUC-SM/arm are used is detailed in [13,15].

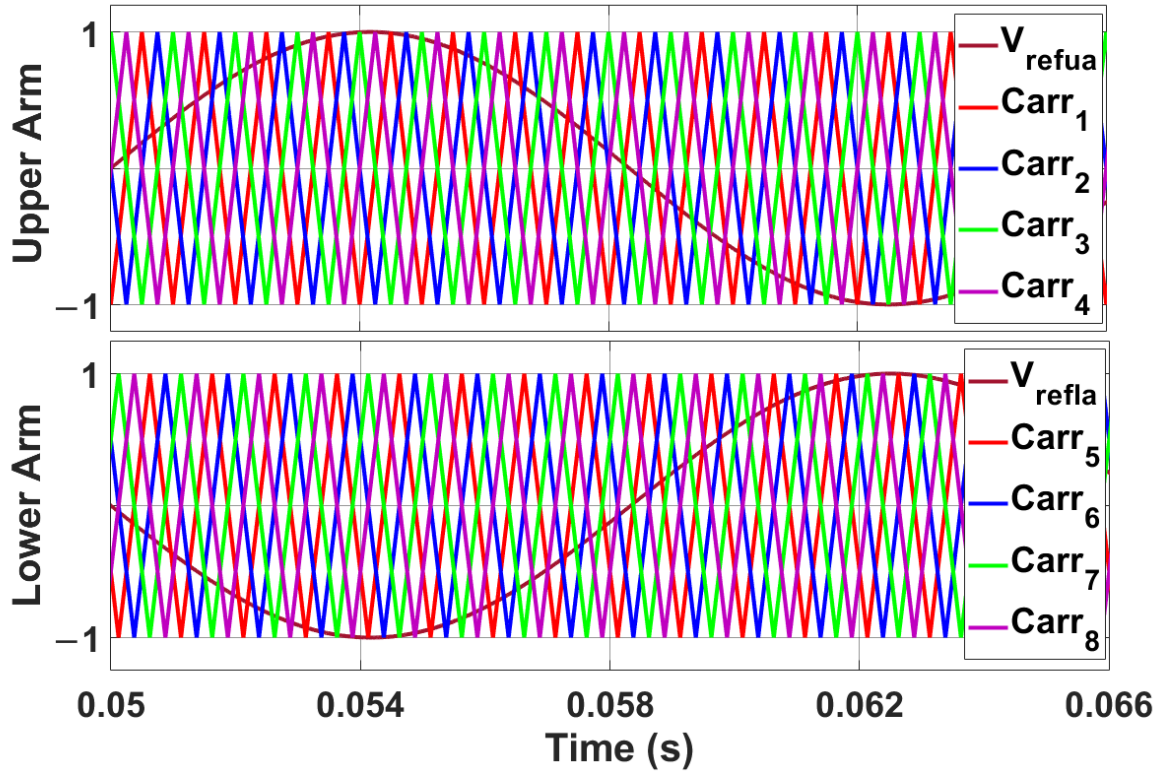


Figure 2. Reference voltage and carrier's waveforms in the upper and lower arm of phase a.

2.3. Comparison between HB-SM and ZPUC-SM for MMC Configurations

The primary benefit of using a ZPUC-SM in MMC configurations is the reduction in the total number of components in the converter. To emphasize this feature, Table 3 presents a comparison between the ZPUC-MMC and HB-MMC, both producing a 9-level phase voltage and a 17-level line-to-line voltage. The converters operate at identical switching frequencies, same DC link voltage value, and have matching parameters. In the case of the HB-MMC, eight HB-SMs are required in each arm to achieve the necessary voltage levels. Each HB consists of two switches and one capacitor, resulting in a total of 24 components per arm. In contrast, the ZPUC-MMC requires only a single SM per arm to produce the same voltage levels. Consequently, employing the ZPUC-SM in an MMC configuration significantly reduces the component count for achieving the same number of voltage levels. This results in decreasing the harmonics content, reducing the grid side filter and reducing the overall converter size, weight, and cost [14].

Table 3. ZPUC-SM Vs. HB-SM in 9L-MMC.

Converter Parameters	HB-SM	ZPUC-SM
DC Link Voltage, V_{dc}, (V)	400	400
Arm Inductance, L_{arm}, (mH)	1	1
Arm Resistance, R_{arm}, (Ω)	0.1	0.1
Load Inductance, L_g, (mH)	25	25
Load Resistance, R_g, (Ω)	20	20
Carrier Frequency, f_c, (Hz)	2000	2000
Power Factor, *PF*	0.9	0.9
Modulation Index, m	0.95	0.95
Number of SM per arm, N	8	1
Capacitors/arm	8	3
Switches/arm	16	6
Total number of components	144	54

3. Modeling and Control of Three-Phase ZPUC-MMC Grid-Connected Converter

3.1. ZPUC-MMC Mathematical Modeling

Modeling MMCs presents unique challenges compared to classical converters due to several factors: the multitude of switches, the necessity for additional controllers to balance floating capacitor voltages, and the elimination of a circulating current. Various modeling techniques have been employed for MMCs, including switching and average modeling [5,23]. While some models offer simplicity and quick simulation, they often sacrifice the representation of important aspects like switching effects, converter blocking behavior, and responses to AC and DC faults. Conversely, complex MMC models provide detailed descriptions but are more difficult to analyze and simulate, leading to slower simulations. In [14], the switching modeling technique is adopted to obtain the general modeling equations of the ZPUC-MMC. All the SMs of one arm were considered as one equivalent voltage source (v_{ui}, v_{li}) [24]. The significance of this mathematical model lies in its role as a foundation for understanding the underlying principles governing the ZPUC-MMC system independent of specific simulations. It allows for analysis, optimization, and extraction of the mathematical equations as a base for designing the control system for the proposed converter. The previously obtained mathematical equations to control each of the grid current and circulating current are given in Equations (4) and (5)

$$v_{oi} = e_i - L_{eq}\frac{di_{oi}}{dt}, \tag{4}$$

$$v_{cci} = L_{arm}\frac{di_{cci}}{dt} + R_{arm}i_{cci}, \tag{5}$$

$L_{eq} = \frac{L_{arm}}{2} + L_g$, $e_i = \frac{v_{li} - v_{ui}}{2}$, and $v_{cci} = \frac{V_{dc}}{2} - \left(\frac{v_{li} + v_{ui}}{2}\right)$, $i = a, b, c$.

Where v_{ui} and v_{li} are the upper and lower arm voltages in phase i, v_{oi} and i_{oi} are the grid voltage and the grid current (also called output current) in phase i, i_{cci} is the circulating current in phase i, L_{arm}, R_{arm} are arm inductance and resistance respectively, and L_g, R_g are the grid reactance and resistance. R_g and R_{arm} are very small, and are eliminated from all mathematical equations.

3.2. ZPUC-MMC Control System

For the efficient and reliable operation of the proposed ZPUC-MMC grid-connected converter, regulating the grid-current (GC), eliminating the circulating current (CC), and balancing the voltages of the ZPUC capacitors in each arm are imperative. Three levels were considered in the applied control system [5,25,26]. A high-level control is implemented to regulate the injected grid current, ensuring low harmonic content and compliance with grid connectivity requirements and standards [27]. A medium-level control aims to suppress the CC, thus reducing power losses in the converter and ripples in the capacitors' voltages of each ZPUC-SM. Lastly, a low-level control includes a modulation technique (PS-PWM) and integrated VB algorithm for generating the switching signals and for balancing the ZPUC-SM capacitors.

ZPUC was previously proposed as a new SM topology where preliminarily results were introduced on the ZPUC-MMC operating as a standalone system. The contribution of this paper is to propose a MMC based on the ZPUC-SM as a grid-tied converter in three-phase configurations, which was not presented before, and to validate its operation and control. For this reason, conventional controllers of MMCs are firstly applied to test the performance of the proposed converter in steady-state and dynamic operations. Due to the excessive number of inputs, outputs, required sensors and measurement, and limited tools available at the university's laboratory, which limit the availability of a physical prototype, FPGA-based RT simulation is adopted in this work. The schematic diagram of the control system of the proposed converter is illustrated in Figures 3–5. It includes GC control, CC control, and integrated VB control within the PS-PWM. Preliminary work was presented without a circulating current control loop. In this work, a circulating current control is added to obtain a comprehensive complete control system. Only the CC control is detailed in this paper as the other control levels were previously designed and detailed in [14].

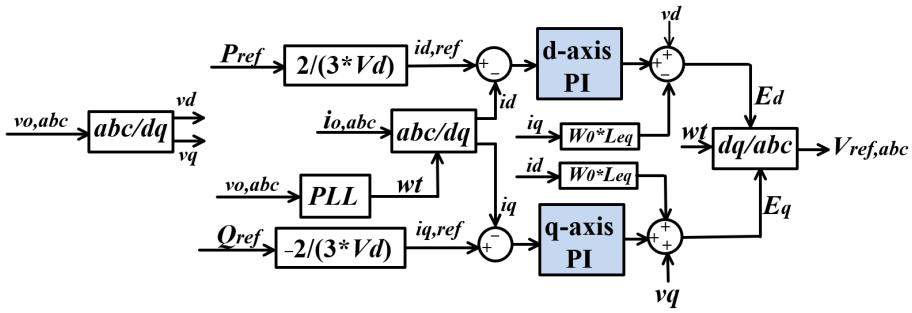


Figure 3. High-level grid-current control of the three-phase ZPUC-MMC: decoupled active and reactive power control on d and q axis.

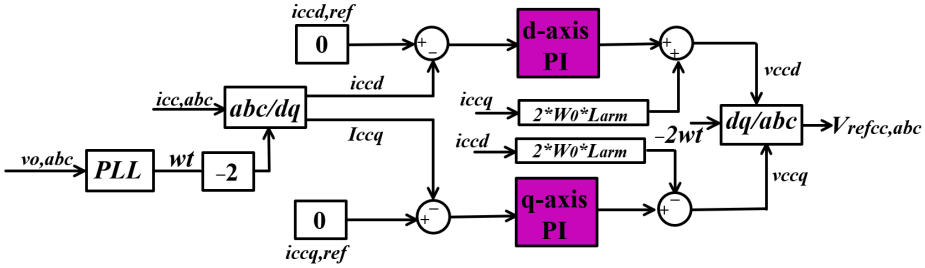


Figure 4. Medium-level circulating current control of the three-phase ZPUC-MMC.

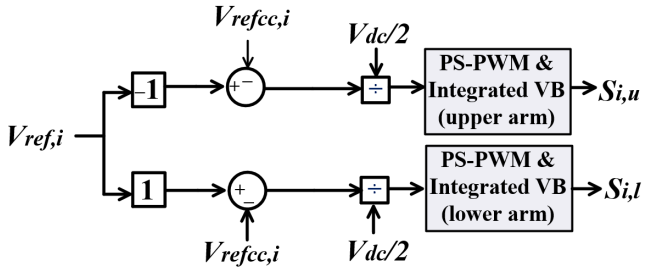


Figure 5. Switching signal generation in each upper and lower arm of each leg.

The CC caused by the variation in the instantaneous voltages across the legs of the ZPUC-MMC is an inherent phenomenon in MMC. Although CC does not affect AC-side grid voltages and grid currents, it is preferred to suppress it for an efficient and reliable operation of the MMC. CC increases the power losses, the switching devices stress, and the RMS current in each arm. Moreover, the CC has side effects on the capacitor's voltage ripple of each individual ZPUC-SM [28]. The available inductances in each arm of a MMC not only provide isolation within arms, but also play a role in limiting the CC. Increasing L_{arm} can reduce the CC to a certain extent, but at the expense of increasing the size, weight, and cost of the converter [7]. In this paper, the CC control method adopted is based on a negative-sequence rotational reference frame where PI regulators are tuned at double the fundamental frequency [28–30]. The main dynamic equation for controlling the CC is defined earlier in Equation (5). The CC in terms of arm currents and output current (grid current) is defined in Equations (6) and (7).

$$i_{ua} = i_{cca} + \frac{i_{oa}}{2}, \tag{6}$$

$$i_{la} = i_{cca} - \frac{i_{oa}}{2}, \tag{7}$$

where i_{ua} and i_{la} are the upper and lower arm currents in phase a, i_{cca} is the circulating current in phase a, and i_{oa} is the output current (also called grid current) in phase a. In fact, the CC is composed of a DC term in addition to a double-line frequency component and can be expressed as in Equation (8). The aim of the CC control is to suppress its second order frequency component.

$$i_{cci} = \frac{I_{dc}}{3} + I_{2f}\sin(2w_0t + \varphi_0 + \varphi_i), \tag{8}$$

$i = a, b, c$, and $\varphi_i = 0, \frac{2\pi}{3}$, and $\frac{-2\pi}{3}$, respectively.

Where, i_{cci} is the circulating current in each phase i, I_{dc} is the total DC current, I_{2f} is the peak value of the second order frequency component, w_0 is the fundamental frequency, and φ_0 is the initial phase angle between the grid current and grid voltage.

As a first step, the CC in each phase is calculated as in (9).

$$i_{cci} = \frac{i_{ui} + i_{li}}{2} - \frac{I_{dc}}{3},\ i = a, b, c \tag{9}$$

The obtained three-phase CCs are then transformed into two DC components in a dq reference frame (i_{ccd}, i_{ccq}). Park transformation of Equation (5) results in obtaining d and q axis components of the reference voltage of the CC as in Equations (10) and (11):

$$v_{ccd} = L_{arm}\frac{di_{ccd}}{dt} + 2L_{arm}w_0i_{ccq}, \tag{10}$$

$$v_{ccq} = L_{arm}\frac{di_{ccq}}{dt} - 2L_{arm}w_0i_{ccd}, \tag{11}$$

Two PI controllers take action in minimizing the d-axis and q-axis components of the CC, and in regulating each one of them to zero. According to Equations (10) and (11), there exist coupling terms between the d and q axis components, therefore a feedforward compensation decoupling method is applied and the compensation terms ($2w_0L_{arm}$) are added to the outputs of the PI controllers as it appears in Figure 4. This results in obtaining references voltages on the d and q axis (v_{ccd} and v_{ccq}) that will be transformed back to the abc reference frame: $V_{refcc,\,i}$, where $i = a$, b, and c.

The final reference voltage for the VB block incorporated within the modulation technique in each of the upper arm ($v_{refu,i}$) and lower arm ($v_{refl,i}$) of each phase is calculated as in Equations (12) and (13) and shown in Figure 5, and the switching signals in each of the upper arm ($S_{i,u}$) and lower arm ($S_{i,l}$) in each phase i are obtained.

$$v_{refu,i} = \frac{-V_{ref,i} - V_{refcc,i}}{\frac{V_{dc}}{2}}\ ,\ i = a, b, c \tag{12}$$

$$v_{refl,i} = \frac{V_{ref,i} - V_{refcc,i}}{\frac{V_{dc}}{2}},\ i = a,\ b, c \tag{13}$$

4. Real-Time Simulations Using CPU and FPGA

4.1. Real-Time Simulation Requirements

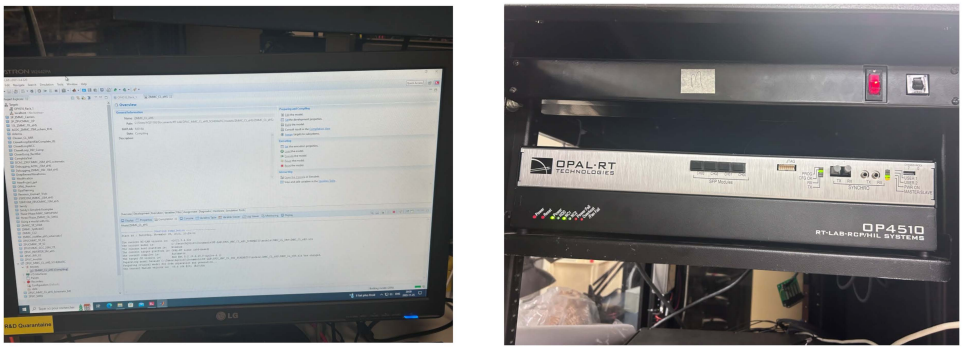
The primary objective of RT simulation is to generate accurate output waveforms that faithfully represent the behavior of real systems under experimental conditions. During RT simulation, the model is executed by a RT simulator using a predefined fixed time-step synchronized with real-world time. If the execution time-step exceeds this predefined value, the RT simulation loses its real-time status, resulting in time-delayed (offline) results [1,2]. When using only CPU-based Real-Time simulation, the overall proposed converter (ZPUC-MMC) with its control system is implemented, and executed only by the Target's cores (processors, CPU). With a complex topology such as MMC, the numerous switches and components and non-linear devices pose significant challenges for computation and necessitate iterative techniques. This results in increasing the load of the CPU to around 100%, while obtaining thousands of overruns. Overruns means the model is executed with a time-step exceeding the specified time-step for the real-time simulation. Thus, the real-time status of the results is lost, and instead the obtained results are similar to time-differed (offline) simulation results (MATLAB/SIMULINK). Addressing this issue typically involves either increasing the specified time-step or optimizing/simplifying the model. However, enlarging the time-step may compromise the accuracy of the results, while simplifying the model may not always suffice, particularly in scenarios involving complex converters like MMCs with numerous submodules (SMs) per arm. Dividing the RT model into subsystems to distribute execution across different CPU cores of the target can help manage the computational load. However, it poses challenges in synchronizing these subsystems to prevent delays and maintain coherence in real-time behavior. In the MMC, given the increasing complexity with the higher number of SM per arm, FPGA-based RT simulation emerges as an optimal solution [17,19,31]. With FPGA-based RT simulation, the converter's execution directly on the FPGA in the nanoseconds range, along with the control system's execution by the target's cores in the microseconds range, facilitate meeting specified execution times without encountering overruns, and while maintaining RT simulation status [17,19,20,31,32].

4.2. Real-Time Implementation of Three-Phase ZPUC-MMC

In the Real-Time simulation process, the OP4510 hardware target, and the RT-LAB software and RT-XSG toolbox were used to perform real-time implementation, simulation, and execution. The OP4510 is a compact entry-level simulator that offers a hybrid architecture with both a powerful CPU and an FPGA for high-performance real-time simulations. It integrates OPAL-RT RT-LAB software and an eFPGAsim real-time platform. In addition,

it has the highest performance processors from INTEL and FPGA chips, as well as industry standard SIMULINK software. Selecting the right combination depends on the specific requirements of the simulation model, however, we were limited to the use of OP4510 due to its availability at the university laboratory. The Target is equipped with four Intel Xeon E3 v5 3.5GHZ CPU cores, and one Xilinx FPGA Kintex-7 325T for electrical circuit solvers. The minimum time-step for the model subsystems executed using Target cores is 7 µs, however for models executed on the FPGA chips, a minimum of 250 ns time-step is required.

The ZPUC-MMC is implemented in real-time using a host PC, OPAL-RT Target "OP4510", and RT-LAB software (simulation in the loop mode), with an FPGA-based Electric Hardware Solver (eHS), as shown in Figure 6. The aim is to verify and validate the effectiveness and robustness of the proposed system and its conventional controller under steady-state and dynamic operations. RT-LAB software is a tool used for running real-time (RT) simulations for OPAL-RT Targets, and provides full integration with MATLAB/SIMULINK. The software is installed on a Personal Computer in the GREPCI laboratory that is connected to the OP4510 hardware target through a Transmission Control Prototype (TCP). RT simulation on RT-LAB is based on having a top-level Simulink model which consists of subsystems divided as follows: (i) Computational subsystems (SM) and (SS) which are executed by the target for calculations, data logging, and I/O managements; and (ii) Graphic user interface subsystems (SC) which is generated by the host PC. In this study, one graphical subsystem (SC_scope) is built to visualize the waveforms, and one computational subsystem (SM_Control), which includes the control system of the ZPUC-MMC as well as the eHS block for implementing the ZPUC-MMC converter using a schematic editor. The VB algorithm integrated within the the PS-PWM, the grid current control, and the circulating current control of the ZPUC-MMC with 1SM/arm are built on the host PC using RT-LAB software (version 2021.3.4.320), and are executed using one core (out of 4) of the target "OP4510". The control system is modeled using the Sim Power Scape (SPS) of SIMULINK/MATLAB and then converted into a compatible model for RT simulation using RT-Lab library blocks, as shown in Figure 7, that represents the system structure as well as the interaction between the real-time target (hardware) and the software platform (host PC). However, the proposed grid-tied ZPUC-MMC converter is built on eHS using the Schematic Editor, as shown in Figure 8, and executed using the FPGA of the target. eHS is an FPGA-based technology that is accessible to many users due to the convenient circuit schematic editor user interface, so that the FPGA is automatically generated without having to write mathematical equations. To obtain the conductance matrix, the Pejovic1 method is employed. A switch in an off-/open state is symbolized by an inductor, while in an on-/close state it is represented by a capacitor. The conduction matrix does not change during simulation and does not require recalculation with each iteration. Specific firmware is selected based on the license class of the target (License class 62). The complete model is built, compiled, and then loaded into the RT hardware (OP4510 target) for RT execution as a final step. The control system operates with a time-step of 20 us. For the ZPUC-MMC model, it is executed on an FPGA with a time step of 695ns. A screenshot of the probe taken during RT simulation is illustrated in Figure 9. The total CPU load (16.99%), the control time-step Ts, and the number of overruns are all together displayed through the probe. The target hardware specifications are illustrated in Table 4, and the system's parameters are described in Table 5. It is important to mention that with the controller executed in the CPU-based RT simulation and the converter in the FPGA-based RT simulation, there is potential for an increase in switching frequency and the number of ZPUC-SM per arm. However, this will not compromise the efficiency or robustness of results during different modes of operation.



(**a**) (**b**)

Figure 6. Desktop computer (**a**) and OP4510 target (**b**) used in GREPCI laboratory.

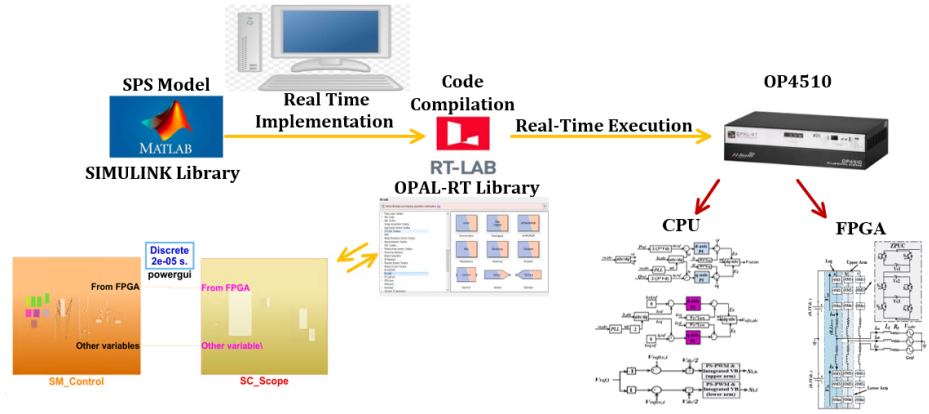


Figure 7. Real-Time execution using RT-LAB software and OP4510 hardware with CPU and FPGA.

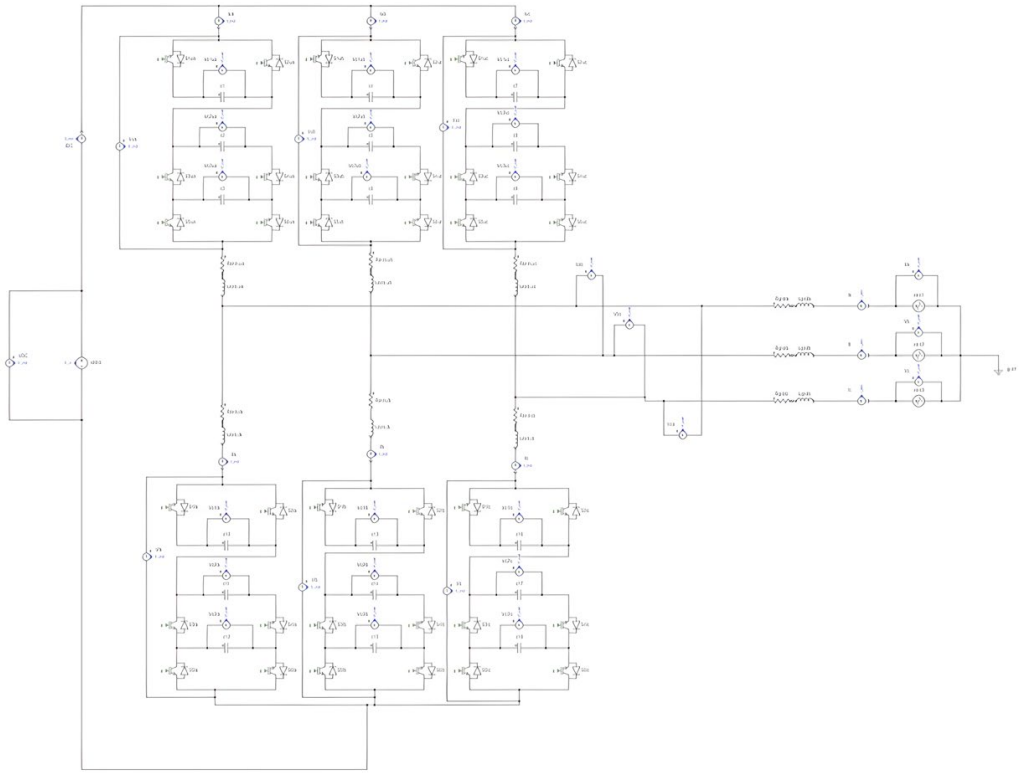


Figure 8. Three-Phase ZPUC-MMC grid-connected converter built on an eHS block using Schematic Editor.

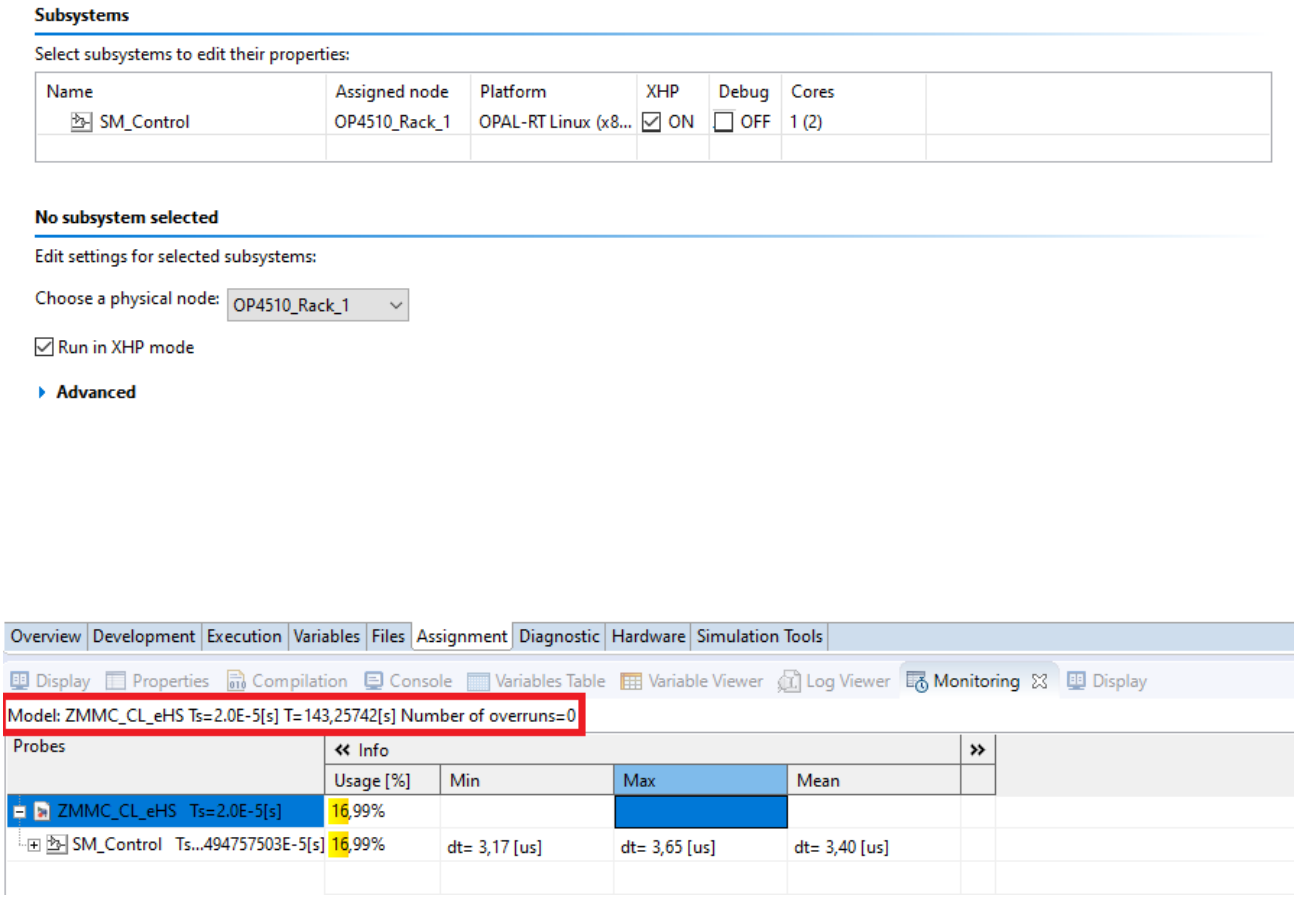


Figure 9. Screenshot of real-time probe monitoring taken during real-time execution of the three-phase ZPUC-MMC grid-connected converter.

Table 4. Real-Time simulator specifications (OP4510).

Target Parts	Values
FPGA	Kintex-7 FPGA, 325T, 326,000 logic cells, 840 DSP slice (Multiplier-adder).
Computer cores	Intel Xeon E3 v5 CPU (4 core, 8 MB cache, 2.1 or 3.5 GHz), 16 GB RAM, 256 GB SSD.

Table 5. Real-Time converter parameters.

Parameters	Values
RMS line-to-line Voltage, V_s	600 V
Line frequency, f_0	60 Hz
DC Bus Voltage, V_{dc}	2000 V
ZPUC-SM per arm, N	1
Active Power, P	1 MW
Grid Reactance, Resistance, L_g, R_g	1 mH, 0.1 Ω
Arm Inductance, Resistance, L_{arm}, R_{arm}	0.5 mH, 0.05 Ω
Capacitors of ZPUC-SM, C_1, C_2, and C_3	30 mF
Switching Frequency, f_{sw}	1000 Hz

5. Real-Time Simulation Results

It is important to note that in RT simulation and implementation, the capacitors of the ZPUC-SM are not assumed pre-charged since the behavior of the converter control is

executed using a mathematical model which predicts the operation of the MMC under different conditions. However, for industrial applications, where actual components of an MMC are used, the capacitors of each ZPUC-SM in each arm should be pre-charged to avoid high inrush currents when the converter is firstly energized. In this case, the pre-charging process involves gradually charging the capacitors to their nominal voltages.

5.1. Steady-State Operation

The RT simulation results under steady state operation are illustrated and analyzed first. The DC bus voltage value is 2000 V, and 1 MW purely active power is injected into the grid.

The three-phase grid currents, alongside the 9L-phase voltages are shown in Figure 10. Considering a balanced three-phase system, simulation outcomes per phase 'a' will be exclusively presented and examined throughout the study under different modes of operation. It can be noticed from Figure 11 that the grid-current control is perfectly achieved. The grid current exhibits a sinusoidal waveform perfectly aligned with the grid voltage, resulting in effectively achieving a unity power factor. Moreover, the *d*-axis and *q*-axis components of the grid current perfectly follow their references while achieving zero steady-state error, as can be observed in Figure 12. Moreover, according to Figure 13, the grid current is controlled to have reduced harmonics content, measuring at 0.59% (<5%) according to IEEE standards std519, affirming the efficacy of the implemented controller. According to the AC voltage waveforms presented in Figure 14, 9L-phase voltage is obtained that ranges from $V_{dc}/2$ (1000 V) to $-V_{dc}/2$ (-1000 V) in increments of $E/2$ (250 V). Additionally, the 5L-upper and lower arm generated voltages range from 0 to 4NE (2000 V) in steps of E (500 V). Furthermore, upon the examination of the waveforms presented in Figure 15, it is evident that the VB algorithm is effectively achieved. The voltages of capacitors C_1 and C_2 are effectively regulated and balanced at around 2E (1000 V), while the voltage across the third capacitor C_3 remains at E (500 V). The voltages across the capacitors are evenly balanced, exhibiting minimal voltage ripple, measuring at less than 10%.In addition, according to Figure 16, showing the upper and lower arms current as well as the CC in phase a, it is evident that the CC control is carried out. The second order component of the CC generated between the upper and lower arm is removed.

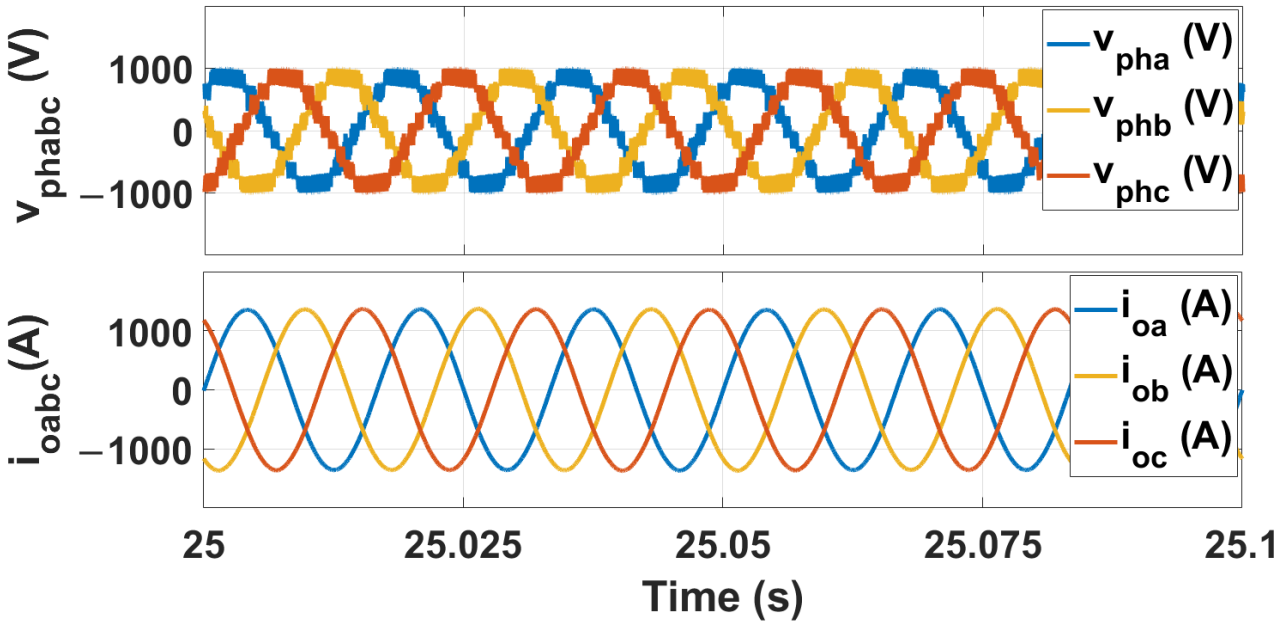


Figure 10. Three-phase grid currents and 9L-three-phase grid voltages during steady-state operation.

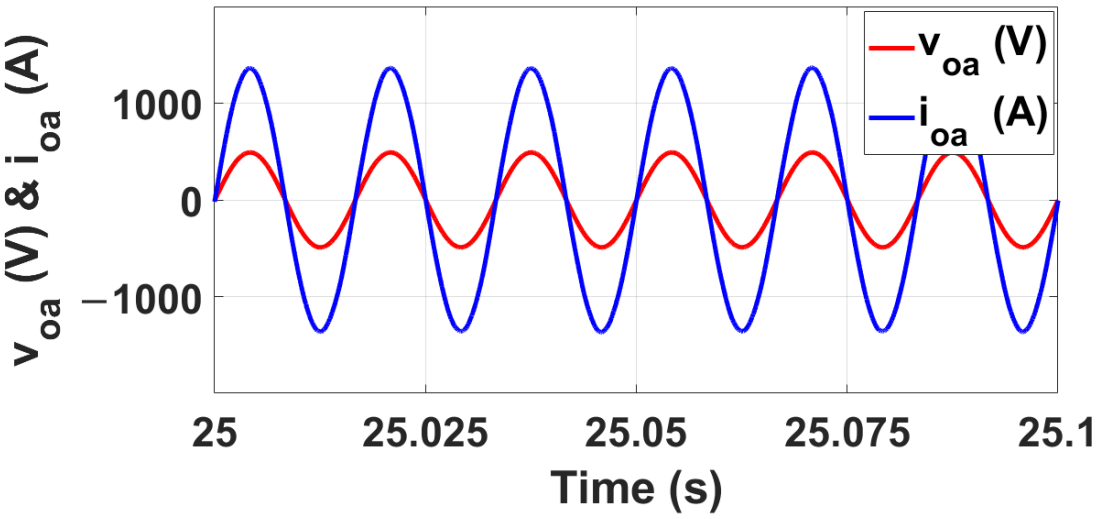


Figure 11. Grid voltage and current in phase a during steady-state operation.

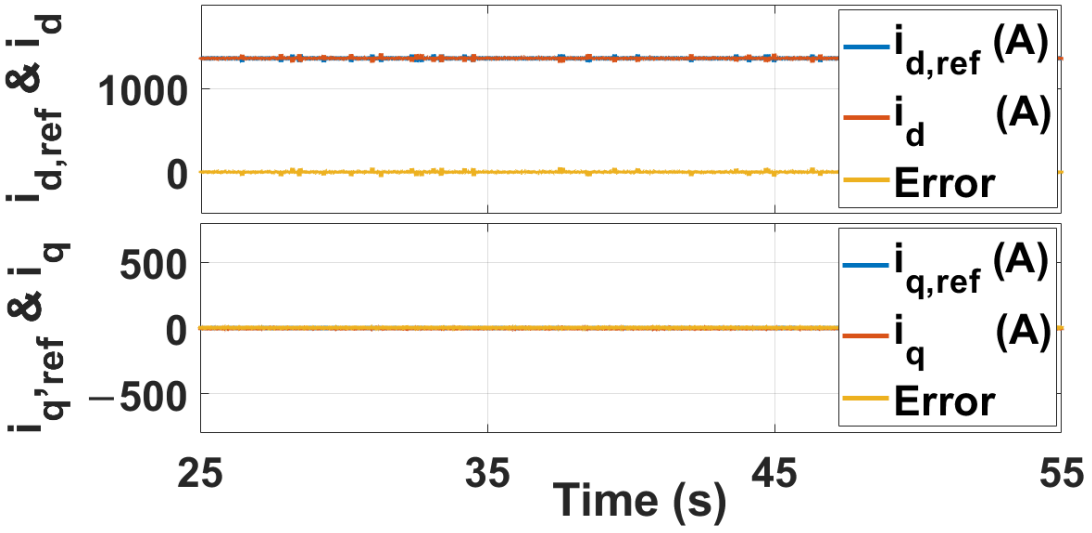


Figure 12. *dq*-axis reference and measured currents during steady-state operation.

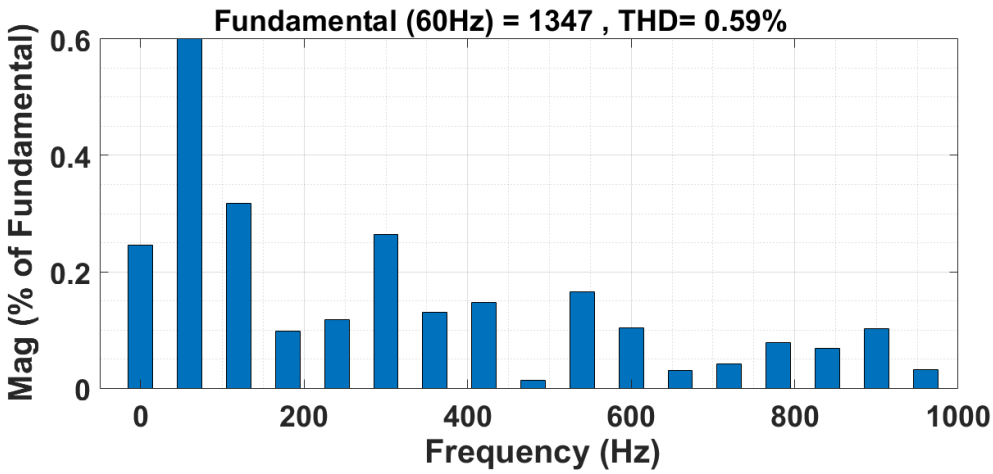


Figure 13. Percentage of THD in grid-current of phase a.

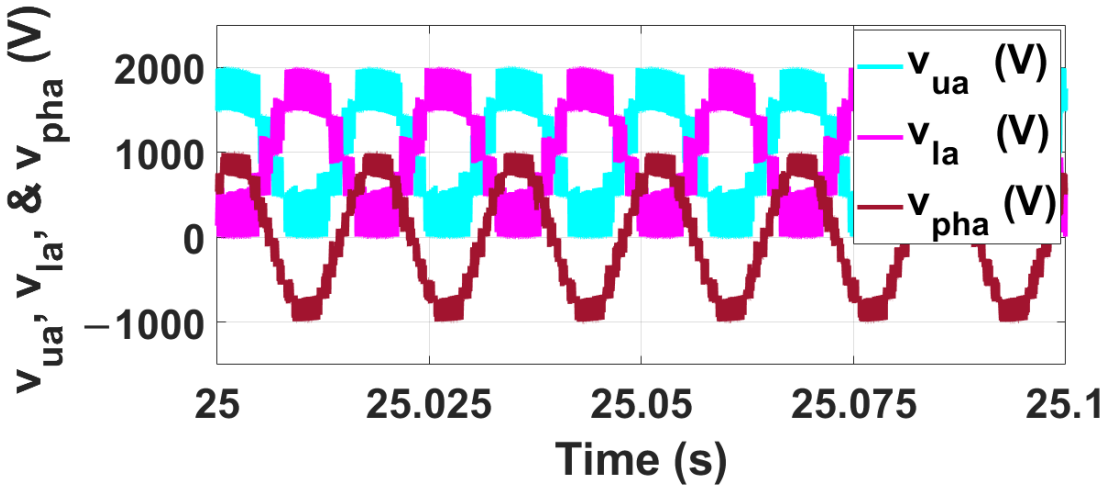


Figure 14. 5L- upper and lower arm voltages, and 9L-phase voltage in phase a during steady-state operation.

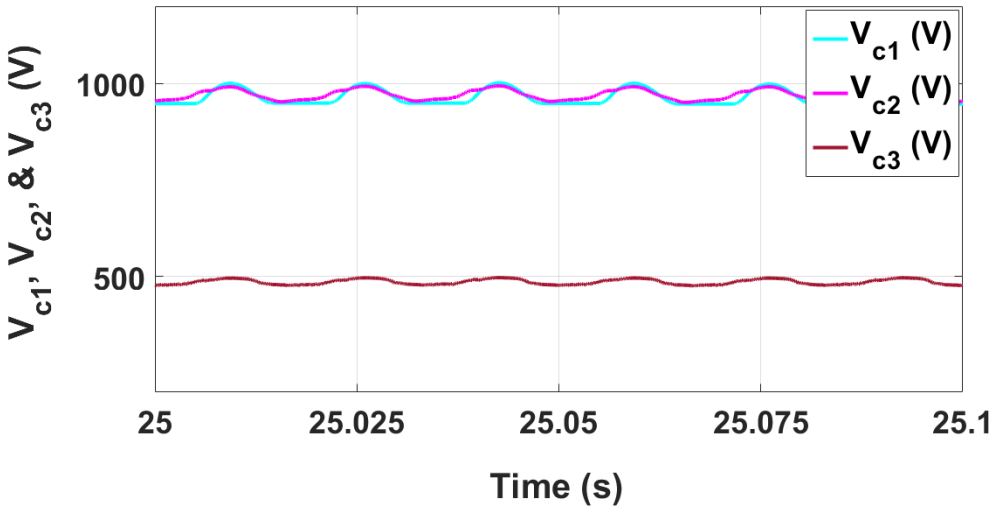


Figure 15. ZPUC-SM capacitor voltages in the upper arm of phase a during steady-state operation.

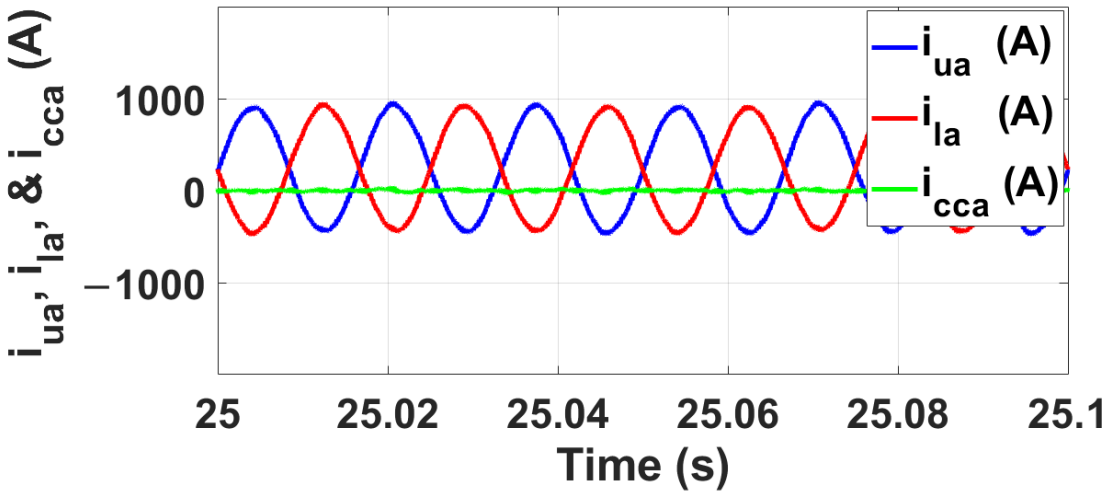


Figure 16. Upper and lower arm currents, and circulating current in phase a during steady-state operation.

5.2. Dynamic Operation

Dynamic testing of the proposed converter involved active power and DC voltage variations.

At t = 25 s, the initial change involves altering the DC voltage source, reducing V_{dc} from 2000 V to 1800 V. The corresponding waveform results are illustrated in Figure 17. The robustness of the grid-current control to DC voltage fluctuations is clearly evident: the injected grid current consistently exhibits sinusoidal waveform and synchronizes precisely with the grid voltage. Also, 5L-voltages are generated across both the upper and lower arm voltages, while 9L-voltages emerge across each phase. Notably, these voltage levels conform to the adjusted DC voltage of 1800 V, confirming the applicability of the formulas presented in Equations (1)–(3) in Section 2. Hence, the voltages across the upper and lower arms span from 0 to 4NE (1800 V), while the 9L-phase voltage ranges from $V_{dc}/2$ (900 V) to $-V_{dc}/2$ (−900 V). Moreover, the three capacitors within the ZPUC-SM continue to maintain balance in accordance with the updated DC voltage, affirming the efficacy of the VB algorithm integrated within the PS-PWM. Specifically, V_{c1} and V_{c2} are balanced and regulated around 2E = 900 V, while V_{C3} remains at E = 450 V. The fluctuations in the capacitor voltages are below 10%. On the other hand, by monitoring the CC that is nearly supressed and equal to zero, it can be concluded that CC control is very well achieved.

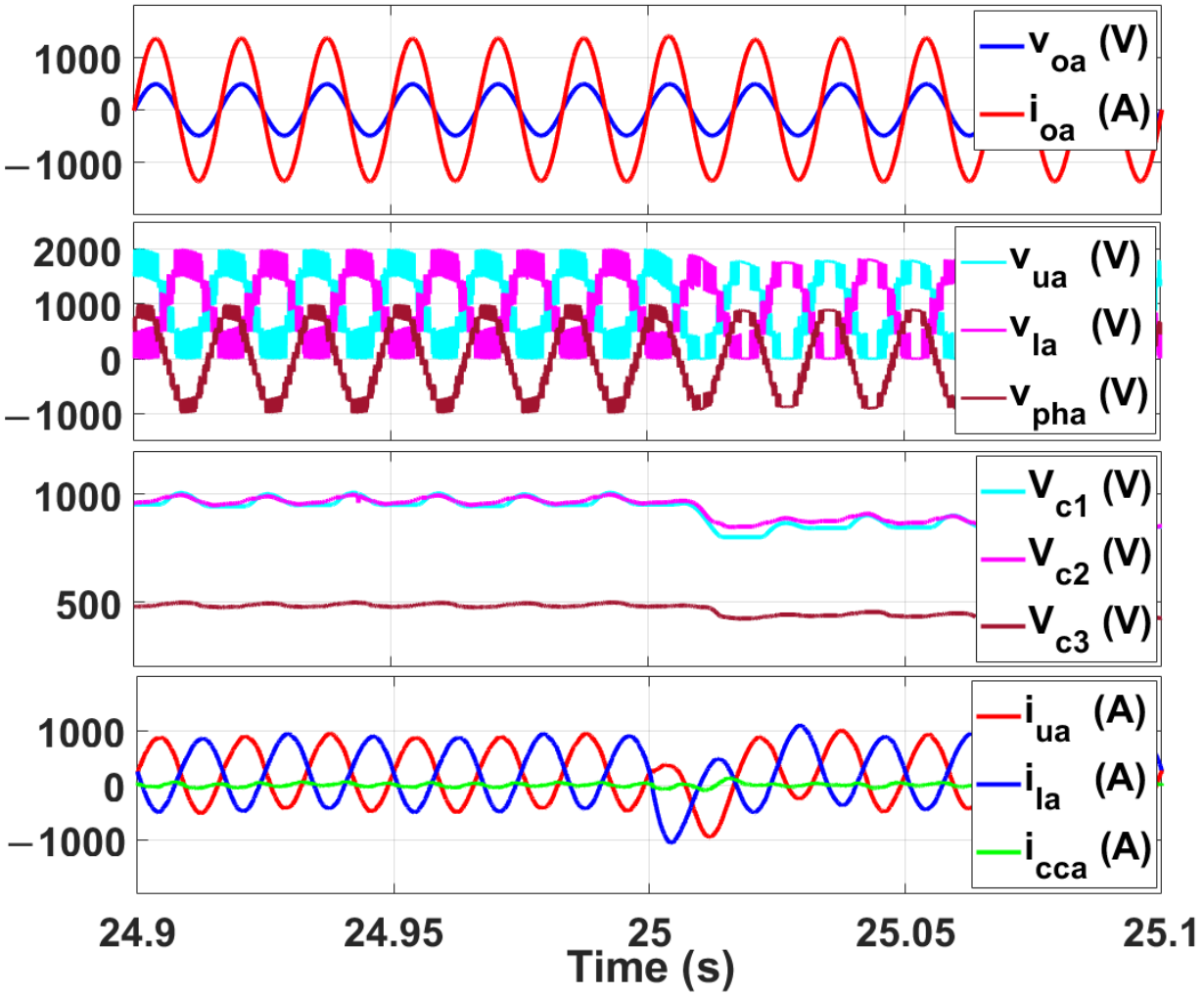


Figure 17. DC voltage variation: step change from 2000 V to 1800 V at t = 25 s.

The second dynamic test involves a sudden alteration in the injected active power at t = 25 s, raising it from 1 MW to 1.2 MW. This step change results in an increase in the grid current, as evidenced by the results depicted in Figure 18. However, it is worth noting that

the grid current consistently maintains a sinusoidal waveform and synchronizes precisely with the grid voltage, verifying the effectiveness of the grid-current control system. In addition, the number of generated voltage levels is not affected: 5L-upper and lower arm voltages and 9L-phase voltages are carried out. The fluctuations in injected active power do not impact the effectiveness of the VB algorithm, which consistently maintains the capacitors' voltages within the ZPUC-SM at desired levels, ensuring they remain balanced and regulated. Also, during this dynamic performance, it is obvious that the CC is reduced and equal to zero, which proves the effectiveness and the robustness of the CC control.

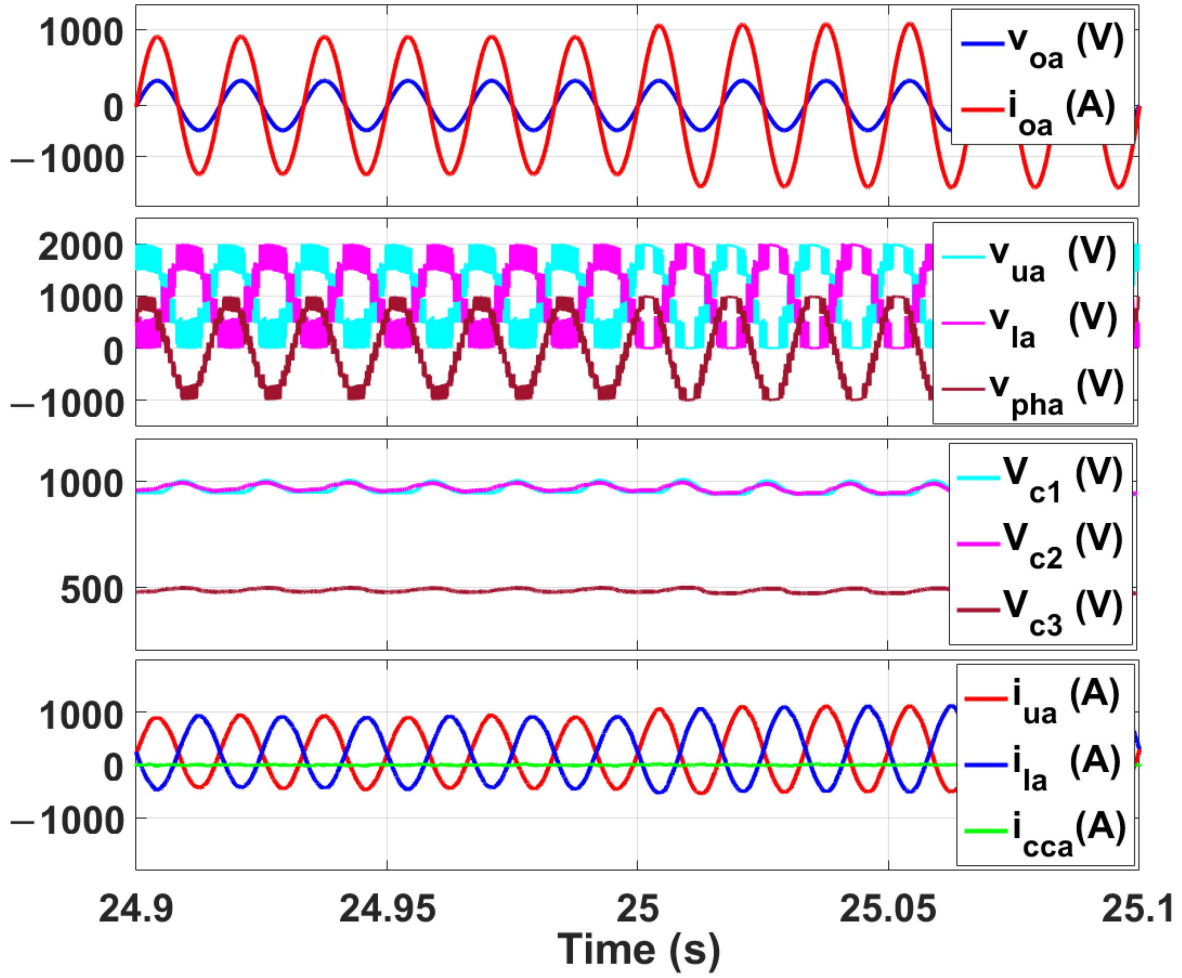


Figure 18. Active power variation: step change from 1 MW to 1.2 MW at t = 25 s.

5.3. Proposed Design Limitations

While the ZPUC-MMC offers several advantages, such as increased voltage levels with fewer SMs, reduced component count, and integrated voltage balancing within the Phase-Shift Pulse Width Modulation, it is important to note that the ZPUC-SM is a unipolar SM and lacks DC fault handling capability. To address this, authors are actively investigating a hybrid submodule structure based on ZPUC and Full-Bridge configurations that will provide DC fault blocking capability.

Furthermore, authors are exploring new applications for the ZPUC-MMC, including the incorporation of multiple ZPUC-SMs per arm. For example, employing two ZPUC-SMs per arm (four per leg) enables the generation of 17-level phase voltages and 33-level line-to-line voltages, thereby enhancing AC voltage waveforms and reducing harmonic content. Additionally, efforts are underway to extend the application of the ZPUC-MMC to HVDC and MVDC systems, accompanied by expanded analyses and test scenarios. These analyses

will encompass the working principles in unbalanced systems and design considerations for redundancy.

6. Conclusions

In this work, a MMC converter using a ZPUC-SM is proposed for three-phase grid-connected applications. The advantage of the proposed topology is to generate a higher number of voltage levels with a reduced number of SMs, which results in reducing the overall size, cost, and volume of the proposed converter. The effectiveness and performance of the converter were validated under steady-state and dynamic operations. Accordingly, conventional controllers of MMCs based on a decoupled *dq* reference frame are applied to regulate the grid current as well as the circulating current in order to have a complete comprehensive control system. The contribution of the work is to adapt the model of the converter in real-time simulation for verification and validation while having zero-overruns. The converter was never built before on a real-time platform, and the innovation regarding the FPGA aspect is in obtaining the model of the converter in the eHS block, which required a lot of tuning for the internal parameters of the converter switches presented in the schematic editor. The overall proposed system is implemented and executed on the CPU- and FPGA-based real-time simulation platform using OPAL-RT Target (OP4510) hardware. The output current is injected to the grid with a low harmonics content, thus obeying the grid connectivity standards. The inherent undesirable circulating current is suppressed, and the capacitors of each ZPUC-SM in each arm are balanced and regulated around desired values without having any additional controller. The obtained real-time simulation results validate the effectiveness and robustness of the proposed converter during steady-state and dynamic operations. It can be concluded that the ZPUC-MMC is a promising solution for grid-connected medium-/high voltage applications.

Author Contributions: Conceptualization, S.A.; methodology, S.A. and F.S.; software, S.A.; validation, S.A. and F.S.; formal analysis, S.A.; investigation, S.A. and F.S.; resources, S.A.; writing—original draft preparation, S.A.; writing—review and editing, S.A., F.S. and R.Z.; supervision, F.S., R.Z. and K.A.-H.; project administration, K.A.-H.; funding acquisition, K.A.-H. All authors have read and agreed to the published version of the manuscript.

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