IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received 11 March 2025, accepted 26 April 2025, date of publication 30 April 2025, date of current version 9 May 2025.

Digital Object Identifier 10.1109/ACCESS.2025.3566015

RESEARCH ARTICLE

Z Packed U-Cell Modular Multilevel Converter for STATCOM Applications

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This work was supported by Canada Research Chair in Electrical Energy Conversion and in Power Electronics at École de Technologie Supérieure.

ABSTRACT The Modular Multilevel Converter (MMC) is a promising topology for STATCOM applications due to its key features, such as modularity, scalability, and reduced harmonic content. Increasing the number of voltage levels in MMC reduces harmonics but simultaneously increases the number of submodules (SMs) per arm, leading to larger sizes and higher costs, which presents a challenge. To address this, this article introduces a novel 17-level MMC-STATCOM based on the Z Packed U-Cell (ZPUC) converter as its SM, which enables the generation of more voltage levels with fewer components and reduced harmonic content, offering significant advantages in terms of size and cost. Given the complex structure of the proposed converter and the associated challenges in building a physical prototype, real-time (RT) simulation using FPGA technology is employed for validation. The key contributions include integrating the ZPUC-SM into a three-phase STATCOM for the first time and adapting the converter model and its control system to RT tools, including RT-LAB with an electric hardware solver for FPGA execution. In addition, capacitor voltage balancing and energy sorting algorithms are integrated within Phase-Shift Pulse Width Modulation, eliminating the need for an additional controller while maintaining the floating capacitors of ZPUC-SMs balanced and regulated. The specifications of the proposed converter are defined, the mathematical model and control system are derived, and a real-time implementation based on CPU and FPGA execution is built to verify the scheme. The obtained RT simulation results provide practical evidence confirming the effective operation of the proposed scheme in VAR compensation mode.

INDEX TERMS Electric hardware solver, modular multilevel converter, real-time implementation, RT-LAB, STATCOM, submodule, Z Packed U-Cell converter.

I. INTRODUCTION

Nowadays, medium-voltage distribution systems face a surge in non-linear and unbalanced loads, primarily from industrial sources. These loads create power quality problems, such as harmonic distortion, low power factor, and uncontrollable reactive power, resulting in disturbances in the operation of the electrical system [1]. To ensure reliable operation, it is crucial to address these disturbances promptly. The static synchronous compensator (STATCOM) emerges as a viable solution, offering effective reactive power compensation and voltage regulation, thereby enhancing power system performance [2], [3], [4].

Voltage Source Converters (VSCs) are considered essential among various types of converters. Two-level VSCs (2L-VSCs) are widely used in industrial applications due to their simple architecture and ease of control. However, implementing a practical STATCOM based on 2L-VSCs necessitates the use of line-frequency transformers, resulting in compensators that are bulky, heavy, and costly. High

The associate editor coordinating the review of this manuscript and approving it for publication was Sunil Kumar Dube.

switching losses and increased harmonic distortion necessitate extensive filtering, which impacts overall efficiency and system complexity. The limited voltage capability and poor scalability pose a challenge to their application in high-power scenarios. These limitations underscore the preference for multi-level converters (MLCs) in modern STATCOM designs, given their superior performance and scalability [5], [6].

STATCOMs based on MLCS have been extensively studied and employed due to their enhanced power ratings, improved power quality, lower harmonic distortion, and the ability to function without the need for bulky line-frequency transformers, making them suitable for medium- and high-voltage applications [5], [7]. Among the various MLC topologies, Flying Capacitor (FC), Neutral Point Clamped (NPC), and Cascaded H-Bridge (CHB) are prominent representatives [8], [9], [10]. The major drawback of the FC topology is the high expense associated with flying capacitors, particularly at low carrier frequencies. Additionally, they are not suitable for applications requiring pure 90° leading or lagging currents [11]. The NPC topology requires an additional voltage balancing circuit to manage the flying capacitors, and both FC and NPC topologies necessitate an increase in component count (capacitors, and clamping diodes) as the voltage levels increase [12]. The CHB topology remains one of the most suitable candidates for high-power reactive power compensation applications. However, CHB converters cannot operate continuously under unbalanced systems unless supplied by separate DC voltage sources. These sources are typically fed through multi-winding transformers, which reintroduce similar issues associated with line frequencies [13], [14].

Among the MLC topologies, Modular Multilevel Converter (MMC) is a promising topology for the next generation of converters for medium-/high voltage applications. Throughout the literature, MMCs have been employed in different applications such as Offshore wind Turbines [15], STATCOMS [16], Photovoltaic Systems [17], and Electric Vehicles [18]. They are characterized by various features such as reduced harmonic content, modularity, scalability, and easy expansion to a higher range of voltage levels [2], [4], [19]. Despite all the advantages of MMC for STATCOM applications, the implementation of this converter is still expensive due to the need for various submodules (SMs) per arm to generate a higher number of voltage levels. Thus, the improvement of the efficiency and the reliability of the converter is mandatory to reduce the operational costs and enable expanding the employment of MMC in the industrial sector and targeting various applications [4]. Additionally, the design of the MMC structure, which is inherently complex, is challenging, and depends on various factors such as the number of SM units per arm, the required number of voltage levels, the rating of semiconductor switches, and the design of SM capacitance [19], [20]. Different efforts have been presented in the literature to improve converter efficiency. These efforts focused on SM design [4], circulating current control reduction/suppression that reduces power losses in the converter [20], and modulation techniques such as the nearest level modulation (NLM) [20] and the PS-PWM [21]. The switching losses of the converter can be improved by the selection of the SM topology [22], the use of wide-bandgap devices [23], and by the use of thyristor/diode bypassed SM [24].

In MMC, harmonic content could be further reduced by increasing the number of SMs/arms which in turn increases the number of generated voltage levels. However, this enhancement comes at the expense of a larger size and higher costs for the converter. Several SM topologies have been developed by researchers to enhance the performance of MMC. The topologies are classified based on various characteristics such as output voltage levels, SM polarity (uni-/bipolar), number of components per SM, and DC fault handling capability (DFH) [25], [26], [27]. The most common configurations are the Half-Bridge (HB) and the Full-Bridge (FB) [28], which both generate only 2L- voltages at their outputs. HB-SM has a very simple configuration and was initially employed in early MMC implementation [29]. In contrast, the FB-SM, despite incurring twice the switching and conduction losses compared to HB-SM, offers the advantage of DFH capability. In [30], the unidirectional cell (U) was introduced. U-SM reduces the number of active switches by half compared to HB-SM but experiences higher losses due to the presence of a diode. Furthermore, Clamped Diode (CD), featuring DFH capability, was introduced in [31]. This topology consists of two consecutive HB-SMs with an additional IGBT switch and two single diodes, thereby increasing both the size and cost of the MMC configuration.

Different multilevel SM topologies have been proposed in the literature, including the three-level neutral point clamped converter (3L-NPC) [26] and the three-level Flying Capacitor converter (3L-FC) [32]. However, 3L-NPC suffers from uneven current sharing among switches, leading to increased conduction losses [33], meanwhile, the drawback of 3L-FC is the huge number of DC voltage sources [26]. Another multilevel topology, the 5L- cross connected cell (5L-CCC) [34], achieves a 5L- output, but presents a major challenge in balancing its two capacitors. In [35], 7L Packed U-Cell converter was employed in MMC configuration to obtain a higher number of generated voltage levels, however, the necessitates a complex voltage balancing algorithm to balance the floating capacitors of the topology. Lately, authors of [36], have introduced the 5L- Z Packed U-Cell (5L-ZPUC) for MMC applications. This topology generates 5L at its output without any additional voltage balancing controller while reducing the components count when compared with other conventional topologies such as the HB-SM. Z Packed U-Cell (ZPUC) converter offers increased voltage levels with fewer components, thereby enhancing cost-effectiveness [37]. The different SM topologies introduced in the literature are summarized in Table 1 and compared in terms of hardware and

TABLE 1. Different SM topologies for MMC.

Type	Hardware Perspective				Control Perspective	
SM	#of SM	#of C	#of IGBTs	#of Diodes	Arm Voltage Levels	Unipolar, Bipolar/ Multilevel?
HB	N	N	2*N	2*N	N	unipolar/no
U	N	N	N	2*N	N	unipolar/no
FB	N	N	4*N	4*N	N	bipolar/no
DC	N	2*N	5*N	7*N	2*N	unipolar/no
3L-NPC	N	2*N	4*N	6*N	3*N	bipolar/yes
3L-FC	N	2*N	4*N	4*N	3*N	bipolar/yes
5L-CCC	N	2*N	6*N	6*N	5*N	bipolar/yes
7L-PUC	N	2*N	6*N	6*N	7*N	bipolar/yes

control perspectives. Using a multilevel topology for the SM increases the number of generated voltage levels in each arm.

Although MMC is a promising topology, validating its control and modulation techniques poses challenges, especially in the absence of a physical prototype. Therefore, real-time (RT) simulation emerges as a vital tool for verifying the performance of complex topologies and validating proposed modulation and control techniques [1], [27], [38].

However, the numerous components of MMC, along with its non-linear devices, pose significant numerical challenges for computation, necessitating iterative techniques for accurate simulations [39], [40], [41].

RT simulation of MMC can be implemented on various platforms including the central processing unit (CPU) and the field programmable gate array (FPGA) [41]. While CPU-based modeling provides flexibility and ease of implementation, the execution time for each node typically ranges in tens of microseconds, thus limiting system accuracy. FPGA technology in RT offers a superior alternative, enabling simulation times to be reduced to hundreds of nanoseconds. This makes FPGA the optimal solution for RT simulation of MMC, allowing for smaller time-steps, faster simulation speeds, and improved result accuracy [39], [40], [41].

Aiming at these problems, this article is devoted to proposing a promising 17L- ZPUC-MMC STATCOM. The contributions include testing the converter for a three-phase STATCOM application using a conventional controller and adapting the converter model and its control to real-time tools including RT-LAB with an electric hardware solver (eHS) for FPGA execution. The proposed approach offers several advantages including: 1) the generation of a higher number of voltage levels with fewer component counts as compared to Half-Bridge MMC [37]. 2) Integration of inherent capacitor voltage balancing (VB) and energy sorting (ES) algorithms within Phase-Shift Pulse Width Modulation (PS-PWM); eliminating the need for an additional controller. 3) Modeling and implementing the complex converter on a RT platform, thus fast and efficient RT results are obtained. The paper is divided as follows: a comprehensive presentation of the ZPUC converter operating as a single SM and in MMC, along with VB and ES algorithms, is provided in section II. The mathematical model and control are described in section III. Then, section IV illustrates the RT implementation and adaptation of the converter model and its proposed control system to real-time simulation tools using OP4510 Target Hardware, RT-LAB software, and electric Hardware Solver (eHS) for FPGA execution. The obtained RT simulation results are presented as proof of concept, validating the operation of the proposed system in VAR compensation mode in section V. ZPUC-MMC potential future works are discussed in section VI. And finally, to sum up, a conclusion is provided in section VII.

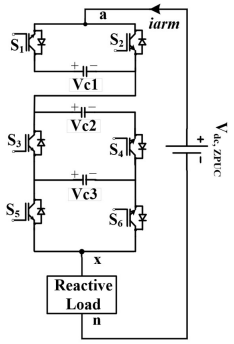

FIGURE 1. Z Packed U-Cell as a single inverter.

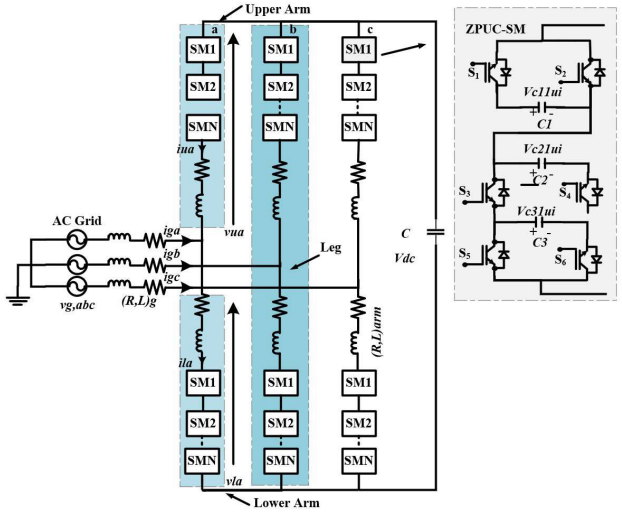

FIGURE 2. Proposed 17L- Z Packed U-Cell MMC STATCOM.

II. PROPOSED 17L-ZPUC-MMC STATCOM

A. ZPUC SINGLE INVERTER

ZPUC was introduced as an inverter for both single-/three phase applications, as well as a submodule in MMC configurations. This converter uses a single DC source in both single-/three-phase systems. According to Fig. 1, t is built with six switches and three floating capacitors, where S_1, S_3, and S_5 are operated in a complementary manner to S_2, S_4, and S_6, creating 8 (2^3) possible switching states. Maintaining balanced capacitor voltages is critical. Depending on the regulated values of the floating capacitors of ZPUC-SM, the

TABLE 2. Five levels ZPUC switching states.

States	S_1 S_3 S_5	V_{ax}	V_{ax} (5L)
1	100	$V_{c1} + V_{c2}$	4E
2	101	$V_{c1} + V_{c2}$ -V_{c3}	3E
3	110	$V_{c1} + V_{c3}$	3E
4	111	V_{c1}	2E
5	000	V_{c2}	2E
6	001	$V_{c2} - V_{c3}$	E
7	010	V_{c3}	E
8	011	0	0

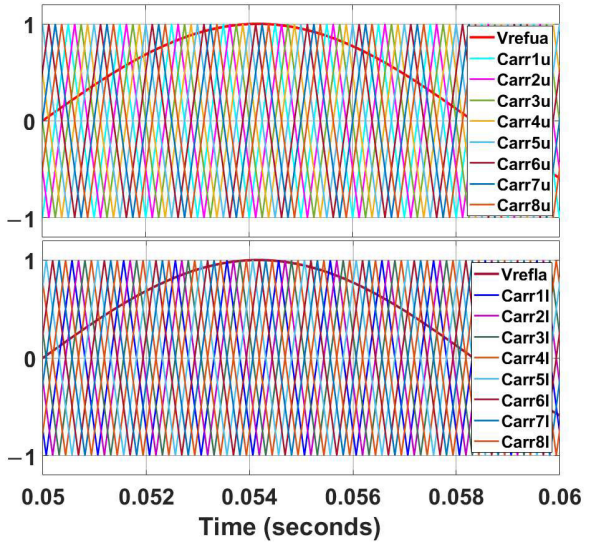

FIGURE 3. Reference voltage and carrier's waveforms in the upper and lower arm of phase a.

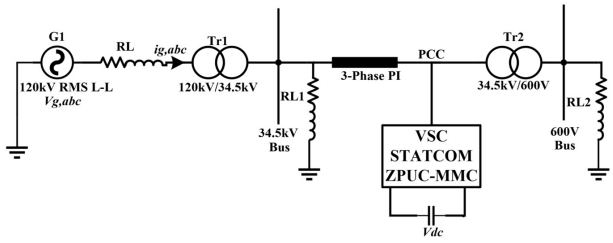

FIGURE 4. VSC ZPUC-MMC STATCOM connected in shunt with PCC.

output voltage can either be seven-level (7L-) or five-level (5L-). In this study, the 5L-ZPUC was selected due to its redundant switching states (see Table 2), which eliminates the need for an extra controller for capacitor voltage balancing, unlike the 7L-ZPUC. The voltage balancing (VB) for ZPUC capacitors is fully integrated within the modulation scheme.

The PS-PWM technique is employed for its various advantages including the uniform distribution of losses across all semiconductor switches, reduced Total Harmonics Distortion (THD), displacement of the harmonics further from the fundamental frequency, and enhancing the speed of integrated VB for auxiliary capacitors of ZPUC [21]. To achieve a 5L output at the ZPUC output, the capacitor voltages need to be set as per (1): capacitors C_1 and C_2 must hold 2E each, while capacitor C_3 should maintain E. Here, 2E represents the total DC voltage across the ZPUC-SM ($V_{dc,ZPUC}$) [13]. As a first step, PS-PWM is applied. To generate L voltage levels, L-1 carriers, and one reference voltage are required. The carriers must be phase-shifted by an angle of 360°/(L-1). In the case of a single ZPUC-SM, a 5L-output voltage is generated using four carriers that are phase-shifted by 360°/4. Selection between different redundant switching states is based on the conditions of capacitor voltages and arm current direction. For a detailed explanation of the integrated VB algorithm of ZPUC-SM within PS-PWM, please refer to [36].

$$v_{c1} = v_{c2} = 2E, v_{c3} = E \tag{1}$$

$$M_{phase} = 8N + 1 \tag{2}$$

$$M_{line} = 16N + 1 \tag{3}$$

B. ZPUC IN MMC-STATCOM

ZPUC-MMC STATCOM, as depicted in Fig. 2, comprises three legs, with each leg consisting of one upper and one lower arm. Each arm contains a total of N ZPUC-SMs, resulting in n ZPUC-SMs per leg. Upper and lower arm voltages constitute $4N + 1$ levels arranged between 0 and $4N$E in E steps, where $4N$E is the total DC link voltage V_{dc}. Phase voltages are composed of M_{phase} levels as in (2), arranged between -2NE and 2NE in E/2 steps. Line-to-line voltages are composed of M_{line} levels as in (3), arranged between -4NE and 4NE in E/4 steps. In this work two ZPUC-SM are used in each arm ($N = 2$), hence a total of 4 ZPUC-SM per leg. Therefore, 9L- are generated in each of the upper and lower arms voltages, and 17L- are generated in each phase voltage. For the efficient and reliable operation of ZPUC-MMC STATCOM, the three floating capacitors of each ZPUC-SM should be balanced and regulated as in (3). The same integrated VB algorithm within PS-PWM of a single ZPUC-SM is applied for MMC application. However, when more than one ZPU-SM is employed per arm, an energy sorting (ES) algorithm is required to achieve energy balancing between ZPUC-SMs within one arm, and between ZPUC-SMs from different arms.

At first, to generate the 9L- upper and lower arms voltages, and based on part A of section II, 8 carriers (L-1) are required in each of the upper and lower arms. The upper arms carriers should be phase-shifted from the lower arms carriers by an angle of 22.5° (180°/8). Meanwhile, carries within the upper arms are phase-shifted at an angle of 45° (360°/8). Therefore, considering phase a, upper arm carriers should be placed at 0°, 45°, 90°, 135°, 180°, 225°, 270°, and 315°. Lower arm carries are placed at 22.5°, 67.5°, 112.5°, 157.5°, 202.5°, 247.5°, 292.5°, and 337.5°. The carriers in both the upper and lower arms of phase a, alongside the voltage reference, are depicted in Fig. 3. After applying PS-PWM, the next stage involves utilizing the ES algorithm to calculate the total energies of each ZPUC-SM across all arms and phases, as defined in (4). These energies are then sorted in ascending order within matrix I, detailed (5). For instance, in the upper arm of phase a, I (1) represents the ZPUC-SM with the lowest energy, while I (2) corresponds

TABLE 3. Comparison with conventional topologies.

SM	%	SWL	CL	Complexity	Cost	Control
HB	M	L	L	L	L	Simple
U	M	L	L	M	M	Simple
FB	M	M	M	L	L	Simple
DC	H	L	M	H	M/H	Moderate
3L-NPC	H	H	H	M	M	Advanced
3L-FC	H	H	H	M	M	Advanced
5L-CCC	M	L	M	H	H	Complex
7L-PUC	H	L	Very L	Very H	H	Complex
5L-ZPUC	Very H	Very L	Very L	M	M	Moderate

to the ZPUC-SM with the highest energy. Subsequently, the selection of optimal redundant switching states is based on the current direction in each arm and the conditions of capacitor voltages, guided by the factors outlined in [42]. A detailed description of the integrated VB algorithm along with the ES algorithm is beyond the scope of this article. For a comprehensive explanation of the VB and ES algorithms, as well as the conditions governing capacitor voltages and arm current directions in generating the various voltage levels, please refer to [36], [42].

$$E_i = \sum_{i=1}^{N} Vc_{ij}^2; j = 1, 2, 3 \tag{4}$$

$$I = sort(E_i) \tag{5}$$

C. COMPARISON WITH OTHER CONVENTIONAL SM TOPOLOGIES

This section compares ZPUC with other topologies based on factors like switching losses, conduction losses, capacitor voltage ripple, efficiency, and complexity. Table 3 Presents a comparison with commonly used topologies. Since HB-SM was the first SM topology proposed for the MMC, all comparisons in the table are made with HB-SM as the baseline [43], [44], [45]. L, M, and H denote low, moderate, and high, while SWL and CL denote switching losses, and conduction losses, respectively.

The trade-off between efficiency, complexity, and cost. is acknowledged. While higher-level topologies offer better performance, they also increase complexity and cost. The choice of SM topology depends on application-specific factors such as voltage level, power rating, efficiency, and cost constraints. In this context, the comparison is between a multilevel SM topology and the HB-SM. HB-SM, consisting of only two switches, results in moderate switching and conduction losses as current flows through just two devices. Despite its simplicity, it lacks redundancy, and the capacitor voltage ripple is moderate, as the DC link voltage in the MMC is divided across a single capacitor within each HB-SM. In contrast, a multilevel SM topology increases the number of switches but introduces redundancy, which reduces switching losses by decreasing the number of switching events. Conduction losses are also minimized as the current is distributed across multiple devices, improving overall efficiency [46].

TABLE 4. Comparison between HB-MMC and ZPUC-MMC.

Symbol	HB-SM	ZPUC-SM
DC Voltage	60kV	60kV
AC Line-to-Line Voltage	34.5kV	34.5kV
System frequency	60Hz	60Hz
Switching Frequency	1000	1000
Modulation Index	0.95	0.95
Number of SM/arm	16	2
Voltage Levels	17L-	17L-
Number of switches/SM	2	6
Number of C/SM	1	3
Components/arm	48	18
Components/topology	288	108
Cells Capacitors	20mF	20mF
V caps	3.75kV	15kV, 7.5kV
Switches V Ratings	5kV	15kV, 7.5kV
Ripple in Vcaps	<5%	<1%

Multilevel topologies, like ZPUC-SM, generate higher voltage levels with fewer SMs, reducing filtering needs and mitigating harmonics. The finer voltage resolution minimizes capacitor voltage ripple, improving overall efficiency. In MMCs, ZPUC-SM divides the DC link voltage equally between the upper and lower legs, reducing voltage ripple compared to other topologies, which apply the full DC link voltage to both legs. Listing the comparisons and features of ZPUC-SM highlights its suitability for high-power applications, improving performance in reactive power compensation for STATCOM applications.

D. COMPARISON BETWEEN HB-SM AND ZPUC-SM FOR MMC AND JUSTIFICATION FOR SELECTING ZPUC OVER HB

Conventional MMC submodules, such as Half-Bridge (HB) and Full-Bridge (FB) have been the cornerstone of MMC design due to their simplicity, reliability, and straightforward control schemes. However, they often require numerous SMs to achieve high voltage levels, increasing system complexity and footprint. In contrast, ZPUC-SM introduces a more compact and efficient alternative by integrating multiple voltage levels within a single cell. This enhances voltage balancing, reduces the required number of SMs, the overall size and cost of the MMC, and offers superior redundancy. Table 4 compares HB-SM and ZPUC-SM for MMC STATCOM applications under identical operating conditions [36], [37].

ZPUC-SM outperforms the HB-SM by generating more voltage levels with fewer SMs per arm. For example, to generate 17 levels (17L-), the HB-MMC requires 16 HB-SMs per arm, resulting in 32 switches per arm (each HB-SM consists of two switches). In contrast, the ZPUC-MMC needs only two ZPUC-SMs per arm, using just 12 switches per arm (each ZPUC-SM consists of six switches). This reduction in the number of SMs lowers the switch count and minimizes switching and conduction losses, thereby improving efficiency and reliability.

In terms of voltage control, the HB-SM provides only two voltage levels per SM (positive or zero), leading to higher voltage ripples and more filtering requirements to maintain quality. In contrast, the ZPUC-SM offers five voltage levels per SM, enabling smoother voltage control, better resolution, and reduced harmonic distortion. ZPUC-SM also balances output voltage more effectively at lower switching frequencies, reducing losses and boosting efficiency.

Additionally, the ZPUC topology integrates well with the Phase-Shift Pulse Width Modulation (PS-PWM) control method, eliminating complex balancing algorithms, and making it ideal for medium/high-voltage applications like STATCOMs.

In a MMC with HB-SM, (i.e. MMC operates as a grid-connected inverter) the total DC link voltage of the MMC converter is applied to both the upper and lower legs of the converter. However, with ZPUC-SM, the DC link voltage is equally split between the upper and lower legs of each phase, resulting in a lower voltage ripple per SM and reduced component stress.

ZPUC-SM was chosen for its ability to generate higher voltage levels with fewer components, reducing switching and conduction losses compared to HB-SM. The choice supports a more efficient, cost-effective solution, simplifying the design while meeting the performance needs of the MMC STATCOM application. ZPUC-SM for MMC enhances performance, reduces component stress, and improves efficiency, making it ideal for applications requiring high-quality output with minimal distortion.

III. MODELING AND CONTROL OF ZPUC-MMC STATCOM

A. MATHEMATICAL MODEL AND GRID-CURRENT CONTROL

ZPUC-MMC STATCOM is implemented based on a voltage source converter (VSC) using a constant DC source represented by a DC link capacitor. The STATCOM is connected in shunt at the Point of Common Coupling (PCC) as shown in Fig. 4. A Switching modeling technique is adopted to extract the mathematical model presented in (6) to design the appropriate control system [37]. All the SMs of one arm are considered as one equivalent voltage source (v_{ui}, v_{li}). Using Kirchhoff's voltage law, the AC side voltages equation yields in (6), where, v_{ui} and v_{li} are the upper and lower arm voltages in phase i, v_{gi} and i_{gi} are the grid voltage and current in phase i, L_{arm}, R_{arm} are arm inductance and resistance respectively, and L_g, R_g are grid inductance and resistance. R_{arm} and R_g are very small, and they could be eliminated in all equations.

$$v_i - L_{eq}\frac{di_{gi}}{dt} + v_{gi} = 0, i = a, b, c \tag{6}$$

$L_{eq} = \frac{L_{arm}}{2} + L_g$, and $v_i = \frac{v_{li} - v_{ui}}{2}$, $i = a, b, c$

The aim is to use conventional controllers from existing literature to assess the functionality of a new application for ZPUC-MMC.

The control system, illustrated in Fig. 5 (a and b), employs decoupled PQ control in dq reference frame. It controls both

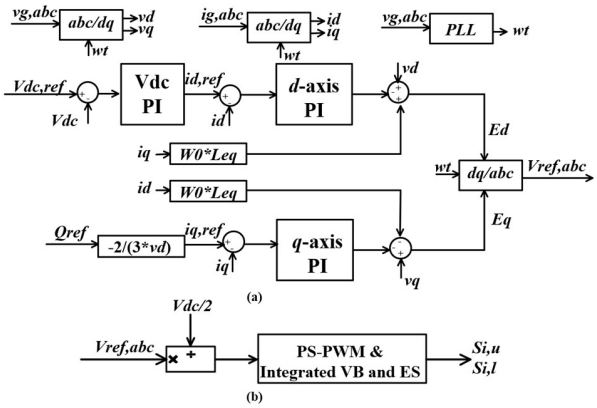

FIGURE 5. Control system of ZPUC-MMC STATCOM.

the d and q axis grid current separately by controlling the active power P and reactive power Q. Park transformation from abc reference frame to rotating $dq0$ reference frame is applied on (6), and the obtained d and q axis variables are as (7) and (8). Where, v_d and v_q, i_d and i_q, and E_d and E_q are the grid voltages, grid currents, and output voltages of the controllers respectively on the d-axis and q-axis and w_0 is the fundamental frequency.

$$E_d = v_d - L_{eq}\frac{di_d}{dt} + L_{eq}w_0 i_q \tag{7}$$

$$E_q = v_q - L_{eq}\frac{di_q}{dt} - L_{eq}w_0 i_d \tag{8}$$

Active and reactive power in $dq0$ reference frame is given below:

$$P = \frac{3}{2}(v_d i_d + v_q i_q) \tag{9}$$

$$Q = \frac{3}{2}(v_q i_d - v_d i_q) \tag{10}$$

Two PI controllers take action to regulate P to zero, and Q to follow reactive power reference Q_{ref}. The DC bus voltage is kept fixed throughout the d-axis external control loop. The command $i_{d,ref}$ is obtained by comparing the actual DC bus voltage (V_{dc}) with the reference DC bus voltage ($V_{dc,ref}$) On the other hand, the command $i_{q,ref}$, is driven by the control objectives for the STATCOM, the provision of the reactive power support. The q-axis reference current is calculated as follows: $i_{q,ref} = -2Q_{ref}/3v_d$.

B. CIRCULATING CURRENT CONTROLLER

In MMC, the instantaneous voltages among the three phases of the converter vary due to the voltage variation in the DC capacitors voltages of ZPUC and result in circulating current (CC) in each of the upper and lower arms of each leg. The relation between CC, output current (it is the grid current), and current in each arm is given as follows:

$$i_{ua} = i_{cca} + \frac{i_{ga}}{2} \tag{11}$$

$$i_{la} = i_{cca} - \frac{i_{ga}}{2} \tag{12}$$

TABLE 5. Upper and lower arms voltages and difference voltage.

Sum of V_u	Sum of V_l	ZPUC-MMC Output Voltage	V_{diff}
4NE	0	2NE	0
4NE	E	(4N-1)E/2	-E
(4N-1)E	0	(4N-1)E/2	E
(4N-1)E		(2N-1)E	0
:	:	:	:
:	:	:	:
E	4NE	-(4N-1)E/2	-E
0	4NE	-2NE	0

where $\boldsymbol{i_{ua}}$ and $\boldsymbol{i_{la}}$ are the upper and lower arms currents in phase a, and $\boldsymbol{i_{cca}}$ is the circulating current in phase a. The CC caused by the variation in the instantaneous voltages among the three legs of the converter is an inherent phenomenon in MMC. Although CC does not affect AC-side grid voltages and grid currents, it is preferred to reduce it as much as possible for an efficient and reliable operation of the MMC [47]. The CC is composed of a DC term in addition to a double-line frequency component and can be expressed as in (13).

$$i_{cci} = \frac{I_{dc}}{3} + I_{2f}\sin(2w_0 t + \varphi_0 + \varphi_i) \tag{13}$$

$i = a, b, c$, and $\varphi_i = 0, \frac{2\pi}{3}$, and $\frac{-2\pi}{3}$ respectively.
where, $\boldsymbol{i_{cci}}$ is the circulating current in each phase i, $\boldsymbol{I_{dc}}$ is the total DC current, and $\boldsymbol{I_{2f}}$ is the peak value of the second-order frequency component, $\boldsymbol{w_0}$ is the fundamental frequency, and $\boldsymbol{\varphi_0}$ is the initial phase angle between the grid current and grid voltage. The available inductances in each arm of a MMC not only isolate upper and lower arms but also play a role in limiting the CC. Increasing L_{arm} can reduce the CC to a certain extent but at the expense of increasing the size, weight, and cost of the converter [48]. CC control has been addressed extensively in literature, and various control methods have been developed.

In ZPUC-MMC, the circulating current is automatically controlled by the integrated VB within the PS-PWM. The main equation that describes the dynamic equation of the CC is described in (14). The equation shows that the difference between DC and AC voltage results in the CC.

Therefore, to mitigate/reduce the CC, this voltage difference should be minimized. Table 5 presents the upper and lower arm voltages corresponding to the $8N + 1$ states, along with the difference between DC and AC voltages (the circulating current). According to Table 5, this difference alternates between 0, E, and -E. Based on section II, part A, the total DC link voltage (V_{dc}) is equal to $4N$E, thus E is inversely proportional to N, the number of ZPUC-MS per arm. The expansion of the number of ZPUC-SM per arm (N) reduces the value of E, which describes the CC, that is the difference between DC and AC voltages.

$$v_{cci} = L_{arm}\frac{di_{cci}}{dt} + R_{arm}i_{cci} \tag{14}$$

where; $\boldsymbol{v_{cci}} = \frac{V_{dc}}{2} - (\frac{v_{li}+v_{ui}}{2})$.

C. INTEGRATED VB AND ES ALGORITHMS WITH PWM

Various modulation techniques have been applied to MMCs such as the PS-PWM, the Level-Shift PWM, the Nearest Level Modulation (NLM), and the Space Vector Modulation (SVM). PS-PWM is applied to ZPUC-MMC due to its various advantages (listed in Section II, Part A). The reference voltage, previously obtained from grid-current control, is fed into the PWM blocks, which integrate both VB and ES algorithms to balance the floating capacitors of each ZPUC-SM in each arm and to balance energy within each leg and across the three legs (phases a, b, and c). Additionally, the output signals from the PWM blocks serve as the switching signals for the upper and lower arm switches in each phase i, where i=a,b, and c.

IV. REAL-TIME IMPLEMENTATION PLATFORM

A. MAIN OBJECTIVES OF REAL-TIME SIMULATION

The main objective of RT simulation is to reproduce the output waveforms of a RT modeled plant that behaves identically to its physical prototype while maintaining high accuracy. To achieve RT simulation status, the execution or the computation of the modeled system should remain within the selected fixed time-step. This means that the execution time-step must be equal to or less than the selected fixed time-step. Otherwise, the execution time-step shrinks beyond the specified fixed time-step, leading to overruns, and RT simulation status is lost. The specified fixed time-step could be increased to eliminate overruns, but this affects the result's accuracy. To theoretically address the challenge of the execution time shrinking, two solutions are proposed. The first solution involves model simplification, where the complexity of the system model is reduced by using approximations or eliminating less critical components, helping to minimize the computational load and prevent the execution time-step from exceeding the selected fixed time-step. The second solution is parallel execution across multiple cores, which distributes the simulation tasks across the available cores on the real-time platform. This helps share the computational load and optimize execution time, though careful management of parallel execution is necessary to avoid synchronization issues. These approaches ensure that the system maintains real-time simulation status while preserving high accuracy in the simulation results.

B. REAL-TIME SIMULATION SOFTWARE AND HARDWARE

Due to the unavailability of a real physical small prototype, RT simulation is used to validate and verify the performance of the proposed converter and its control system under different modes of operation. Various RT simulation platforms are available today, such as Speedgoat, Typhoon HIL, and OPAL-RT. In this work, the OPAL-RT platform is used. Specialized hardware (Target) and software are required to perform RT execution. The OP4510 Target is employed in this work due to its availability in the GREPCI laboratory of the University. It offers a hybrid architecture with both

a powerful CPU and an FPGA for high-performance RT simulations. It integrates RT-LAB software and eFPGAsim RT platform. RT-LAB software is installed on a host PC at the GREPCI laboratory, and the host PC and the Target are connected via a Transmission Control Protocol (TCP), as illustrated in Fig. 6. In this article, a Model-in-the-Loop (MIL) or Control-in-the-Loop (CIL) simulation approach was used, where both the controller and the converter are modeled and executed using real-time hardware (Target). Specifically, the control system was executed on the CPU of the target, while the converter model was implemented and executed using the FPGA of the target. In industrial practice, alternative real-time simulation modes, such as Hardware-in-the-Loop (HIL) or Rapid-Control-Prototyping (RCP), can also be employed. In HIL mode, the controller is typically implemented on a Digital Signal Processor (DSP), while the converter model runs on the real-time target. In RCP mode, a physical prototype of the converter is used, which communicates with the real-time simulator for testing and validation.

RT-LAB software is fully compatible with MATLAB/SIMULINK and provides an environment for testing and debugging complex power electronics converters. In the first step, the control system (VB and ES algorithms, and current control) is implemented in SIMULINK/MATLAB using the Sim Power Block Set (SPS). Then, through RT-LAB software, the control model in SPS is adapted for RT simulation by using specified blocks from the RT-LAB Library. RT-LAB software is based on a top-level SIMULINK model where only subsystems (Main SM, and Secondary SS) can be executed. Each subsystem requires one core from the Target for execution. It is important to note that one core of the Target is allocated by default for the Target processor.

Additionally, the electric Hardware Solver (eHS) block from RT-LAB software is inserted to model the ZPUC-MMC converter via the integrated schematic editor in eHS, which allows the design of ZPUC-MMC using switches, capacitors, inductors, and DC voltage source [49]. The Target hardware OP4510 typically consists of a high-performance processor (CPU) composed of four Intel Xeon 3.5GHZ processor cores, and one Xilinx Kintex-7 325T FPGA. The model subsystems executed using Target cores require a minimum time-step of 7μs. However, for models executed on FPGA chips, a minimum time-step of 250ns is necessary.

C. REAL-TIME SIMULATION OF 17L-ZPUC-MMC STATCOM

Using only CPU-based RT simulation for complex power electronics systems, such as the ZPUC-MMC, is impractical. When utilizing only CPU-based RT simulation, the entire system (converter and control) is implemented in RT-LAB. The control (SM) is set as the main subsystem, while the converter (SS) is the secondary subsystem. In this setup, the system runs on just two cores of the Target machine. For instance, when employing one ZPUC-SM in a MMC, real-time status can only be obtained with a time-step of 47μs, which is quite large and negatively impacts accuracy. Increasing further the number of ZPU-SMs within the MMC arm results in more components, including switches and non-linear devices, which pose additional computational challenges and increase the CPU load. This can lead to the CPU becoming fully loaded, generating overruns.

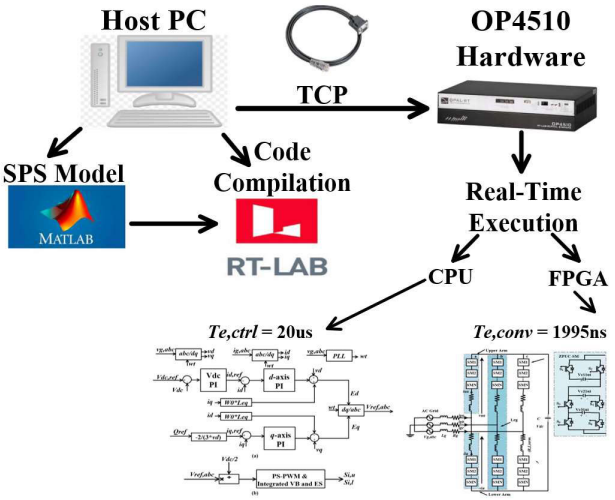

FIGURE 6. Real-Time implementation of 17L-ZPUC-MMC.

When overruns occur, the executed time-step does not meet the specified time-step, causing results to be time-differed (offline) and not real-time. Increasing the specified time-step might be an alternative, but it comes at the expense of accuracy. Meanwhile, decomposing the system into additional subsystems to distribute execution across different available cores is challenging in terms of maintaining parallel execution. Therefore, for RT execution of ZPUC-MMC, both CPU and FPGA-based RT simulation should be employed. In this case, the control system is implemented on RT-LAB by transforming the control SPS model into a valid RT-LAB model using RT-LAB blocks library. The control system is then executed by the Target core. On the other hand, ZPUC-MMC STATCOM is implemented in the schematic editor, which is fully integrated within the eHS block of RT-LAB and then executed using the FPGA of the Target.

A significant contribution of the work is adapting the model of the converter for real-time simulation, ensuring verification and validation while achieving zero-overruns. Obtaining the model of the converter in the eHS block for FPGA execution required extensive tuning of the internal parameters of the converter switches presented in the schematic editor.

V. REAL-TIME SIMULATION RESULTS

The proposed system along with its control system is implemented and executed on a RT simulation platform in a Model-in-the-Loop (MIL) mode of operation. The control system is executed with a time-step of 20μs ($T_{e,ctrl}$), and the converter itself is executed with a time-step of 1995ns ($T_{e,conv}$). The setup of the RT platform shown in Fig. 6 is completed by connecting the host PC and the OPAL-RT target

TABLE 6. System parameters.

Parameters	Symbols	Values
RMS line-to-line Voltage	V_s	34.5kV
Grid Frequency	f_0	60Hz
DC Voltage Reference	$V_{dc,ref}$	60kV
Reactive Power Range	Q_{ref}	-150/150Mvar
Grid Reactance and Resistance	L_g, R_g	1mH, 0.1Ω
Arm Inductance and Resistance	L_{arm}, R_{arm}	0.5mH,0.05Ω
Number of ZPUC-SM per arm	N	2
ZPUC Capacitors	C_1, C_2, C_3	30mF
Switching Frequency	f_{sw}	1000Hz

Hardware (OP4510) via a Transmission Control Prototype (TCP). The target features 3.5GHz Intel Xeon four-core processors with Red Hat Linux Operating System and a powerful Xilinx Kintex-7 FPGA. The simulation parameters are outlined in Table 6. Assuming a balanced three-phase system, the results per phase 'a' will only be displayed and analyzed.

A. BALANCED THREE-PHASE SYSTEMS

At t = 25s, the compensated reactive power shifts from -150 Mvar capacitive to 150 Mvar inductive. Consequently, the grid-side current changes from leading the grid voltage by 90° to lagging it by 90° as depicted in Fig. 7. Notably, throughout this transition, the current waveform maintains a perfect sinusoidal shape. According to Fig. 7, 17L-($8N + 1$) phase voltage (v_{pa}) is perfectly generated and arranged between $-V_{dc}/2$ (-30kV) and $V_{dc}/2$ (30kV) in E/2 steps (3.75kV). In addition, 9L- ($4N + 1$) upper and lower arm voltages (v_{ua}, v_{la}) are quite generated and are arranged between 0 and 4NE (60kV) in E steps (7.5kV). These 9L-voltages result from adding the 5L- voltages generated by each ZPUC-SM in each upper arm (v_{u1a}, v_{u2a}) and lower arm (v_{l1a}, v_{l2a}) as shown in Fig. 8. This shows the good dynamic performance of the proposed system through FPGA-based RT simulations. Also, the DC bus voltage remains constant with zero steady-state error as shown in Fig. 9, enabling uninterrupted converter operation. According to Fig. 10, the integrated VB and ES algorithms are perfectly achieved. The three capacitor voltages of each ZPUC-SM in each upper and lower arm of phase 'a' are very well balanced and regulated around desired values with a small voltage ripple. The voltages of capacitors C_1 and C_2 of each ZPUC-SM in each arm are equal to 2E (15kV), and the voltage of capacitor C_3 is equal to E (7.5kV). Thus, $v_{c1xja} = v_{c2xja}$ =15kV, and v_{c3xja} =7.5kv, where; $x = 1, 2$ is the index of ZPUC-SM in each arm, and $j = u, l$ is the index of each arm (upper, lower) in phase a.

B. DYNAMIC OPERATION

To assess the dynamic performance of the proposed converter, tests were conducted under variations in the DC voltage reference and reactive power reference.

The first variation involves a step change of 20% in the DC voltage reference, applied at t = 25s, increasing V_{dcref} from 60kV to 72kV. Additionally, at t = 25s, the compensated reactive power shifts from capacitive to inductive. The respective results are depicted in Fig. 11. It is clearly observed that the grid-current control remains robust against DC voltage variations: the current remains sinusoidal, leading the grid voltage by 90° before the step change (capacitive reactive power) and shifting to lagging the grid voltage by 90° after the step change (inductive reactive power). Similarly, 9L- voltages are generated in each of the upper and lower arms (v_{ua}, v_{la}), with 17L- voltages appearing in the phase voltage (v_{pa}). However, these voltage levels adapt to the newly applied DC voltage value (72kV), validating the previously introduced formulas in (1), (2), and (3) in section II. Consequently, the upper and lower arm voltages are arranged between 0 and $4E$ (72kV), while the 17L- phase voltage varies between $V_{dc}/2$ (36kV) and -$V_{dc}/2$ (-36kV). Furthermore, the three capacitors of ZPUC-SM1 in both the upper and lower arms of the phase

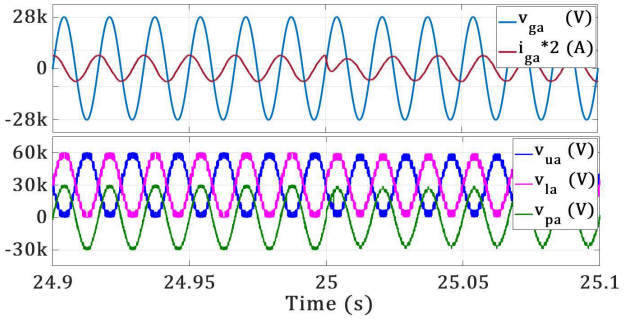

FIGURE 7. Grid voltage and current (v_{ga}, i_{ga}), 9L-upper and lower arm voltages (v_{ua}, v_{la}), and 17L- phase voltage (v_{pa}) in phase a.

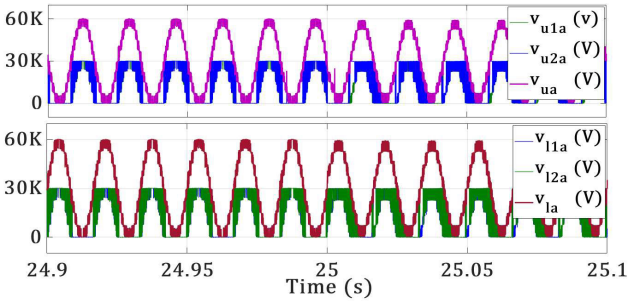

FIGURE 8. 5L- ZPUC-SMs voltages in upper and lower arm (v_{u1a}, v_{u2a}, v_{l1a}, v_{l2a}), and 9L- upper and lower arm voltages (v_{ua}, v_{la}) in phase a.

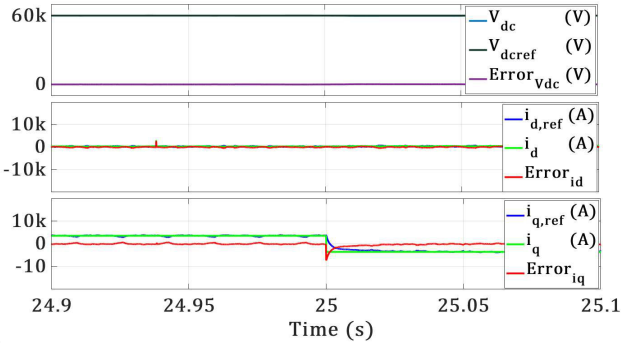

FIGURE 9. DC bus voltage (V_{dc}), and currents on the d and q axes.

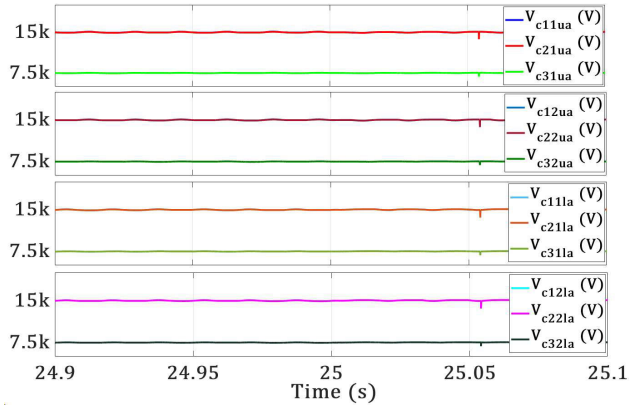

FIGURE 10. Capacitor voltages of ZPUC-SMs in phase a.

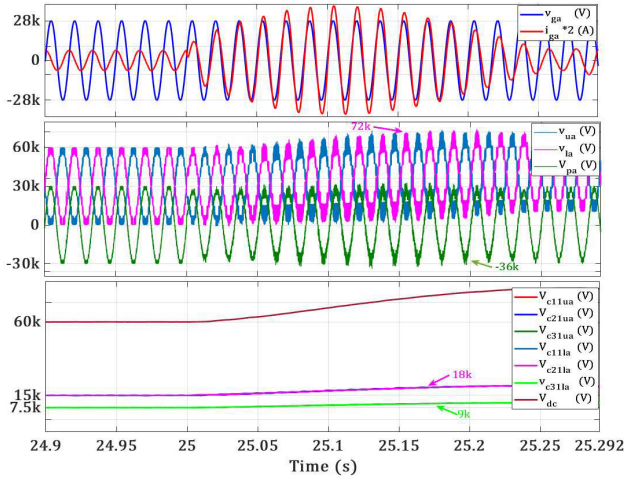

FIGURE 11. Dynamic operation: DC voltage variation.

'a' maintain balance around their desired values according to the new DC voltage, validating the effectiveness of the voltage balancing and energy sorting algorithms integrated within the PS-PWM. Specifically, V_{c11ua}, V_{c21ua}, V_{c11la}, and v_{c21la} are balanced and regulated around $2E = 18$kV, while $V_{C31ua} = V_{c31la} = 9\text{kV} = E$. The capacitor voltage ripple remains below 10%.

The second variation involves a step change in the reactive power reference over a time range of 50 seconds, aimed at ensuring the STATCOM operates efficiently across its full operating range, from -150 Mvar to +150 Mvar. The dynamic step change is illustrated in Fig. 12, with the corresponding real-time simulation results shown in Figs. 13, 14, and 15. Since each second in the real-time simulation corresponds to one second in the real world, and given the difficulty of testing the three different variations within the same time range (0s-50s), the results are divided into three time-slots: at t = 15s, a step change is applied, reducing the reactive power reference from -150 Mvar into -75 Mvar. At t = 25s, another step change occurs, shifting the reactive power reference from capacitive (-75 Mvar) to inductive (75Mvar). Finally, at t = 35 s, the inductive reactive power increases to 150 Mvar.

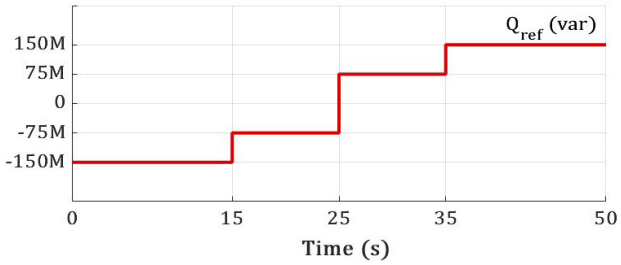

FIGURE 12. Dynamic operation: reactive power step variation.

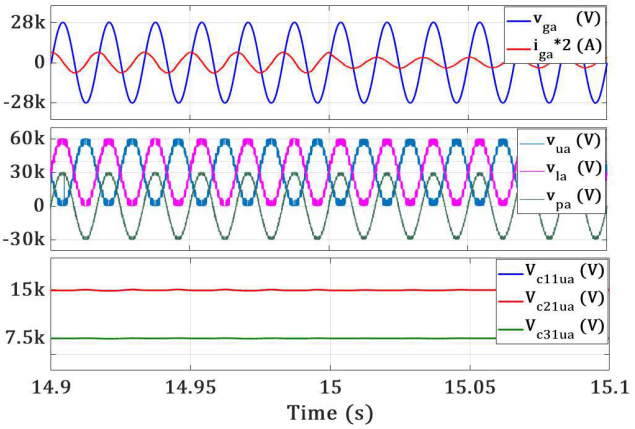

FIGURE 13. Dynamic operation: -150Mvar to -75 Mvar.

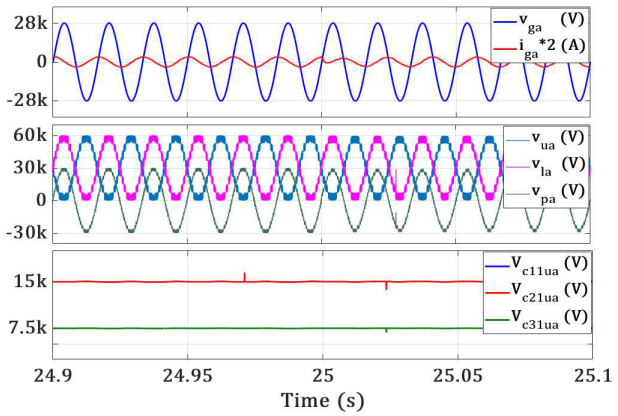

FIGURE 14. Dynamic operation: -75 Mavr to +75 Mvar.

As shown in Fig. 13, the sinusoidal grid current consistently leads the grid voltage by 90°, but at t = 15s, the current amplitude decreases due to the reduction of the reactive power reference to -75 Mvar. At t = 25s, the current shifts from leading to lagging the grid voltage by 90°, as the reference changes from capacitive to inductive as described in Fig. 14. In Fig.15, the current continues lagging the grid voltage by 90°, but its amplitude increases as the reactive power reference is stepped from 75 Mvar to 150 Mvar.

In all cases, the same number of voltage levels (9L-) are generated in each of the upper and lower arms of phase a, and 17L- phase voltage is consistently generated. Additionally, the capacitors of each ZPUC-SM continue to balance around their regulated values, validating the robustness and

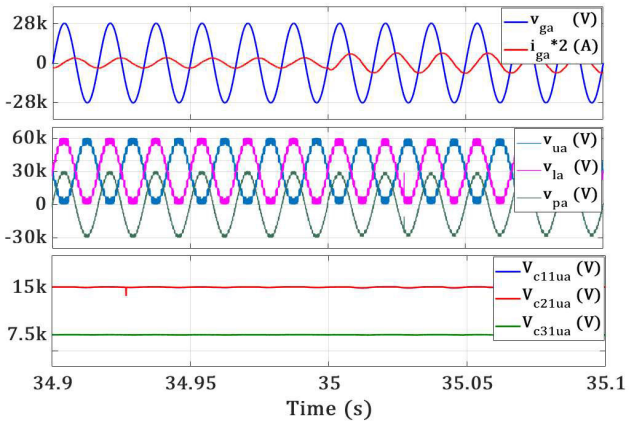

FIGURE 15. Dynamic operation: +75 Mvar to +150 Mvar.

effectiveness of the voltage balancing and energy sorting algorithms integrated within the PS-PWM.

VI. TOPOLOGY LIMITATIONS AND FUTURE WORK

One potential advantage of the ZPUC-SM in MMC systems is its ability to boost voltage levels using fewer building blocks (SMs). It also has a simpler design due to the lower number of components, and it incorporates an automatic voltage balancing function achieved through a PS-PWM technique. However, one drawback of ZPUC-SM is that it operates with only one voltage polarity (unipolar) and switching devices cannot block DC fault currents. External DC circuit breakers are required. However, they are not as mature as AC circuit breakers and have some related losses, fault clearing time, and arcing time [50]. Therefore, for High-/Medium-Voltage Direct Current (HVDC and MVDC) MMC applications, using ZPUC is challenging due to the high probability of experiencing pole-to-pole or pole-to-ground faults. A DC fault is one of the severe faults that can occur in an MMC and has a significant impact on the grid. It is usually classified based on the distance between the fault and the DC connection point. A DC fault occurring 1 meter away from the DC connection point is considered the worst-case scenario for a converter. The switches will be subjected to high overcurrent that will propagate to the AC side if the fault is not isolated. To overcome this limitation, the authors are developing a new submodule design that combines the strengths of both ZPUC and Full-Bridge configurations. This hybrid design aims to include the capability to block DC faults.

Future work could focus on developing advanced control strategies, such as Model Predictive Control (MPC) or Adaptive Control, to further optimize the performance of MMC-based STATCOMs under dynamic conditions and varying grid scenarios. Another important research area involves improving component reliability, particularly capacitors and switches in submodules. Long-term reliability studies and improvements in power semiconductor technologies are essential for reducing maintenance costs and extending system lifespans.

In ZPUC-MMCs, circulating current control is inherently integrated with voltage balancing and modulation techniques. While arm inductors help to minimize CC, it cannot be totally eliminated. However, the presence of second-order harmonics within the CC can be addressed. This opens the door to a novel approach: exploring the application of external controllers, like those used in established MMC configurations such as the HB-MMC, to manage CC independently. Such an approach could potentially allow for its complete suppression [51].

VII. CONCLUSION

This work introduces a promising MMC-STATCOM based on ZPUC-SM, thoroughly exploring its adaptation for FPGA-based real-time simulation. The proposed ZPUC-MMC offers several advantages, including fewer components, lower cost, increased voltage levels, and highly accurate real-time simulation results, validating the converter's operation. The system operates in VAR compensation mode, using conventional controllers based on the decoupled *dq* reference frame for grid current internal loop regulation, and DC bus voltage external loop regulation. Despite these benefits, technical challenges remain, particularly in blocking DC faults and controlling circulating currents in MMCs. Future research will focus on developing a hybrid ZPUC design to address DC fault blocking and exploring advanced control techniques to fully mitigate circulating currents. Additionally, further investigation into integrating real-time hardware simulations with physical prototypes will be crucial for validating the proposed system in industrial applications.

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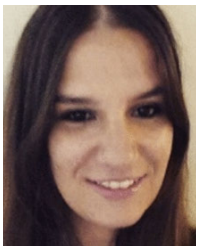

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